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SN54LS299, SN54S299 . . . J OR W PACKAGE **Multiplexed Inputs/Outputs Provide** • SN74LS299, SN74S299 . . . DW OR N PACKAGE Improved Bit Density (TOP VIEW) Four Modes of Operations: 19 S1 Hold (Store) Shift Left 18 SL G2 🛛 3 Shift Right Load Data 17 DOH G/QG 4 E/QE 16 □н/он Operates with Outputs Enabled or at High Z **[**6 15 C/QC 14 D/QD A/QA 13 B/QB **[**]8 • 3-State Outputs Drive Bus Lines Directly QA' 12 CLK 10 GND 0 Can Be Cascaded for N-Bit Word Lengths • SN54LS323 and SN74LS323 Are Similar But SN54LS299, SN54S299 ... FK PACKAGE **Have Synchronous Clear** (TOP VIEW) ល្អី ស្ត្រី ស្ត្រី ស្ត្រី Applications: Stacked or Push-Down Registers **Buffer Storage, and Accumulator** G/QG[] 4 18 []SL E/QE 5 Registers 17 []QH' C/QC]6 16 [H/QH GUARANTEED TYPICAL A/QA] 7 15 [F/QF QA']8 TYPE SHIFT (CLOCK) POWER 14 D/QD FREQUENCY DISSIPATION 10 11 12 'LS299 25 MHz 175 mW 'S299 50 MHz 700 mW

description

These Schottky TTL eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

				INPL	ITS						IN	PUTS/0	DUTPU	TS			OUT	PUTS
MODE	CLR	FUNC		CON	TPUT TROL	CLK	CLK SERIAL		A/QA	8/Q8	c/ac	D/QD	E/QE	F/Q _F	G/QG	н/о _н	a _{A'}	a _{H'}
		S1	SO	G1†	G2†		SL	SR										
	L	×	L	L	L	х	X	х	L	L	L	L	L	L	L	L	L	L
Clear	L	L	х	L	L	х	X	X	L	L	L	L	L	L	L	L ·	L	L
	L	н	н	х	X	х	X	х	×	x	х	×	х	х	х	×	L	L
Hold	н	L	Ł	L	۴L	x	X	x	QAO	O _{B0}	Q _{C0}	0 _{D0}	QE0	QF0	Q _{G0}	0 _{H0}	QA0	QHO
	н	X	x	L	L	٤	×	x	QAO	0 _{B0}	QC0	Q _{D0}	Q _{E0}	QFO	QGO	Q _{H0}	QA0	QH0
Chife Diaha	н	L	н	L	L	t	X	н	н	QAn			QDn	QEn	QFn	QGn	н	QGn
Shift Right	н	L	н	L	L	1	X	L	L	QAn	QBn		0 _{Dn}			QGn	L	QGn
01:11.1.11	н	н	L	L	L	t	н	X	QBn	QCn	QDn	QEn	QEn	QGn	QHn	н	Q _{8n}	н
Shift Left	н	Ĥ H	L	L	L	1	L	х	QBn	QCn	QDn		QFn	QGn	QHn	L	QBn	L
Load	н	н	н	X	X	t	x	X	а	b	c	d	e	f	9	h	a	h

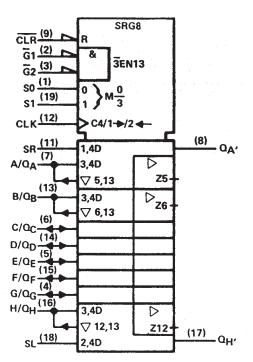
a... h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.



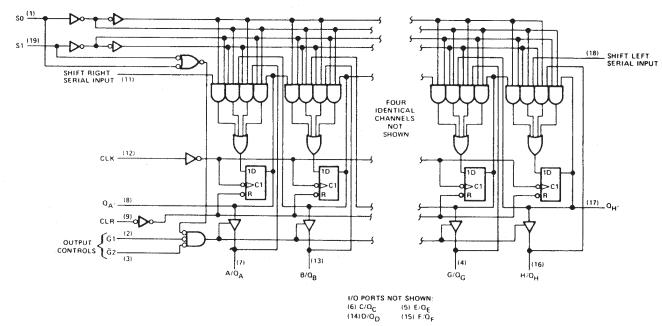
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logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, N, and W packages.



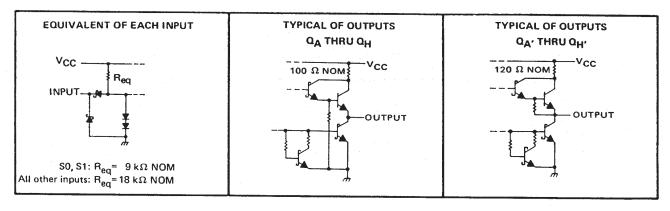
logic diagram (positive logic)

Pin numbers shown are for DW, J, N, and W packages.



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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)											•	•				. 7 \	1
Input voltage																. 7 \	/
Off-state output voltage																5.5 \	/
Operating free-air temperature range: SN54LS	299				• •									-55°(C to	125°C	5
SN74LS	299	•	•••	•						•			•	. 0'	°C to	o 70° (;
Storage temperature	•••	•	• •	•	• •	•	• •	•		•	•			65°(C to	150°C	2

NOTE 1: Voltage values are with respect to network ground terminal,

recommended operating conditions

		s	N54LS2	99	s	N74LS2	99	
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, VCC		4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH	Q _A thru Q _H			-1			-2.6	
main rever earpar carrent, IOH	QA' or QH'			-0.4		· · ·	-0.4	mA
Low-level output current, IOL	Q _A thru Q _H			12			24	<u> </u>
	Q _A ' or Q _H '			4			8	mA
Clock frequency, fclock		0		20	0		20	MHz
Width of clock pulse, tw(clock)	Clock high	30			30			1
	Clock low	1.8			10			ns
Width of clear pulse, tw(clear)	Clear low	25			20			ns
	Select	351			351			
Setup time, t _{su}	High-level data [†]	201			201			1
	Low-level data [†]	201			201			ns
	Clear inactive-state	241			201			
Hold time, t _h	Select	101			101			
	Data [†]	3†			01			ns
Operating free-air temperature, TA		-55		125	0		70	°c

 † Data includes the two serial inputs and the eight input/output data lines.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST COND	UTIONST	SI	V54LS2	99	St	N74LS2	99	
	TANAMETEN		TESTCONL	ATTONS .	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	UNIT
Чн	High-level input voltage			-	2			2			V
VIL	Low-level input voltage		·				0.7			0.8	V
VIK	Input clamp voltage		V _{CC} = MIN,	I _I = -18 mA			-1.5			-1.5	V
Val	High lovel output voltage	Q _A thru Q _H	$V_{CC} = MIN,$	V _{IH} = 2 V,	2.4	3.2		2.4	3.1		
∨он	High-level output voltage	QA' or QH'	VIL = VILmax,	IOH = MAX	2.5	3.4		2.7	3.4		V
		Q _A thru Q _H	V _{CC} = MIN,	$I_{OL} = 12 \text{ mA}$		0,25	0.4		0.25	0.4	
VOL	Low-level output voltage	ad and all	$V_{\rm H} = 2 V$,	IOL = 24 mA					0.35	0.5	l v
VUL	Low-level output voltage	QA' or QH'	VIH = 2 V, VIL = VILmax	IOL = 4 mA		0.25	0.4		0.25	0.4	1 °
		at or att		IOL = 8 mA					0.35	0.5	1
IOZH	Off-state output current,	Q _A thru Q _H	V _{CC} = MAX,	V _{IH} = 2 V,			40			40	μΑ
·02n	high-level voltage applied	ag and an	V _O ≈ 2.7 V				40			40	<u></u> ۳۵
^I OZL	Off-state output current,	Q _A thru Q _H	$V_{CC} = MAX,$	V _{IH} = 2 V,			400			-400	μΑ
-021	low-level voltage applied	ag und an	V _O = 0.4 V				400			- 400	μ
	Input current at maximum	S0, S1		V ₁ = 7 V			200			200	
4	input voltage	A thru H	V _{CC} = MAX	V ₁ = 5.5 V			100			100	μΑ
	input voltage	Any other		Vi = 7 V			100			100	1
t	High-level input current	A thru H, SO, S1		V1 = 2.7 V			40			40	
ŧн	rign-level input current	Any other	V _{CC} = MAX,	$v_1 = 2.7 v_1$	-		20			20	μA
1	Low-level input current	S0, S1	V	× - 0.4 ×			-0.8			-0.8	
μL	cow-level input current	Any other	V _{CC} = MAX,	V ₁ = 0.4 V			-0.4			-0.4	m A
	Short-circuit output current§	Q _A thru Q _H		······································	30		130	-30		-130	
los	short-circuit output current •	Q _{A'} or Q _{H'}	V _{CC} = MAX		-20		-100	-20		-100	- mA
ICC	Supply current		V _{CC} = MAX		1	33	53		33	53	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. [‡]All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 V$, $T_A = 25^{\circ}C$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	түр	MAX	UNIT
f _{max}			See Note 2	20	35		MHz
tPLH	CLK	0.4.07.0.4	$R_1 = 2 k\Omega$, $C_1 = 15 pF$	1	22	33	
^t PHL	- CLK	Q _A ' or Q _H '	$H = 2 K_{32}, C = 15 \text{ pr}$	-	26	39	ns
tPHL .	CLR	QA' or QH'	7		27	40	ns
^t PLH	0	Q _A thru Q _H			17	25	
^t PHL	CLK		$R_1 = 665 \Omega$, $C_1 = 45 pF$		26	39	ns
^t PHL	CLR	Q _A thru Q _H			26	40	ns
^t PZH	<u> </u>	Q _A thru Q _H	7		13	21	
^t PZL	01,02	CA III CA			19	30	ns
^t PHZ	<u> </u>	Q _A thru Q _H	$R_L = 665 \Omega$, $C_L = 5 pF$	1	10	20	
^t PLZ					10	15	ns

 $\P_{f_{max}} \equiv \max(mum \ clock \ frequency$

tpLH = propagation delay time, low-to-high-level output.

tpHL ≡ propagation delay time, high-to-low-level output

 $tp_{ZH} \equiv output enable time to high level$

 $t_{PZL} \cong output enable time to low level$

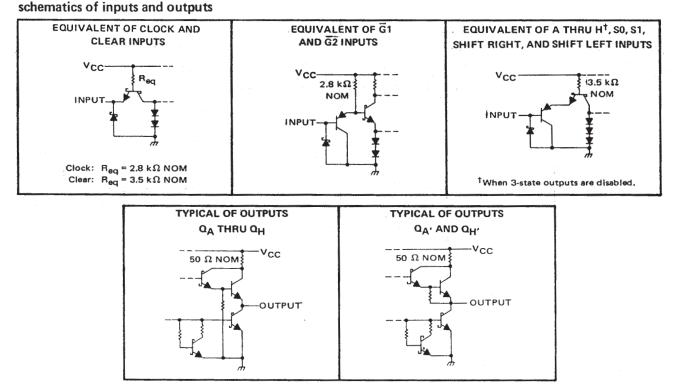
 $t_{PHZ} \equiv$ output disable time from high level

 $t_{PLZ} \equiv output disable time from low level$

NOTE 2: For testing fmax, all outputs are loaded simultaneously, each with CL and RL as specified for the propagation times, Load circuits and voltage waveforms are shown in Section 1.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1) 7 V
Input voltage
Off-state output voltage
Operating free-air temperature range: SN54S299 (See Note 1)55°C to 125°C
SN74S299
Storage temperature range

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		S	SN54S29	9		SN74S29	9	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH	Q _A thru Q _H			-2			-6.5	mA
inginever output current, IOH	Q _A ' or Q _H '			0.5			0.5	mA
Low-level output current, IOI	Q _A thru Q _H			20			20	mA
	Q _A ' or Q _H '			6			6	mA
Clock frequency, fclock		0		50	0		50	MHz
Width of clock pulse, tw(clock)	Clock high	10			10			
(clock)	Clock low	10			10			ns
Width of clear pulse, tw(clear)	Clear low	10			10			ns
	Select	15†			15†			
Setup time, t _{su}	High-level data‡	71			71			
Setup time, isu	Low-level data [‡]	51			51			ns
	Clear inactive-state	10†			101			
Hold time, t _h	Select	51			51			
	Data‡	51			51			ns
Operating free-air temperature, TA		-55		125	0		70	°C

[‡] Data includes the two serial inputs and the eight input/output data lines.



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	PARAMETER		TEST CON	DITIONST	MIN	түр‡	MAX	UNIT
VIH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	v
VIK	Input clamp voltage		V _{CC} = MIN,	$l_{1} = -18 mA$			-1.2	v
v _{он}	High-level output voltage	Q _A thru Q _H	V _{CC} = MIN,	VIH = 2 V,	2.4	3.2		
TOH		QA' or QH'	V _{IL} = 0.8 V,	IOH = MAX	2.7	3.4		V
VOL	Low-level output voltage	•	V _{CC} = MIN,	V _{1H} = 2 V,		·····		
- OL			VIL = 0.8 V,	IOL = MAX			0.5	V
IOZH	Off-state output current,	0 11 0	V _{CC} = MAX,	VIH = 2 V,				
-024	high-level voltage applied	Q _A thru Q _H	V ₀ = 2.4 V				100	μA
OZL	Off-state output current,	Q the Q	V _{CC} = MAX,	VIH = 2 V,				
-02L	low-level voltage applied	Q _A thru Q _H	V _O = 0.5 V				-250	μA
4	Input current at maximum input voltage		V _{CC} = MAX,	V _I = 5.5 V			1	mA
ŧн	High-level input current	A thru H, SO, S1					100	
		Any other	V _{CC} = MAX,	V ₁ = 2.7 V			50	μA
		CLK or CLR					-2	mA
HL.	Low-level input current	S0, S1	V _{CC} = MAX,	Vi = 0.5 V			-500	μA
		Any other		i i			-250	μA
los	Short-circuit output current§	Q _A thru Q _H			-40		-100	·
		Q _A ' or Q _H '	V _{CC} = MAX		-20		-100	mA
'cc	Supply current		V _{CC} = MAX			140	225	mA

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

 \ddagger All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 V$, $T_A = 25^{\circ}C$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	түр	MAX	UNIT
f _{max}			See Note 2	50	70		MHz
^t PLH	CLK	0.4.05.0.4		1	12	20	
^t PHL		Q _A ' or Q _H '	$R_L = 1 k\Omega$, $C_L = 15 pF$		13	20	ns
^t PHL	CLR	Q _A ' or Q _H '			14	21	ns
^t PLH	CLK	0	-		15	21	
^t ₽HL		Q _A thru Q _H			15	21	ns
^t PHL	CLR	Q _A thru Q _H	$R_{L} \approx 280 \ \Omega$, $C_{L} = 45 \ pF$.		16	24	ns
^t PZH	<u><u> </u></u>	0 11 0	-		10	18	
^t PZL		Q _A thru Q _H			12	18	ns
^t PHZ	<u> </u>	0.11.0	$R_1 = 280 \Omega, C_1 = 5 pF$		7	12	
^t PLZ		م Q _A thru Q _H			7	12	ns

¶f_{max} = maximum clock frequency

tpLH = Propagation delay time, low-to-high-level output

tpHL = Propagation delay time, high-to-low-level output

tpzH = output enable time to high level

tpzL = output enable time to low level

tpHZ = output disable time from high level tpLZ = output disable time from low level

NOTE 2: For testing fmax, all outputs are loaded simultaneously, each with CL and RL as specified for the propagation times.

Load circuits and voltage waveforms are shown in Section 1.





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PACKAGING INFORMATION

Orderable Device	Status ("	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
78024012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
7802401RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
7802401RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
7802401SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
7802401SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
SN54LS299J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SN54LS299J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SN54S299J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	
SN54S299J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	
SN74LS299DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS299DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS299DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS299DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS299DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS299DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS299N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS299N	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS299NE4	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS299NE4	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74S299DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	
SN74S299DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	
SN74S299DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	
SN74S299DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	
SN74S299N	OBSOLETE	PDIP	Ν	20		TBD	Call TI	Call TI	
SN74S299N	OBSOLETE	PDIP	Ν	20		TBD	Call TI	Call TI	



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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74S299N3	OBSOLETE	PDIP	Ν	20		TBD	Call TI	Call TI	
SN74S299N3	OBSOLETE	PDIP	Ν	20		TBD	Call TI	Call TI	
SNJ54LS299FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS299FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS299J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SNJ54LS299J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SNJ54LS299W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	
SNJ54LS299W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	
SNJ54S299FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	
SNJ54S299FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	
SNJ54S299J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	
SNJ54S299J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	
SNJ54S299W	OBSOLETE	CFP	W	20		TBD	Call TI	Call TI	
SNJ54S299W	OBSOLETE	CFP	W	20		TBD	Call TI	Call TI	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LS299, SN54S299, SN74LS299, SN74S299 :

• Catalog: SN74LS299, SN74S299

• Military: SN54LS299, SN54S299

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20



LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N**) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AC.



LAND PATTERN DATA



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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