Asynchronous Clear

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
′164	36 MHz	21 mW per bit
'LS164	36 MHz	10 mW per bit

description

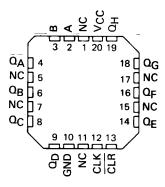
These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup-time requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

The SN54164 and SN54LS164 are characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to 125 $\,^{\circ}$ C. The SN74164 and SN74LS164 are characterized for operation from 0 $\,^{\circ}$ C to 70 $\,^{\circ}$ C.

SN54164, SN54LS164...J OR W PACKAGE SN74164...N PACKAGE SN74LS164...D OR N PACKAGE (TOP VIEW)

д [1 2	14 V _{CC}
$a_A \Box$	3	12 \(\oldsymbol{12} \)
α_{B} [4	11 QF
α _C □	5	10∏ Q E
$\sigma_{D} \sqsubset$	6	9 ☐ CLR
GND [7	8DCLK

SN54LS164 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

FUNCTION TABLE

L	INPUTS				OUTP	UTS
CLEAR	CLOCK	Α	В	α_{A}	α_{B}	Q _H
L	X	Х	Х	L	L	L
Н	L	×	Х	Q _{A0}	o_{B0}	α_{H0}
Н	1	н	Н	Н	\mathbf{Q}_{An}	Q_{Gn}
Н	1	L	X	L	\mathbf{Q}_{An}	q_{Gn}
Н	1	Х	L	L	Q _{An}	Q_{Gn}

H = high level (steady state), L = low level (steady state)

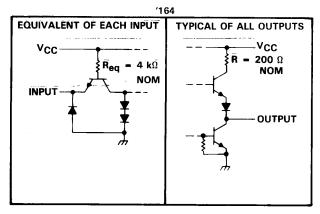
X = irrelevant (any input, including transitions)

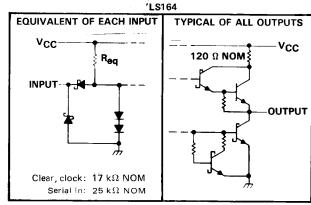
↑ = transition from low to high level.

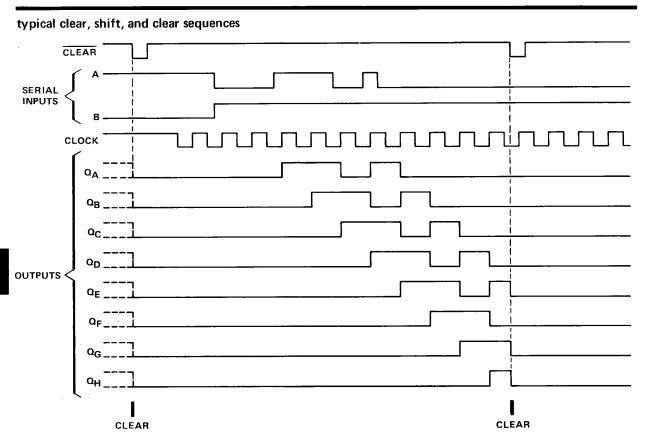
 ${
m Q}_{A0},\,{
m Q}_{B0},\,{
m Q}_{H0}$ = the level of ${
m Q}_A,\,{
m Q}_B,\,{
m or}\,\,{
m Q}_H,$ respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

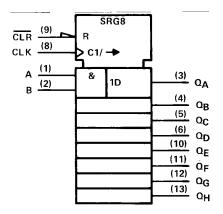
schematics of inputs and outputs





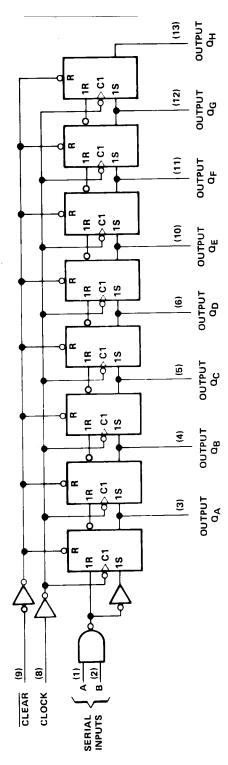


logic symbol†



 $^{^{\}dagger}$ This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

SN54164, SN74164 **8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS**

absolute maximum ratings over oprating	g free-air temperature range (unless otherwise noted)
Input voltage	

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54164				UNIT		
	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, VCC	4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH			-400			-400	μΑ
Low-level output current, IQL			8	<u> </u>		8	mA
Clock frequency, fclock	0		25	0		25	MHz
Width of clock or clear input pulse, tw	20			20			ns
Data setup time, t _{su} (see Figure 1)	15			15			ns
Data setup time, t _{SU} (Clear Inactive) (see Figure 1)	20			20			ns
Data hold time, th (see Figure 1)	5			5	-		ns
Operating free-air temperature, TA	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	•		SN5416	4	,	SN7416	4	דומט
PARAMETER	TEST CONDITIONS	MIN	ТҮР‡	MAX	MIN	TYP‡	MAX	UNII
VIH High-level input voltage		2			2			٧
VIL Low-level input voltage				8.0			0.8	\ \
VIK Input clamp voltage	V _{CC} = MIN, I _I = -12 mA			-1.5			-1.5	V
VOH High-level output voltage	$V_{CC} = MIN$, $V_{IH} = 2 V$, $V_{IL} = 0.8 V$, $I_{OH} = -400 \mu A$	2.4	3.2		2.4	3.2		٧
VOL Low-level output voltage	$V_{CC} = MIN, V_{IH} = 2 V,$ $V_{IL} = 0.8 V, I_{OL} = 8 mA$		0.2	0.4		0.2	0.4	V
I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V,			1			1	mA
IIH High-level input current	V _{CC} = MAX, V ₁ = 2.4 V			40			40	μΑ
IL Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-1.6			-1.6	mA
IOS Short-circuit output current §	V _{CC} = MAX	-10		-27.5	-9		-27.5	mA
	V _{CC} = MAX, V _{I(clock)} = 0.4 V	Î	30			30		mA
ICC Supply current	See Note 2 V _{I(clock)} = 2.4 V		37	54		37	54]

[†] For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: ICC is measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5 V, applied to clear.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ} \text{ C}$

	PARAMETER	TEST CONDIT	IONS	MIN	TYP	MAX	UNIT
f _{max}	Maximum clock frequency		C _L = 15 pF	25	36		MHz
	Propagation delay time, high-to-low-level	i	C _L = 15 pF		24	36	ns
^t PHL	Q outputs from clear input	B 800 G	C _L = 50 pF		28	42	1
	Propagation delay time, low-to-high-level	R _L = 800 Ω,	C _{L.} = 15 pF	8	17	27	ns
+	Q outputs from clock input	See Figure 1	C _L = 50 pF	10	20	30] ""
	Propagation delay time, high-to-low-level		C _L = 15 pF	10	21	32	ns
tPHL			C _L = 50 pF	10	25	37]



[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than two outputs should be shorted at a time.

SN54LS164, SN74LS164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

absolute maximum ratings over operati	ting free-air temperature range (unless othe	rwise noted)
	SN54LS164	-55°C to 125°C
Storage temperature range	311/4L3104	
NOTE 1: Voltage values are with respect to network	k ground terminal.	

recommended operating conditions

		S	N54LS1	64	S	N74LS1	64	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	٧
ЮН	High-level output current			- 0.4			- 0.4	mΑ
lOL	Low-level output current			4			8	mA
fclock	Clock frequency	0		25	0		25	MHz
tw	Width of clock or clear input pulse	20			20			ns
t _{su}	Data setup time (See Figure 1)	15			15			ns
t _{su}	Clear inactive setup time (See Figure 1)	20			20		_	ns
th	Data hold time (See Figure 1)	5			5			ns
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

24244552	TEST CONDITIONS!	TEST CONDITIONS†				SN74LS164			UNIT
PARAMETER	TEST CONDITIONS		MIN	MIN TYP‡ MAX			TYP [‡]	MAX	UNII
VIK	$V_{CC} = MIN$, $I_I = -18 \text{ mA}$	·			- 1.5			- 1 .5	٧
V _{OH}	$V_{CC} = MIN$, $V_{IH} = 2 V$, V_{II} $I_{OH} = -0.4 \text{ mA}$	L = MAX,	2.5	3.5		2.7	3.5		٧
	$V_{CC} = MIN$, $V_{IH} = 2 V$,	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
v_{OL}	V _{IL} = MAX	I _{OL} = 8 mA					0.35	0.5]
l _l	V _{CC} = MAX, V _I = 7 V			·	0.1			0.1	mA
лн Пн	$V_{CC} = MAX$, $V_I = 2.7 V$			20			20		μΑ
ΙΙL	$V_{CC} = MAX$, $V_I = 0.4 V$				-0.4			-0.4	mA
los	V _{CC} = MAX		- 20		- 100	- 20		- 100	mA
lcc	V _{CC} = MAX, See Note 3	_		16	27		16	27	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, VCC = 5 V, TA = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
fmax	Maximum clock frequency		25	36		MHz
tPHL	Propagation delay time, high-to-low-level Q outputs from clear input	$R_L = 2 k\Omega$, $C_L = 15 pF$,		24	36	ns
tPLH	Propagation delay time, low-to-high-level Q outputs from clock input	See Figure 1		17	27	ns
tPHL	Propagation delay time, high-to-low-level Q outputs from clock input			21	32	ns



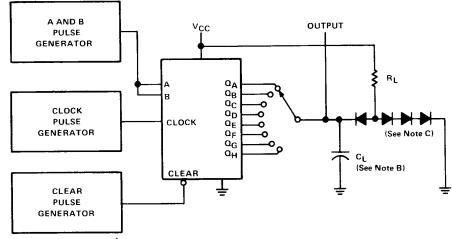
 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

⁵Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

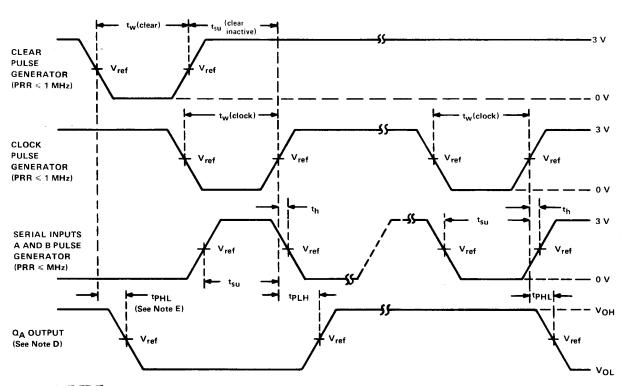
NOTE 3: I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4 V, and a momentary ground, then 4.5 V applied to clear.

SN54164, SN54LS164, SN74164, SN74LS164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. The pulse generators have the following characteristics: duty cycle \leq 50%, $Z_{out} \approx$ 50 Ω ; for '164, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns, and for LS164, $t_r \leq$ 15 ns, $t_f \leq$ 6 ns.
 - B. C_L includes probe and jig capacitance.
 - C. All diodes are 1N3064 or equivalent.
 - D. QA output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
 - E. Outputs are set to the high level prior to the measurement of tpHL from the clear input.
 - F. For '164, $V_{ref} = 1.5 \text{ V}$; for 'LS164, $V_{ref} = 1.3 \text{ V}$.

FIGURE 1-SWITCHING TIMES



23-Mar-2012

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
JM38510/00903BCA	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
JM38510/30605B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/30605B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/30605BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
JM38510/30605BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
JM38510/30605BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
JM38510/30605BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
JM38510/30605SCA	ACTIVE	CDIP	J	14	25	TBD	A42	N / A for Pkg Type	
JM38510/30605SCA	ACTIVE	CDIP	J	14	25	TBD	A42	N / A for Pkg Type	
JM38510/30605SDA	ACTIVE	CFP	W	14	25	TBD	A42	N / A for Pkg Type	
JM38510/30605SDA	ACTIVE	CFP	W	14	25	TBD	A42	N / A for Pkg Type	
M38510/30605B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/30605B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/30605BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
M38510/30605BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
M38510/30605BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
M38510/30605BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
M38510/30605SCA	ACTIVE	CDIP	J	14	25	TBD	A42	N / A for Pkg Type	
M38510/30605SCA	ACTIVE	CDIP	J	14	25	TBD	A42	N / A for Pkg Type	
M38510/30605SDA	ACTIVE	CFP	W	14	25	TBD	A42	N / A for Pkg Type	
M38510/30605SDA	ACTIVE	CFP	W	14	25	TBD	A42	N / A for Pkg Type	
SN54164J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
SN54164J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
SN54LS164J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN54LS164J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN74164N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN74164N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN74LS164D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LS164D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS164DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS164DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS164DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS164DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS164DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS164DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS164DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS164DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS164DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS164DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS164J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
SN74LS164J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
SN74LS164N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS164N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS164N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN74LS164N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN74LS164NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS164NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS164NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS164NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	





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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LS164NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS164NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS164NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS164NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54164J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
SNJ54164J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
SNJ54164W	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI	
SNJ54164W	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI	
SNJ54LS164FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS164FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS164J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SNJ54LS164J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SNJ54LS164W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
SNJ54LS164W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

23-Mar-2012

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54164, SN54LS164, SN54LS164-SP, SN74164, SN74LS164:

Catalog: SN74164, SN74LS164, SN54LS164

Military: SN54164, SN54LS164

• Space: SN54LS164-SP

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NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application



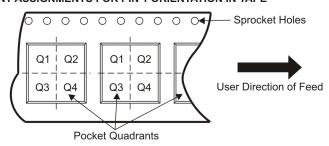
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS164DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS164NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS164DR	SOIC	D	14	2500	346.0	346.0	33.0
SN74LS164NSR	SO	NS	14	2000	346.0	346.0	33.0

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB



FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

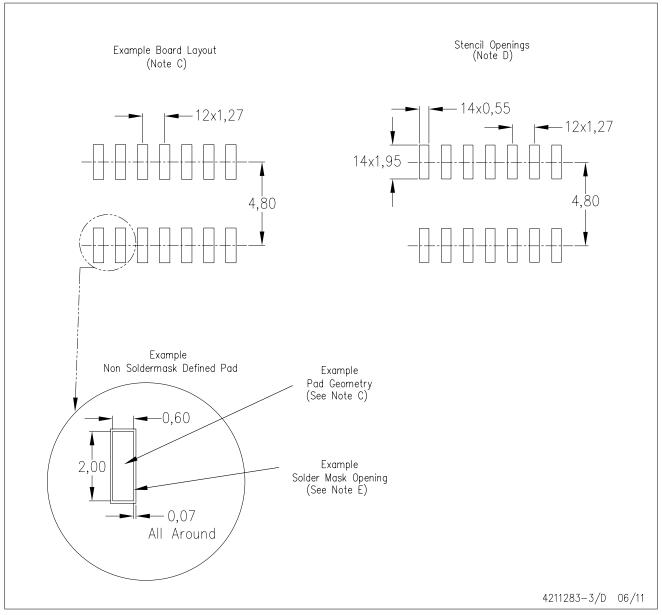


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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