

CD54HC165, CD74HC165, CD54HCT165

Data sheet acquired from Harris Semiconductor

February 1998 - Revised October 2003

High-Speed CMOS Logic 8-Bit Parallel-In/Serial-Out Shift Register

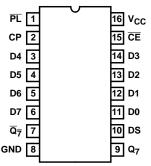
Features

- · Buffered Inputs
- Asynchronous Parallel Load
- Complementary Outputs
- Fanout (Over Temperature Range)

 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)
 - CMOS Input Compatibility, I_I \leq 1 μ A at V_{OL}, V_{OH}

Pinout

CD54HC165, CD54HCT165 (CERDIP) CD74HC165, CD74HCT165 (PDIP, SOIC) TOP VIEW



Description

The 'HC165 and 'HCT165 are 8-bit parallel or serial-in shift registers with complementary serial outputs (Q_7 and $\overline{Q_7}$) available from the last stage. When the parallel load (\overline{PL}) input is LOW, parallel data from the D0 to D7 inputs are loaded into the register asynchronously. When the \overline{PL} is HIGH, data enters the register serially at the DS input and shifts one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by typing the Q_7 output to the DS input of the succeeding device.

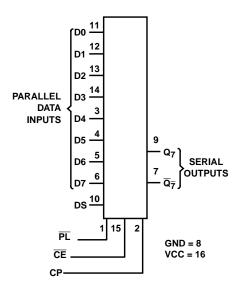
For predictable operation the LOW-to-HIGH transition of $\overline{\text{CE}}$ should only take place while CP is HIGH. Also, CP and $\overline{\text{CE}}$ should be LOW before the LOW-to-HIGH transition of PL to prevent shifting the data when $\overline{\text{PL}}$ goes HIGH.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC165F3A	-55 to 125	16 Ld CERDIP
CD54HCT165F3A	-55 to 125	16 Ld CERDIP
CD74HC165E	-55 to 125	16 Ld PDIP
CD74HC165M	-55 to 125	16 Ld SOIC
CD74HC165MT	-55 to 125	16 Ld SOIC
CD54HC165M96	-55 to 125	16 Ld SOIC
CD74HCT165E	-55 to 125	16 Ld PDIP
CD74HCT165M	-55 to 125	16 Ld SOIC
CD74HCT165MT	-55 to 125	16 Ld SOIC
CD54HCT165M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Functional Diagram



TRUTH TABLE

			INPUTS			Q _n RE	GISTER	OUTPUTS	
OPERATING MODE	PL	CE	СР	DS	D0 - D7	Q ₀	Q ₁ - Q ₆	Q ₇	\overline{Q}_7
Parallel Load	L	Х	Х	Х	L	L	L-L	L	Н
	L	Х	Х	Х	Н	Н	H-H	Н	L
Serial Shift	Н	L	1	I	Х	L	q _{0 -} q ₅	q ₆	q ₆
	Н	L	1	h	Х	Н	q _{0 -} q ₅	q ₆	q ₆
Hold Do Nothing	Н	Н	Х	Х	Х	q ₀	91 - 96	q ₇	q ₇

H =High Voltage Level

h = High Voltage Level One Set-up Time Prior To The Low-to-high Clock Transition

I = Low Voltage Level One Set-up Time Prior To The Low-to-high Clock Transition

L = Low Voltage Level

X = Don't Care

↑ = Transition from Low to High Level

 q_{n} = Lower Case Letters Indicate The State Of the Reference Output Clock Transition

Absolute Maximum Ratings

DC Supply Voltage, V $_{CC}$-0.5V to 7V DC Input Diode Current, I_{IK} For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ ± 20 mA DC Output Diode Current, I_{OK} For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$±20mA DC Drain Current per Output, IO For $V_O < -0.5 V V_O > V_{CC} + 0.5 V$±25mA DC Output Source or Sink Current per Output Pin, IO DC V_{CC} or Ground Current, I_{CC or} I_{GND}±50mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (oC/W)
E (PDIP) Package	. 67
M (SOIC) Package	
Maximum Junction Temperature	
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C
(SOIC - Lead Tips Only)	

Operating Conditions

Temperature Range (T _A)55°C to 125°C
Supply Voltage Range, V _{CC}
HC Types2V to 6V
HCT Types
DC Input or Output Voltage, V _I , V _O 0V to V _{CC}
Input Rise and Fall Time
2V
4.5V 500ns (Max)
6V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

			ST ITIONS			25°C		-40°C T	O 85°C	-55°C T	O 125 ⁰ C	
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES	HC TYPES											
High Level Input	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
Voltage				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
Voltage				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	٧
High Level Output	V _{OH}	V _{IH} or	-0.02	2	1.9	-	-	1.9	-	1.9	-	٧
Voltage CMOS Loads		V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output			-4	4.5	3.98	-	-	3.84	-	3.7	-	٧
Voltage TTL Loads			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output	V _{OL}	V _{IH} or	0.02	2	-	-	0.1	-	0.1	-	0.1	V
Voltage CMOS Loads		V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	٧
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Voltage TTL Loads			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	l _l	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μА

DC Electrical Specifications (Continued)

			ST ITIONS			25°C		-40°C T	O 85°C	-55°C T	O 125°C	
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Quiescent Device Current	Icc	V _{CC} or GND	0	6	-	-	8	-	80	-	160	μА
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	lı	V _{CC} to GND	0	5.5	-	-	±0.1	-	±1	-	±1	μА
Quiescent Device Current	Icc	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μА
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 2)	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μА

NOTE:

HCT Input Loading Table

INPUT	UNIT LOADS
DS, D0 to D7	0.35
CP, PL	0.65

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g. 360 μA max at $25^{0}C.$

Prerequisite For Switching Specifications

			25°C		-40°C TO 85°C		-55°C TO 125°C		
PARAMETER	SYMBOL	V _{CC} (V)	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES									
CP Pulse Width	t _{WL} , t _{WH}	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns

^{2.} For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

Prerequisite For Switching Specifications (Continued)

			25	o°C	-40°C 7	O 85°C	-55°C T	O 125°C	
PARAMETER	SYMBOL	V _{CC} (V)	MIN	MAX	MIN	МАХ	MIN	MAX	UNITS
PL Pulse Width	t _{WL}	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
Set-up Time	t _{SU}	2	80	-	100	-	120	-	ns
DS to CP		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
CE to CP	t _{SU(L)}	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
D0-D7 to PL	t _{SU}	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
Hold Time	t _H	2	35	-	45	-	55	-	ns
DS to CP or $\overline{\text{CE}}$		4.5	7	-	9	-	11	-	ns
		6	6	-	8	-	9	-	ns
CE to CP	t _H	2	0	-	0	-	0	-	ns
		4.5	0	-	0	-	0	-	ns
		6	0	-	0	-	0	-	ns
Recovery Time	t _{REC}	2	100	-	125	-	150	-	ns
PL to CP		4.5	20	-	25	-	30	-	ns
		6	17	-	21	-	26	-	ns
Maximum Clock Pulse	f _{MAX}	2	6	-	5	-	4	-	MHz
Frequency		4.5	30	-	24	-	20	-	MHz
		6	35	-	28	-	24	-	MHz
HCT TYPES	<u>'</u>			•			!		
CP Pulse Width	t_{WL} , t_{WH}	4.5	18	-	23	-	27	-	ns
PL Pulse Width	t _{WL}	4.5	20	-	25	-	30	-	ns
Set-up Time DS to CP	t _{SU}	4.5	20	-	25	-	30	-	ns
CE to CP	t _{SU(L)}	4.5	20	-	25	-	30	-	ns
D0-D7 to PL	t _{SU}	6	20	-	25	-	30	-	ns
Hold Time DS to CP or CE	t _H	4.5	7	-	9	-	11	-	ns
CE to CP	t _S , t _H	4.5	0	-	0	-	0	-	ns
Recovery Time PL to CP	t _{REC}	4.5	20	-	25	-	30	-	ns
Maximum Clock Pulse Frequency	f _{MAX}	4.5	27	-	22	-	18	-	MHz

Switching Specifications Input $t_{\rm f},\,t_{\rm f}=6{\rm ns}$

		TEST		25	°C	-40°C TO 85°C	-55°C TO 125°C	
PARAMETER	SYMBOL	CONDITIONS	V _{CC} (V)	TYP	MAX	MAX	MAX	UNITS
HC TYPES								
Propagation Delay	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	165	205	250	ns
CP or $\overline{\text{CE}}$ to \mathbb{Q}_7 or $\overline{\mathbb{Q}}_7$			4.5	-	33	41	50	ns
		C _L = 15pF	5	13	-	-	-	ns
		C _L = 50pF	6	-	28	35	43	ns
PL to Q ₇ or $\overline{Q}_{\overline{7}}$	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	175	220	265	ns
			4.5	-	35	44	53	ns
		C _L = 15pF	5	14	-	-	-	ns
		C _L = 50pF	6	-	30	37	45	ns
D7 to Q_7 or $\overline{Q}_{\overline{7}}$	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	150	190	225	ns
			4.5	-	30	38	45	ns
		C _L = 15pF	5	12	-	-	-	ns
		C _L = 50pF	6	-	26	33	38	ns
Output Transition Times	t _{TLH} , t _{THL}	C _L = 50pF	2	-	75	95	110	ns
			4.5	-	15	19	22	ns
			6	-	13	16	19	ns
Input Capacitance	C _{IN}	-	-	-	10	10	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C _{PD}	-	5	17	-	-	-	pF
HCT TYPES		<u> </u>	l .			<u> </u>		
Propagation Delay	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	40	50	60	ns
CP or $\overline{\text{CE}}$ to Q_7 or $\overline{Q}_{\overline{7}}$		C _L = 15pF	5	17	-	-	-	ns
PL to Q ₇ or $\overline{Q}_{\overline{7}}$	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	40	50	60	ns
		C _L = 15pF	5	17	-	-	-	ns
D7 to Q_7 or $\overline{Q}_{\overline{7}}$	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	35	44	53	ns
		C _L = 15pF	5	14	-	-	-	ns
Output Transition Times	t _{TLH} , t _{THL}	C _L = 50pF	4.5	-	15	19	22	ns
Input Capacitance	C _{IN}	C _L = 50pF	-	-	10	10	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C _{PD}	-	5	24		-	-	pF

- 3. $\ensuremath{\text{C}_{\text{PD}}}$ is used to determine the dynamic power consumption, per package.
- 4. P_D = V_{CC}² f_i + Σ (C_L V_{CC}² + f_O) where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

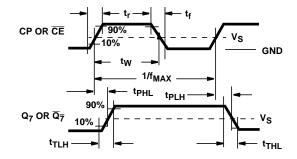


FIGURE 3. SERIAL-SHIFT MODE

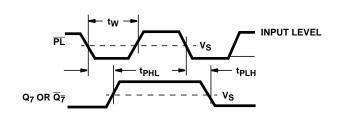


FIGURE 4. PARALLEL-LOAD MODE

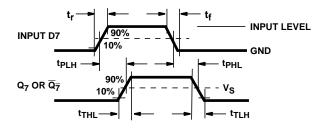


FIGURE 5. PARALLEL-LOAD MODE

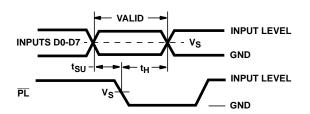


FIGURE 6. PARALLEL-LOAD MODE

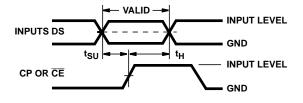


FIGURE 7. SERIAL-SHIFT MODE

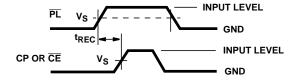


FIGURE 8. SERIAL-SHIFT MODE

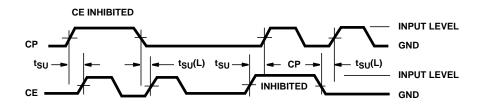


FIGURE 9. SERIAL-SHIFT, CLOCK-INHIBIT MODE



5-Sep-2011

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-8685501EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
CD54HC165F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD54HCT165F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD74HC165E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC165EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC165M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC165M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC165M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC165M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC165ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC165MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC165MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC165MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC165MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT165E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT165EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT165M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT165M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT165M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT165M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	





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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CD74HCT165ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT165MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT165MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT165MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT165MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF CD54HC165, CD54HCT165, CD74HC165, CD74HCT165:





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● Catalog: CD74HC165, CD74HCT165

• Military: CD54HC165, CD54HCT165

NOTE: Qualified Version Definitions:

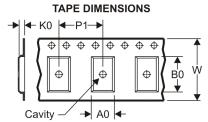
- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





Α0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC165M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
CD74HC165M96	SOIC	D	16	2500	346.0	346.0	33.0	

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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