SBAS246A – DECEMBER 2001 – MAY 2003

Dual Channel, Low Power, 16-Bit, Serial Input DIGITAL-TO-ANALOG CONVERTER

FEATURES

- ***micro*POWER OPERATION: 500μA at 5V**
- **POWER-ON RESET TO ZERO-SCALE**
- **POWER SUPPLY: +2.7V to +5.5V**
- **16-BIT MONOTONIC OVER TEMPERATURE**
- **SETTLING TIME: 10μs to ±0.003% FSR**
- **ULTRA-LOW AC CROSSTALK: –100dB typ**
- **LOW-POWER SERIAL INTERFACE WITH SCHMITT-TRIGGERED INPUTS**
- **ON-CHIP OUTPUT BUFFER AMPLIFIER WITH RAIL-TO-RAIL OPERATION**
- **DOUBLE BUFFERED INPUT ARCHITECTURE**
- **SIMULTANEOUS OR SEQUENTIAL OUTPUT UPDATE AND POWERDOWN**
- **TINY MSOP-8 PACKAGE**

APPLICATIONS

- **PORTABLE INSTRUMENTATION**
- **CLOSED-LOOP SERVO-CONTROL**
- **PROCESS CONTROL**
- **DATA ACQUISITION SYSTEMS**
- **PROGRAMMABLE ATTENUATION**
- **PC PERIPHERALS**

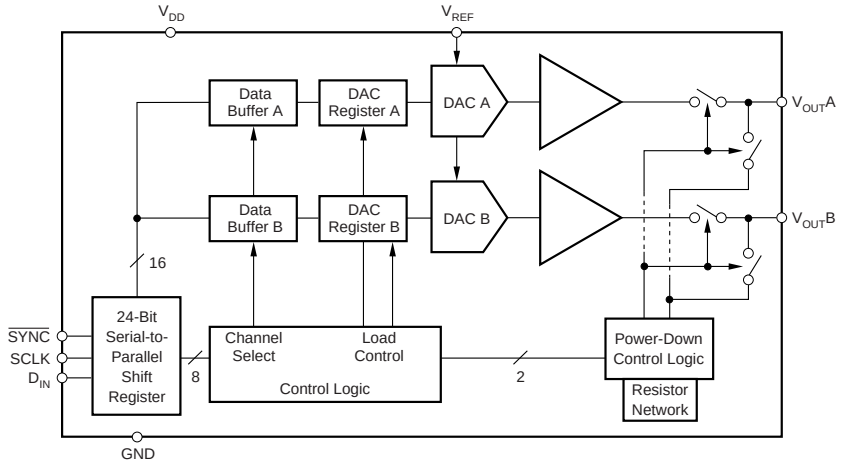
DESCRIPTION

The DAC8532 is a dual channel, 16-bit Digital-to-Analog Converter (DAC) offering low power operation and a flexible serial host interface. Each on-chip precision output amplifier allows rail-to-rail output swing to be achieved over the supply range of 2.7V to 5.5V. The device supports a standard 3-wire serial interface capable of operating with input data clock frequencies up to 30MHz for V_{DD} = 5V.

The DAC8532 requires an external reference voltage to set the output range of each DAC channel. Also incorporated into the device is a power-on reset circuit which ensures that the DAC outputs power up at zero-scale and remain there until a valid write takes place. The DAC8532 provides a flexible power-down feature, accessed over the serial interface, that reduces the current consumption of the device to 200nA at 5V.

The low-power consumption of this device in normal operation makes it ideally suited to portable battery-operated equipment and other low-power applications. The power consumption is 2.5mW at 5V, reducing to 1μW in power-down mode.

The DAC8532 is available in a MSOP-8 package with a specified operating temperature range of –40°C to +105°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS(1)

V_{DD} to GND	–0.3V to +6V
Digital Input Voltage to GND	–0.3V to $+V_{DD}$ + 0.3V
V_{OUTA} or V_{OUTB} to GND	–0.3V to $+V_{DD}$ + 0.3V
Operating Temperature Range	–40°C to +105°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature Range (T_J max)	+150°C
Power Dissipation	(T_J max — T_A)/θ_{JA}
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
Lead Temperature, Soldering:	
Vapor Phase (60s)	+215°C
Infrared (15s)	+220°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFICATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8532	MSOP-8	DGK	–40°C to +105°C	D32E	DAC8532IDGK	Tube, 80
	"	"	"	"	DAC8532IDGKR	Tape and Reel, 2500

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

V_{DD} = +2.7V to +5.5V. –40°C to +105°C, unless otherwise specified.

PARAMETER	CONDITIONS	DAC8532 MIN	DAC8532 TYP	DAC8532 MAX	UNITS
STATIC PERFORMANCE(1)					
Resolution		16			Bits
Relative Accuracy				±0.0987	% of FSR
Differential Nonlinearity	16-Bit Monotonic			±1	LSB
Zero-Scale Error			+5	+25	mV
Full-Scale Error			–0.15	–1.0	% of FSR
Gain Error				±1.0	% of FSR
Zero-Scale Error Drift			±20		µV/°C
Gain Temperature Coefficient			±5		ppm of FSR/°C
Channel-to-Channel Matching	R_L = 2kΩ, C_L = 200pF		15		mV
PSRR			0.75		mV/V
OUTPUT CHARACTERISTICS(2)					
Output Voltage Range		0		V_{REF}	V
Output Voltage Settling Time	To ±0.003% FSR				
	0200_H to $FD00_H$		8	10	µs
	R_L = 2kΩ; 0pF < C_L < 200pF				
	R_L = 2kΩ; C_L = 500pF		12		µs
Slew Rate			1		V/µs
Capacitive Load Stability	R_L = ∞		470		pF
	R_L = 2kΩ		1000		pF
Code Change Glitch Impulse	1LSB Change Around Major Carry		20		nV-s
Digital Feedthrough			0.5		nV-s
DC Crosstalk			0.25		LSB
AC Crosstalk			–100	–96	dB
DC Output Impedance			1		Ω
Short-Circuit Current	V_{DD} = +5V		50		mA
	V_{DD} = +3V		20		mA
Power-Up Time	Coming Out of Power-Down Mode				
	V_{DD} = +5V		2.5		µs
	Coming Out of Power-Down Mode				
	V_{DD} = +3V		5		µs
AC PERFORMANCE	BW = 20kHz, V_{DD} = 5V				
	F_{OUT} = 1kHz, 1st 19 Harmonics Removed				
SNR			94		dB
THD			67		dB
SFDR			69		dB
SINAD			65		dB

ELECTRICAL CHARACTERISTICS (Cont.)

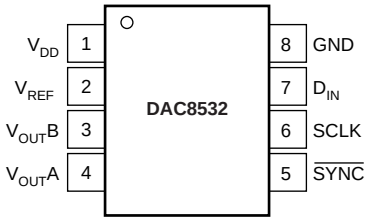
V_{DD} = +2.7V to +5.5V. –40°C to +105°C, unless otherwise specified.

PARAMETER	CONDITIONS	DAC8532 MIN	DAC8532 TYP	DAC8532 MAX	UNITS
REFERENCE INPUT					
Reference Current	$V_{REF} = V_{DD} = +5V$		67	90	µA
	$V_{REF} = V_{DD} = +3V$		40	54	µA
Reference Input Range		0		V_{DD}	V
Reference Input Impedance			75		kΩ
LOGIC INPUTS (2)					
Input Current				±1	µA
$V_{IN}L$, Input LOW Voltage	V_{DD} = +5V			0.8	V
$V_{IN}L$, Input LOW Voltage	V_{DD} = +3V			0.6	V
$V_{IN}H$, Input HIGH Voltage	V_{DD} = +5V	2.4			V
$V_{IN}H$, Input HIGH Voltage	V_{DD} = +3V	2.1			V
Pin Capacitance				3	pF
POWER REQUIREMENTS					
V_{DD}		2.7		5.5	V
I_{DD} (normal mode)	DAC Active and Excluding Load Current				
V_{DD} = +3.6V to +5.5V	$V_{IH} = V_{DD}$ and V_{IL} = GND		500	800	µA
V_{DD} = +2.7V to +3.6V	$V_{IH} = V_{DD}$ and V_{IL} = GND		450	750	µA
I_{DD} (all power-down modes)					
V_{DD} = +3.6V to +5.5V	$V_{IH} = V_{DD}$ and V_{IL} = GND		0.2	1	µA
V_{DD} = +2.7V to +3.6V	$V_{IH} = V_{DD}$ and V_{IL} = GND		0.05	1	µA
POWER EFFICIENCY					
I_{OUT}/I_{DD}	I_{LOAD} = 2mA, V_{DD} = +5V		89		%
TEMPERATURE RANGE					
Specified Performance		–40		+105	°C

NOTES: (1) Linearity calculated using a reduced code range of 485 to 64714; output unloaded. (2) Ensured by design and characterization, not production tested.

PIN CONFIGURATION

Top View **MSOP-8**



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	V_{DD}	Power supply input, +2.7V to +5.5V.
2	V_{REF}	Reference voltage input.
3	$V_{OUT}B$	Analog output voltage from DAC B.
4	$V_{OUT}A$	Analog output voltage from DAC A.
5	$\overline{SYNC}$	Level triggered $\overline{SYNC}$ input (active LOW). This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes LOW, it enables the input shift register and data is transferred on the falling edge of SCLK. The action specified by the 8-bit control byte and 16-bit data word is executed following the 24th falling SCLK clock edge (unless $\overline{SYNC}$ is taken HIGH before this edge in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC8532).
6	SCLK	Serial Clock Input. Data can be transferred at rates up to 30 MHz at 5V.
7	D_{IN}	Serial Data Input. Data is clocked into the 24-bit input shift register on each falling edge of the serial clock input.
8	GND	Ground reference point for all circuitry on the part.

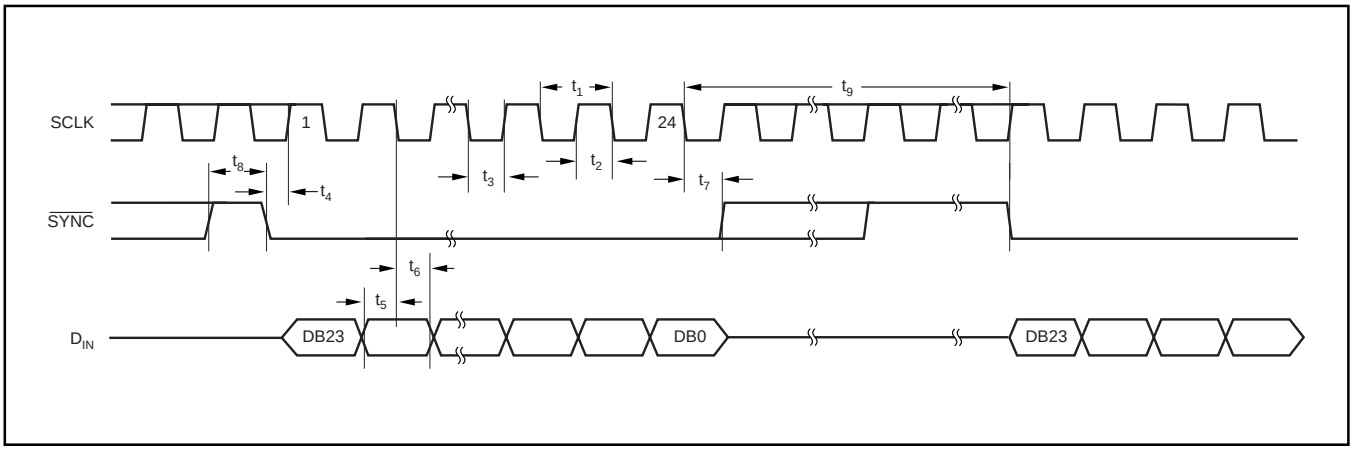
TIMING CHARACTERISTICS[1, 2]

V_{DD} = +2.7V to +5.5V; all specifications –40°C to +105°C unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	DAC8532			UNITS
			MIN	TYP	MAX	
t_1[3]	SCLK Cycle Time					
		V_{DD} = 2.7V to 3.6V	50			ns
		V_{DD} = 3.6V to 5.5V	33			ns
t_2	SCLK HIGH Time					
		V_{DD} = 2.7V to 3.6V	13			ns
		V_{DD} = 3.6V to 5.5V	13			ns
t_3	SCLK LOW Time					
		V_{DD} = 2.7V to 3.6V	22.5			ns
		V_{DD} = 3.6V to 5.5V	13			ns
t_4	$\overline{SYNC}$ to SCLK Rising Edge Setup Time					
		V_{DD} = 2.7V to 3.6V	0			ns
		V_{DD} = 3.6V to 5.5V	0			ns
t_5	Data Setup Time					
		V_{DD} = 2.7V to 3.6V	5			ns
		V_{DD} = 3.6V to 5.5V	5			ns
t_6	Data Hold Time					
		V_{DD} = 2.7V to 3.6V	4.5			ns
		V_{DD} = 3.6V to 5.5V	4.5			ns
t_7	24th SCLK Falling Edge to $\overline{SYNC}$ Rising Edge					
		V_{DD} = 2.7V to 3.6V	0			ns
		V_{DD} = 3.6V to 5.5V	0			ns
t_8	Minimum $\overline{SYNC}$ HIGH Time					
		V_{DD} = 2.7V to 3.6V	50			ns
		V_{DD} = 3.6V to 5.5V	33			ns
t_9	24th SCLK Falling Edge to $\overline{SYNC}$ Falling Edge	V_{DD} = 2.7V to 5.5V	100			ns

NOTES: (1) All input signals are specified with $t_R = t_F$ = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. (2) See Serial Write Operation timing diagram, below. (3) Maximum SCLK frequency is 30MHz at V_{DD} = +3.6V to +5.5V and 20MHz at V_{DD} = +2.7V to +3.6V.

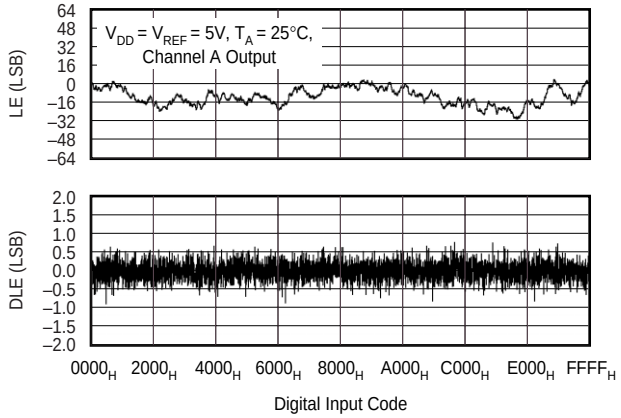
SERIAL WRITE OPERATION



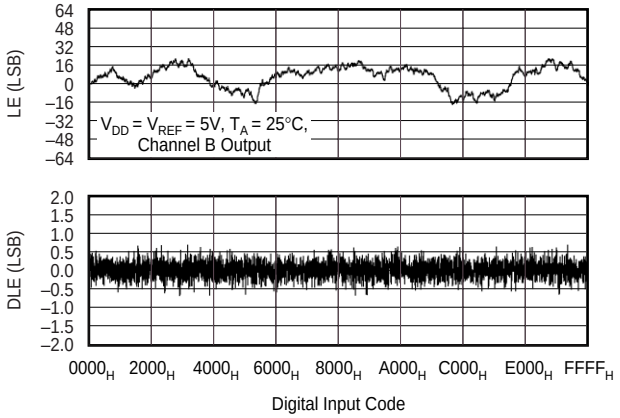
TYPICAL CHARACTERISTICS

At T_A = +25°C, unless otherwise noted.

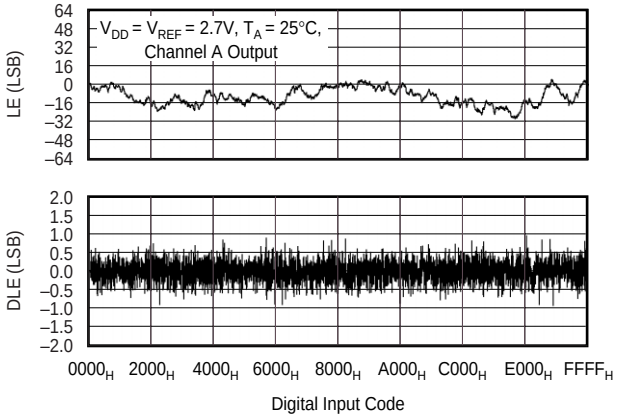
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE



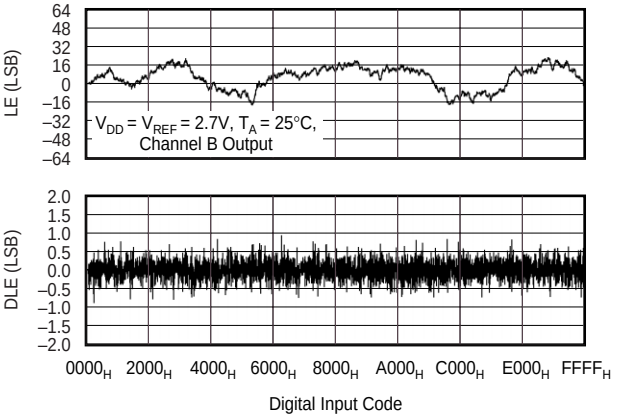
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE



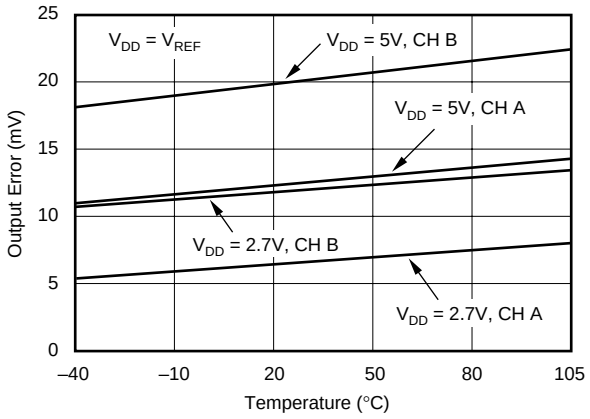
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE



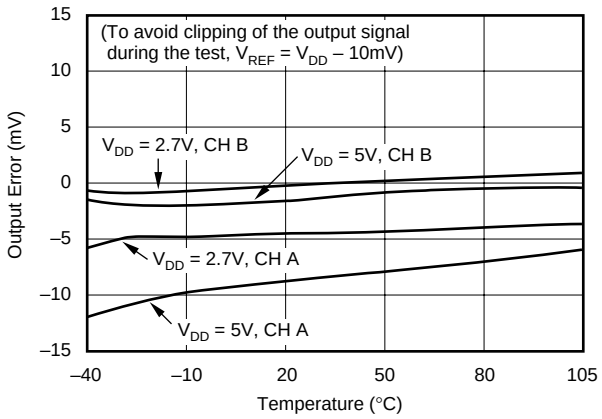
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE



ZERO-SCALE ERROR vs TEMPERATURE



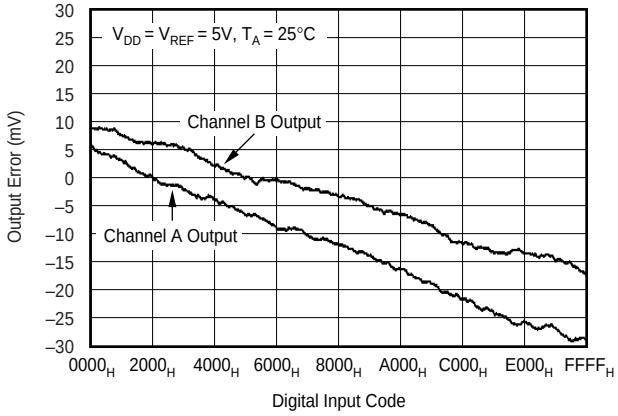
FULL-SCALE ERROR vs TEMPERATURE



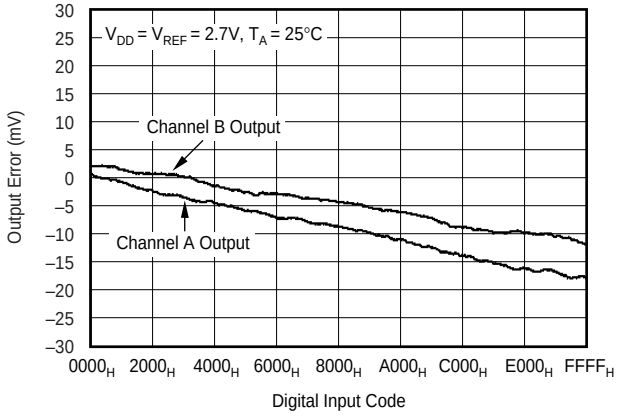
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, unless otherwise noted.

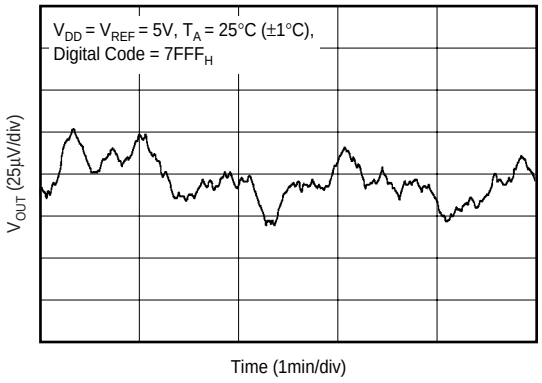
ABSOLUTE ERROR



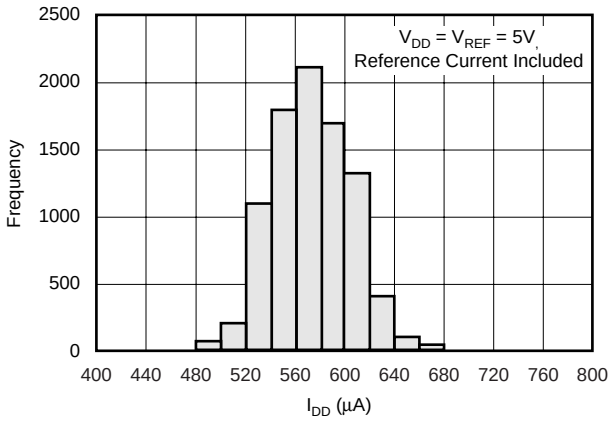
ABSOLUTE ERROR



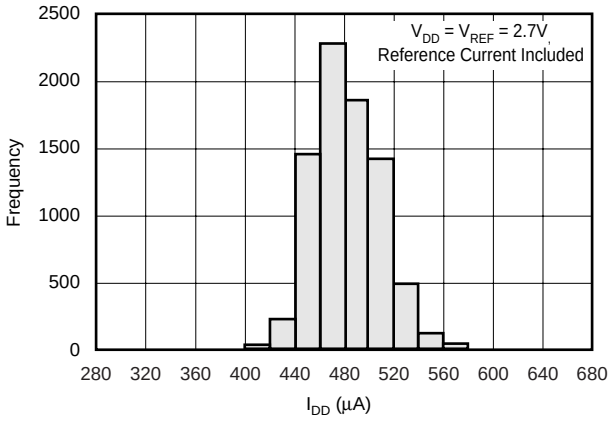
OUTPUT VOLTAGE DRIFT



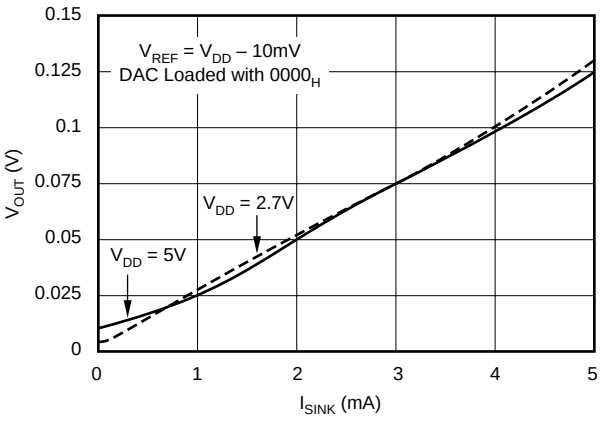
HISTOGRAM OF CURRENT CONSUMPTION



HISTOGRAM OF CURRENT CONSUMPTION



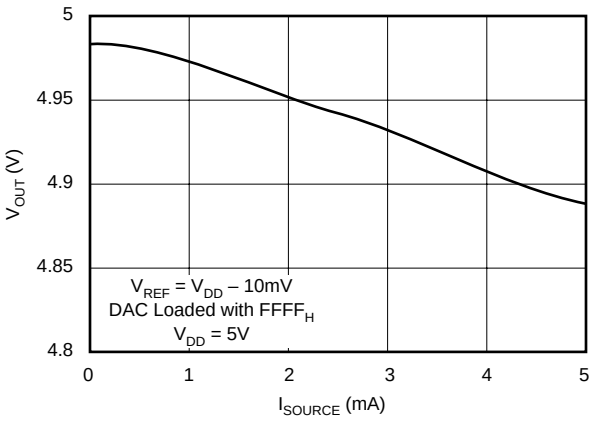
SINK CURRENT CAPABILITY



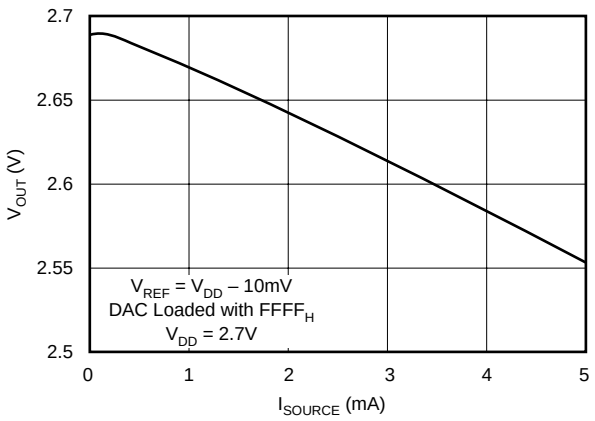
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, unless otherwise noted.

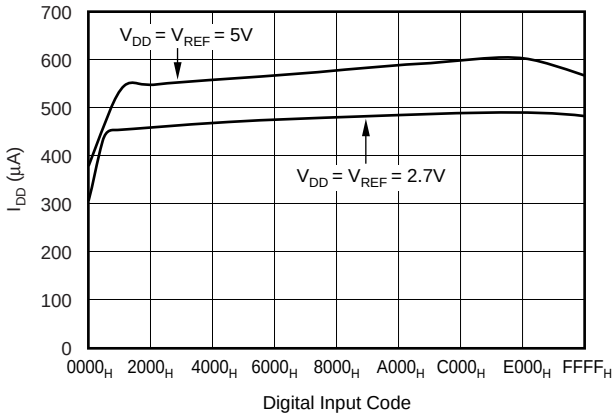
SOURCE CURRENT CAPABILITY



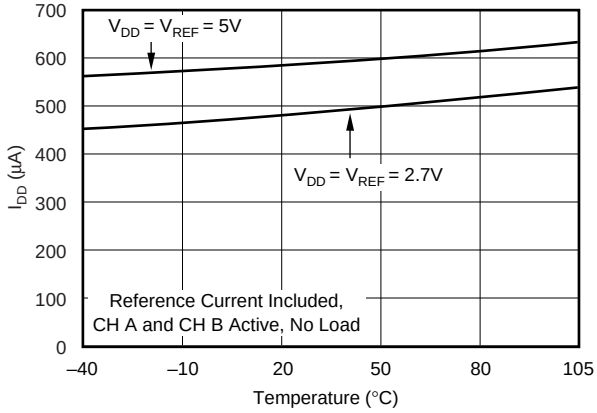
SOURCE CURRENT CAPABILITY



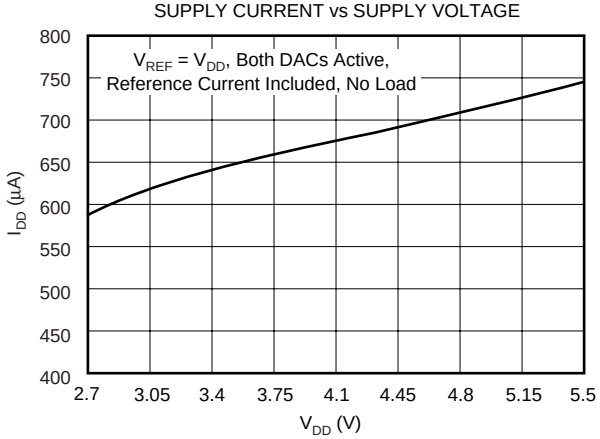
SUPPLY CURRENT vs DIGITAL INPUT CODE



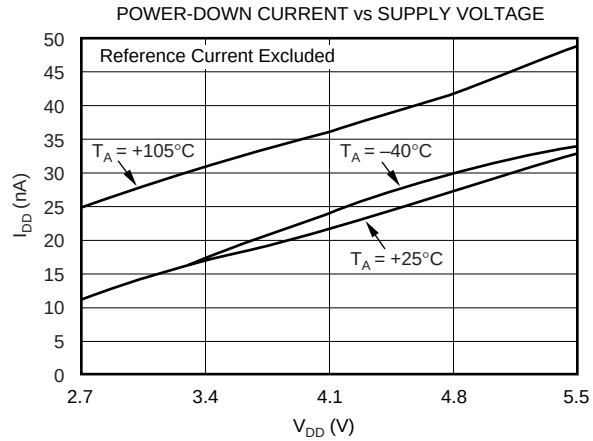
SUPPLY CURRENT vs TEMPERATURE



SUPPLY CURRENT vs SUPPLY VOLTAGE



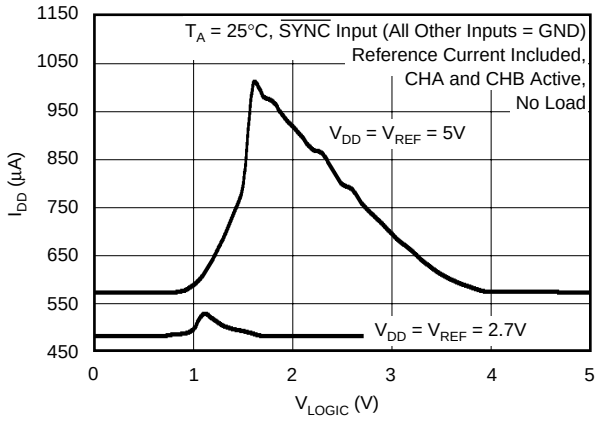
POWER-DOWN CURRENT vs SUPPLY VOLTAGE



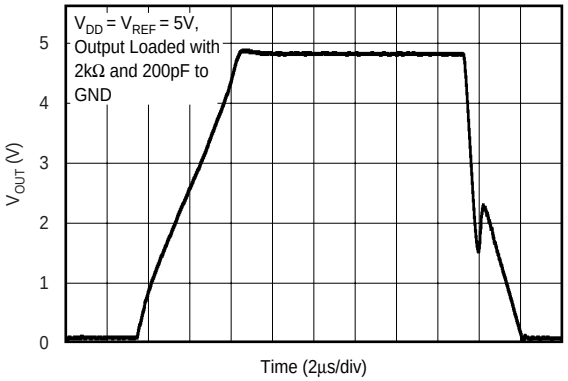
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, unless otherwise noted.

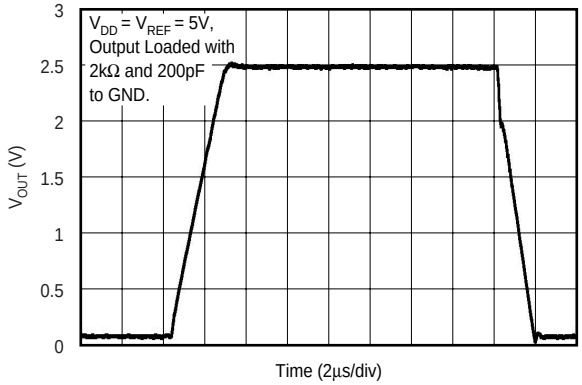
SUPPLY CURRENT vs LOGIC INPUT VOLTAGE



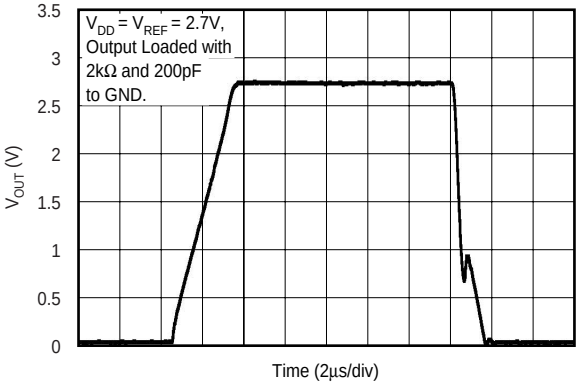
FULL-SCALE SETTLING TIME
(Large Signal)



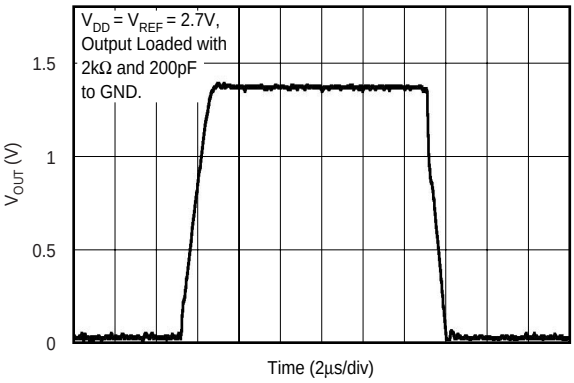
HALF-SCALE SETTLING TIME
(Large Signal)



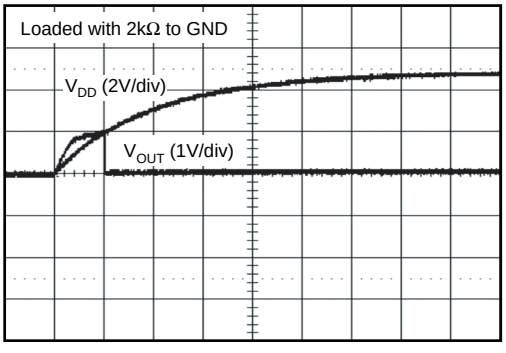
FULL-SCALE SETTLING TIME
(Large Signal)



HALF-SCALE SETTLING TIME
(Large Signal)



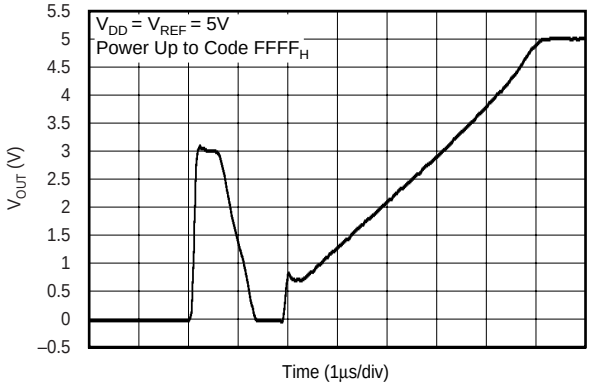
POWER-ON RESET TO ZERO-SCALE



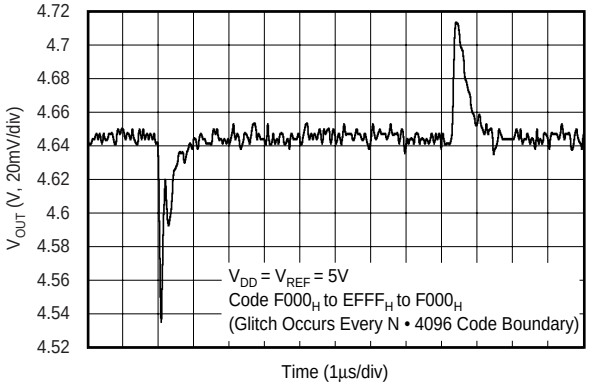
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, unless otherwise noted.

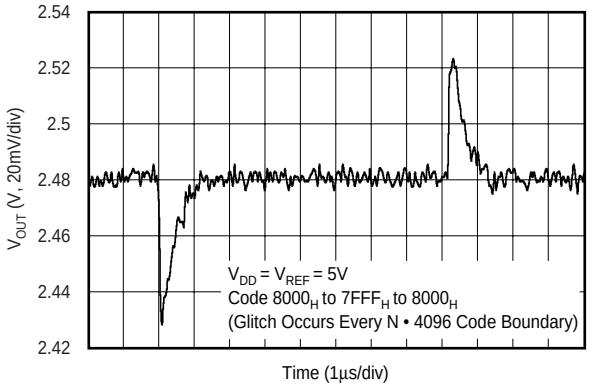
EXITING POWER-DOWN MODE



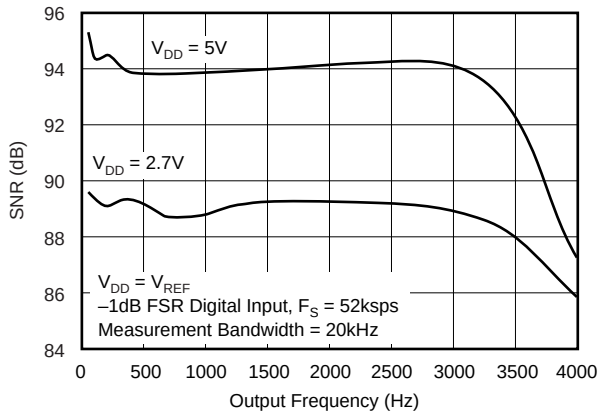
OUTPUT GLITCH
(Worst Case)



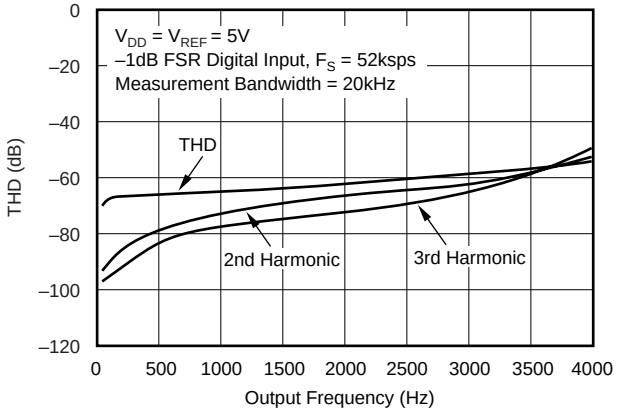
OUTPUT GLITCH
(Mid-Scale)



SIGNAL-TO-NOISE RATIO vs OUTPUT FREQUENCY



TOTAL HARMONIC DISTORTION
vs OUTPUT FREQUENCY



THEORY OF OPERATION

DAC SECTION

The architecture of each channel of the DAC8532 consists of a resistor string DAC followed by an output buffer amplifier. Figure 1 shows a simplified block diagram of the DAC architecture.

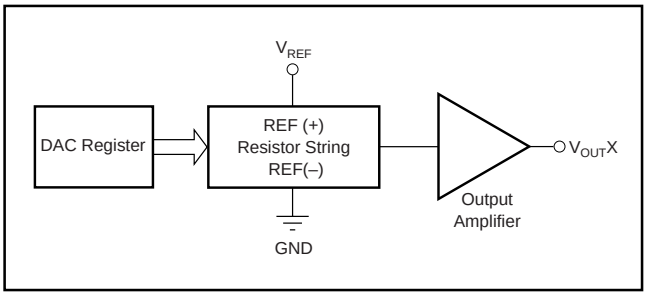


FIGURE 1. DAC8532 Architecture.

The input coding for each device is unipolar straight binary, so the ideal output voltage is given by:

$$V_{OUT}X = V_{REF} \bullet \frac{D}{65536}$$

where D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65535. $V_{OUT}X$ refers to channel A or B.

RESISTOR STRING

The resistor string section is shown in Figure 2. It is simply a divide-by-2 resistor followed by a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off. This voltage is then applied to the output amplifier by closing one of the switches connecting the string to the amplifier.

OUTPUT AMPLIFIER

Each output buffer amplifier is capable of generating rail-to-rail voltages on its output which approaches an output range of 0V to V_{DD} (gain and offset errors must be taken into account). Each buffer is capable of driving a load of 2kΩ in parallel with 1000pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical characteristics.

SERIAL INTERFACE

The DAC8532 uses a 3-wire serial interface ($\overline{SYNC}$, SCLK, and D_{IN}), which is compatible with SPI™, QSPI™, and Microwire™ interface standards, as well as most DSPs. See the Serial Write Operation timing diagram for an example of a typical write sequence.

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Microwire is a registered trademark of National Semiconductor.

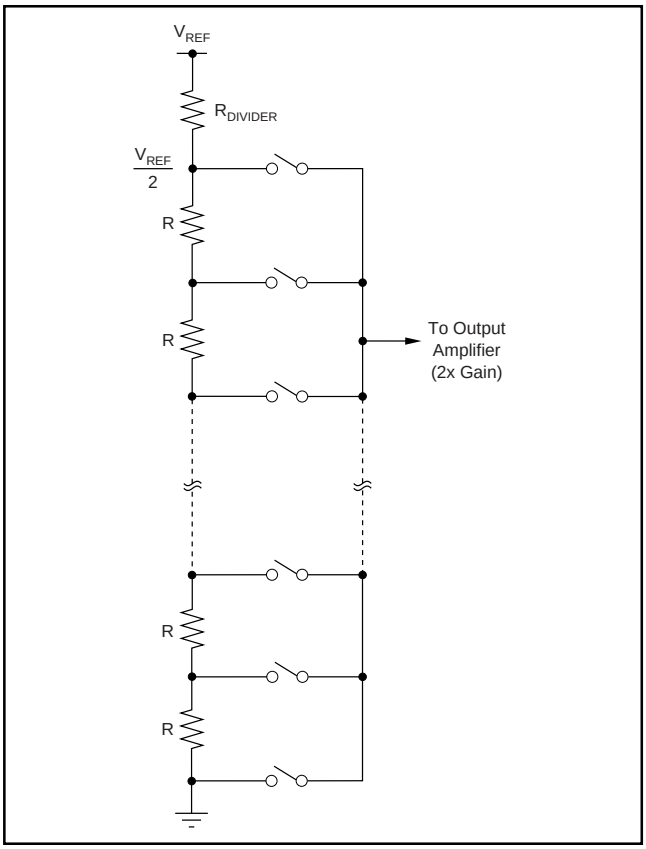


FIGURE 2. Resistor String.

The write sequence begins by bringing the $\overline{SYNC}$ line LOW. Data from the D_{IN} line is clocked into the 24-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 30MHz, making the DAC8532 compatible with high speed DSPs. On the 24th falling edge of the serial clock, the last data bit is clocked into the shift register and the programmed function is executed (i.e., a change in Data Buffer contents, DAC Register contents, and/or a change in the power-down mode of a specified channel or channels).

At this point, the $\overline{SYNC}$ line may be kept LOW or brought HIGH. In either case, the minimum delay time from the 24th falling SCLK edge to the next falling $\overline{SYNC}$ edge must be met in order to properly begin the next cycle. To assure the lowest power consumption of the device, care should be taken that the digital input levels are as close to each rail as possible. (Please refer to the “Typical Characteristics” section for the “Supply Current vs Logic Input Voltage” transfer characteristic curve).

INPUT SHIFT REGISTER

The input shift register of the DAC8532 is 24 bits wide (see Figure 5) and is made up of 8 control bits (DB16-DB23) and 16 data bits (DB0-DB15). The first two control bits (DB22 and DB23) are reserved and must be “0” for proper operation. LD A (DB20) and LD B (DB21) control the updating of each analog output with the specified 16-bit data value or power-down command. Bit DB19 is a “Don't Care” bit which does not affect the operation of the DAC8532 and can be 1 or 0. The following control bit, Buffer Select (DB18), controls the destination of the data (or power-down command) between DAC A and DAC B. The final two control bits, PD0 (DB16) and PD1 (DB17), select the power-down mode of one or both of the DAC channels. The four modes are normal mode or any one of three power-down modes. A more complete description of the operational modes of the DAC8532 can be found in the Power-Down Modes section. The remaining sixteen bits of the 24-bit input word make up the data bits. These are transferred to the specified Data Buffer or DAC Register, depending on the command issued by the control byte, on the 24th falling edge of SCLK. Please refer to Tables II and III for more information.

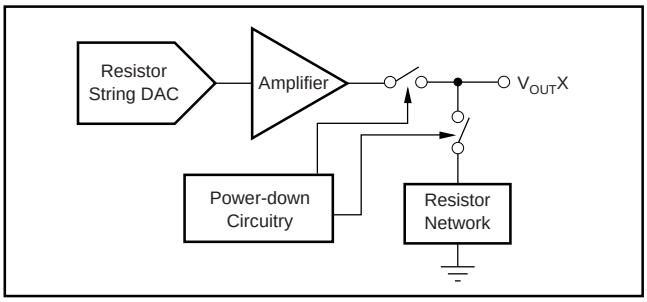


FIGURE 3. Output Stage During Power-Down (High-Impedance)

$\overline{\text{SYNC}}$ INTERRUPT

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept LOW for at least 24 falling edges of SCLK and the addressed DAC register is updated on the 24th falling edge. However, if $\overline{\text{SYNC}}$ is brought HIGH before the 24th falling edge, it acts as an interrupt to the write sequence; the shift register is reset and the write sequence is discarded. Neither an update of the data buffer contents, DAC register contents or a change in the operating mode occurs (see Figure 4).

POWER-ON RESET

The DAC8532 contains a power-on reset circuit that controls the output voltage during power-up. On power-up, the DAC registers are filled with zeros and the output voltages are set to zero-scale; they remain there until a valid write sequence and load command is made to the respective DAC channel. This is useful in applications where it is important to know the state of the output of each DAC output while the device is in the process of powering up.

No device pin should be brought high before power is applied to the device.

POWER-DOWN MODES

The DAC8532 utilizes four modes of operation. These modes are accessed by setting two bits (PD1 and PD0) in the control register and performing a “Load” action to one or both DACs. Table I shows how the state of the bits correspond to the mode of operation of each channel of the device. (Each DAC channel can be powered down simultaneously or independently of each other. Power-down occurs after proper data is written into PD0 and PD1 and a “Load” command occurs.) Please refer to the "Operation Examples" section for additional information.

PD1 (DB17)	PD0 (DB16)	OPERATING MODE
0	0	Normal Operation
—	—	Power-Down Modes
0	1	Output Typically 1kΩ to GND
1	0	Output Typically 100kΩ to GND
1	1	High Impedance

TABLE I. Modes of Operation for the DAC8532.

When both bits are set to 0, the device works normally with a typical power consumption of 500μA at 5V. For the three power-down modes, however, the supply current falls to 200nA at 5V (50nA at 3V). Not only does the supply current fall but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the device is known while it is in power-down mode. There are three different options for power-down: The output is connected internally to GND through a 1kΩ resistor, a 100kΩ resistor, or it is left open-circuited (High-Impedance). The output stage is illustrated in Figure 3.

All analog circuitry is shut down when the power-down mode is activated. Each DAC will exit power-down when PD0 and PD1 are set to 0, new data is written to the Data Buffer, and the DAC channel receives a “Load” command. The time to exit power-down is typically 2.5μs for V_{DD} = 5V and 5μs for V_{DD} = 3V (See the Typical Characteristics).

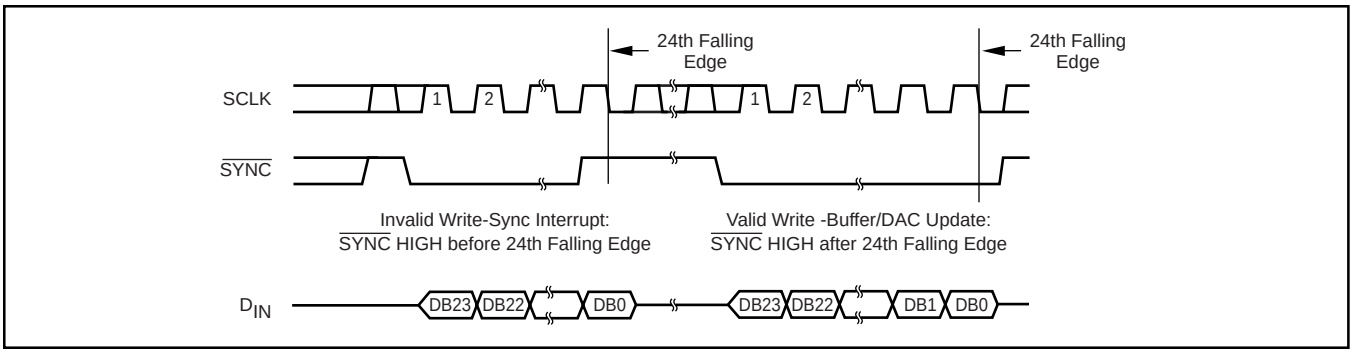


FIGURE 4. Interrupt and Valid $\overline{\text{SYNC}}$ Timing.

DB23											DB12
0	0	LDB	LDA	X	Buffer Select	PD1	PD0	D15	D14	D13	D12
DB11											**DB0**
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

FIGURE 5. DAC8532 Data Input Register Format.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13-D0	DESCRIPTION
Reserved	Reserved	Load B	Load A	Don't Care	Buffer Select	PD1	PD0	MSB	MSB-1	MSB-2...LSB	
(Always Write 0)					0 = A, 1 = B						
0	0	0	0	X	#	0	0	Data			WR Buffer # w/Data
0	0	0	0	X	#	(see Table III)		X			WR Buffer # w/Power-Down Command
0	0	0	1	X	#	0	0	Data			WR Buffer # w/Data and Load DAC A
0	0	0	1	X	0	(see Table III)		X			WR Buffer A w/Power-Down Command and LOAD DAC A (DAC A Powered Down)
0	0	0	1	X	1	(see Table III)		X			WR Buffer B w/Power-Down Command and LOAD DAC A
0	0	1	0	X	#	0	0	Data			WR Buffer # w/Data and Load DAC B
0	0	1	0	X	0	(see Table III)		X			WR Buffer A w/Power-Down Command and LOAD DAC B
0	0	1	0	X	1	(see Table III)		X			WR Buffer B w/ Power-Down Command and LOAD DAC B (DAC B Powered Down)
0	0	1	1	X	#	0	0	Data			WR Buffer # w/Data and Load DACs A and B
0	0	1	1	X	0	(see Table III)		X			WR Buffer A w/Power-Down Command and Load DACs A and B (DAC A Powered Down)
0	0	1	1	X	1	(see Table III)		X			WR Buffer B w/Power-Down Command and Load DACs A and B (DAC B Powered Down)

TABLE II. Control Matrix.

D17	D16	OUTPUT IMPEDANCE POWERDOWN COMMANDS
PD1	PD0	
0	1	1kΩ
1	0	100kΩ
1	1	High Impedance

TABLE III. Power-Down Commands.

OPERATION EXAMPLES

Example 1: Write to Data Buffer A; Write to Data Buffer B; Load DACA and DACB Simultaneously

- 1st—Write to Data Buffer A:

Reserved	Reserved	LDB	LDA	DC	Buffer Select	PD1	PD0	DB15	.....	DB1	DB0
0	0	0	0	X	0	0	0	D15	.....	D1	D0

- 2nd—Write to Data Buffer B and Load DAC A and DAC B simultaneously:

Reserved	Reserved	LDB	LDA	DC	Buffer Select	PD1	PD0	DB15	.....	DB1	DB0
0	0	1	1	X	1	0	0	D15	.....	D1	D0

The DACA and DACB analog outputs simultaneously settle to the specified values upon completion of the 2nd write sequence. (The "Load" command moves the digital data from the data buffer to the DAC register at which time the conversion takes place and the analog output is updated. "Completion" occurs on the 24th falling SCLK edge after $\overline{\text{SYNC}}$ LOW.)

Example 2: Load New Data to DACA and DACB Sequentially

- 1st—Write to Data Buffer A and Load DAC A: DACA output settles to specified value on completion:

Reserved	Reserved	LDB	LDA	DC	Buffer Select	PD1	PD0	DB15	.....	DB1	DB0
0	0	0	1	X	0	0	0	D15	.....	D1	D0

- 2nd—Write to Data Buffer B and Load DAC B: DACB output settles to specified value on completion:

Reserved	Reserved	LDB	LDA	DC	Buffer Select	PD1	PD0	DB15	.....	DB1	DB0
0	0	1	0	X	1	0	0	D15	.....	D1	D0

After completion of the 1st write cycle, the DACA analog output settles to the voltage specified; upon completion of write cycle 2, the DACB analog output settles.

Example 3: Power-Down DACA to 1kΩ and Power-Down DACB to 100kΩ Simultaneously

- 1st—Write power-down command to Data Buffer A:

Reserved	Reserved	LDB	LDA	DC	Buffer Select	PD1	PD0	DB15	.....	DB1	DB0
0	0	0	0	X	0	0	1	Don't Care			

- 2nd—Write power-down command to Data Buffer B and Load DACA and DACB simultaneously:

Reserved	Reserved	LDB	LDA	DC	Buffer Select	PD1	PD0	DB15	.....	DB1	DB0
0	0	1	1	X	1	1	0	Don't Care			

The DACA and DACB analog outputs simultaneously power-down to each respective specified mode upon completion of the 2nd write sequence.

Example 4: Power-Down DACA and DACB to High Impedance Sequentially:

- 1st—Write power-down command to Data Buffer A and Load DAC A: DAC A output = High-Z:

Reserved	Reserved	LDB	LDA	DC	Buffer Select	PD1	PD0	DB15	.....	DB1	DB0
0	0	0	1	X	0	1	1	Don't Care			

- 2nd—Write power-down command to Data Buffer B and Load DAC B: DAC B output = High-Z:

Reserved	Reserved	LDB	LDA	DC	Buffer Select	PD1	PD0	DB15	.....	DB1	DB0
0	0	1	0	X	1	1	1	Don't Care			

The DACA and DACB analog outputs sequentially power-down to high impedance upon completion of the 1st and 2nd write sequences, respectively.

MICROPROCESSOR INTERFACING

DAC8532 to 8051 INTERFACE

Figure 6 shows a serial interface between the DAC8532 and a typical 8051-type microcontroller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DAC8532, while RXD drives the serial data line of the device. The $\overline{SYNC}$ signal is derived from a bit-programmable pin on the port of the 8051. In this case, port line P3.3 is used. When data is to be transmitted to the DAC8532, P3.3 is taken LOW. The 8051 transmits data in 8-bit bytes; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left LOW after the first eight bits are transmitted, then a second and third write cycle is initiated to transmit the remaining data. P3.3 is taken HIGH following the completion of the third write cycle. The 8051 outputs the serial data in a format which presents the LSB first, while the DAC8532 requires its data with the MSB as the first bit received. The 8051 transmit routine must therefore take this into account, and "mirror" the data as needed.

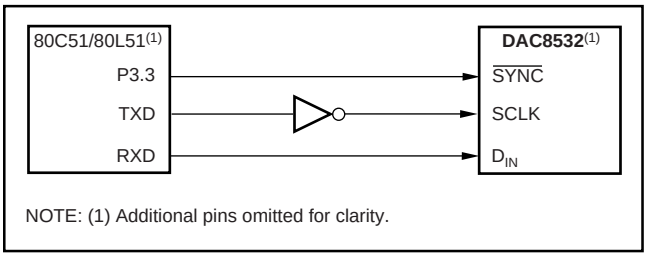


FIGURE 6. DAC8532 to 80C51/80L51 Interface.

DAC8532 to Microwire INTERFACE

Figure 7 shows an interface between the DAC8532 and any Microwire compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the DAC8532 on the rising edge of the SK signal.

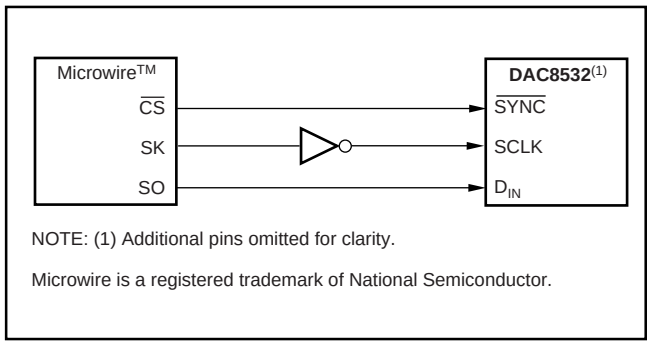


FIGURE 7. DAC8532 to Microwire Interface.

DAC8532 to 68HC11 INTERFACE

Figure 8 shows a serial interface between the DAC8532 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC8532, while the MOSI output drives the serial data line of the DAC. The $\overline{SYNC}$ signal is derived from a port line (PC7), similar to the 8051 diagram.

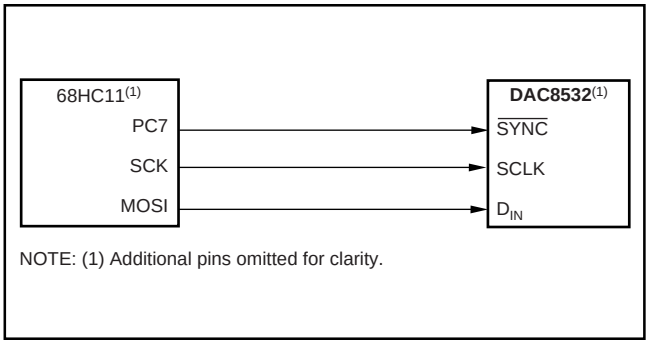


FIGURE 8. DAC8532 to 68HC11 Interface.

The 68HC11 should be configured so that its CPOL bit is 0 and its CPHA bit is 1. This configuration causes data appearing on the MOSI output to be valid on the falling edge of SCK. When data is being transmitted to the DAC, the $\overline{SYNC}$ line is held LOW (PC7). Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. (Data is transmitted MSB first.) In order to load data to the DAC8532, PC7 is left LOW after the first eight bits are transferred, then a second and third serial write operation is performed to the DAC. PC7 is taken HIGH at the end of this procedure.

DAC8532 to TMS320 DSP INTERFACE

Figure 9 shows the connections between the DAC8532 and a TMS320 digital signal processor. By decoding the FSX signal, multiple DAC8532s can be connected to a single serial port of the DSP.

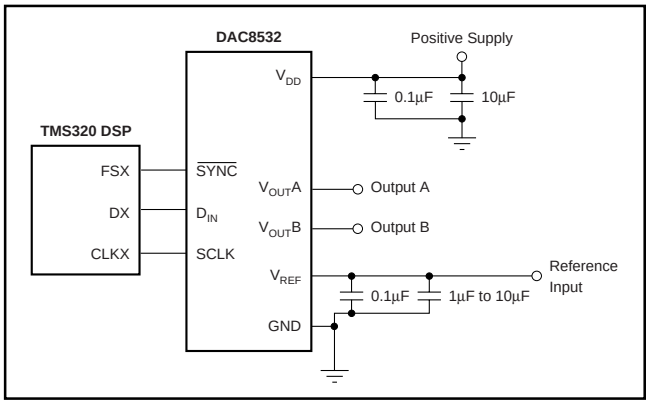


FIGURE 9. DAC8532 to TMS320 DSP.

APPLICATIONS

CURRENT CONSUMPTION

The DAC8532 typically consumes 250uA at V_{DD} = 5V and 225uA at V_{DD} = 3V for each active channel, including reference current consumption. Additional current consumption can occur at the digital inputs if V_{IH}<<V_{DD}. For most efficient power operation, CMOS logic levels are recommended at the digital inputs to the DAC.

In power-down mode, typical current consumption is 200nA. A delay time of 10 to 20ms after a power-down command is issued to the DAC is typically sufficient for the power-down current to drop below 10µA.

DRIVING RESISTIVE AND CAPACITIVE LOADS

The DAC8532 output stage is capable of driving loads of up to 1000pF while remaining stable. Within the offset and gain error margins, the DAC8532 can operate rail-to-rail when driving a capacitive load. Resistive loads of 2kΩ can be driven by the DAC8532 while achieving a typical load regulation of 1%. As the load resistance drops below 2kΩ, the load regulation error increases. When the outputs of the DAC are driven to the positive rail under resistive loading, the PMOS transistor of each Class-AB output stage can enter into the linear region. When this occurs, the added IR voltage drop deteriorates the linearity performance of the DAC. This only occurs within approximately the top 20mV of the DAC's digital input-to-voltage output transfer characteristic. The reference voltage applied to the DAC8532 may be reduced below the supply voltage applied to V_{DD} in order to eliminate this condition if good linearity is a requirement at full scale (under resistive loading conditions).

CROSSTALK AND AC PERFORMANCE

The DAC8532 architecture uses separate resistor strings for each DAC channel in order to achieve ultra-low crosstalk performance. DC crosstalk seen at one channel during a full-scale change on the neighboring channel is typically less than 0.5LSBs. The AC crosstalk measured (for a full-scale, 1kHz sine wave output generated at one channel, and measured at the remaining output channel) is typically under –100dB.

In addition, the DAC8532 can achieve typical AC performance of 96dB SNR (Signal-to-Noise Ratio) and 65db THD (Total Harmonic Distortion), making the DAC8532 a solid choice for applications requiring low SNR at output frequencies at or below 4kHz.

OUTPUT VOLTAGE STABILITY

The DAC8532 exhibits excellent temperature stability of 5ppm/°C typical output voltage drift over the specified temperature range of the device. This enables the output voltage of each channel to stay within a ±25µV window for a ±1°C ambient temperature change.

Good Power-Supply Rejection Ratio (PSRR) performance reduces supply noise present on V_{DD} from appearing at the outputs to well below 10µV-s. Combined with good DC noise performance and true 16-bit differential linearity, the DAC8532 becomes a perfect choice for closed-loop control applications.

SETTLING TIME AND OUTPUT GLITCH PERFORMANCE

Settling time to within the 16-bit accurate range of the DAC8532 is achievable within 10µs for a full-scale code change at the input. Worst case settling times between consecutive code changes is typically less than 2µs, enabling update rates up to 500ksps for digital input signals changing code-to-code. The high-speed serial interface of the DAC8532 is designed in order to support these high update rates.

For full-scale output swings, the output stage of each DAC8532 channel typically exhibits less than 100mV of overshoot and undershoot when driving a 200pF capacitive load. Code-to-code change glitches are extremely low (~10uV) given that the code-to-code transition does not cross an Nx4096 code boundary. Due to internal segmentation of the DAC8532, code-to-code glitches occur at each crossing of an Nx4096 code boundary. These glitches can approach 100mVs for N = 15, but settle out within ~2µs.

USING REF02 AS A POWER SUPPLY FOR DAC8532

Due to the extremely low supply current required by the DAC8532, a possible configuration is to use a REF02 +5V precision voltage reference to supply the required voltage to the DAC8532's supply input as well as the reference input, as shown in Figure 10. This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5V. The REF02 will output a steady supply voltage for the DAC8532. If the REF02 is used, the current it needs to supply to the DAC8532 is 567µA typical and 890µA max for V_{DD} = 5V. When a DAC output is loaded, the REF02 also needs to supply the current to the load. The total typical current required (with a 5kΩ load on a given DAC output) is:

$$567\mu A + (5V/5k\Omega) = 1.567mA$$

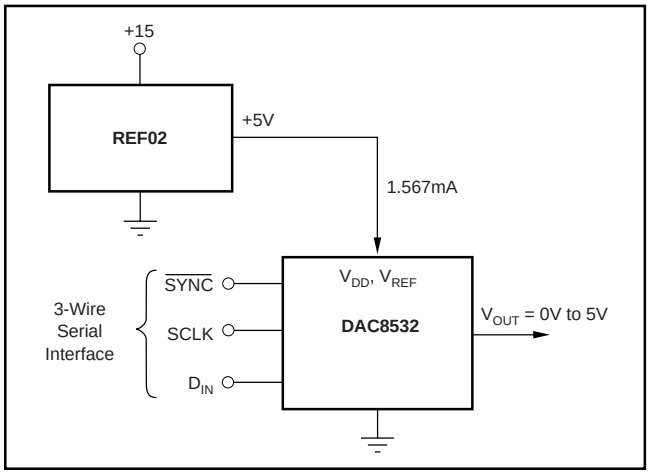


FIGURE 10. REF02 as a Power Supply to the DAC8532.

The load regulation of the REF02 is typically 0.005%/mA, which results in an error of 392µV for the 1.5mA current drawn from it. This corresponds to a 5.13LSB error for a 0V to 5V output range.

BIPOLAR OPERATION USING THE DAC8532

The DAC8532 has been designed for single-supply operation but a bipolar output range is also possible using the circuit in Figure 11. The circuit shown will give an output voltage range of $\pm V_{REF}$. Rail-to-rail operation at the amplifier output is achievable using an amplifier such as the OPA703, see Figure 11.

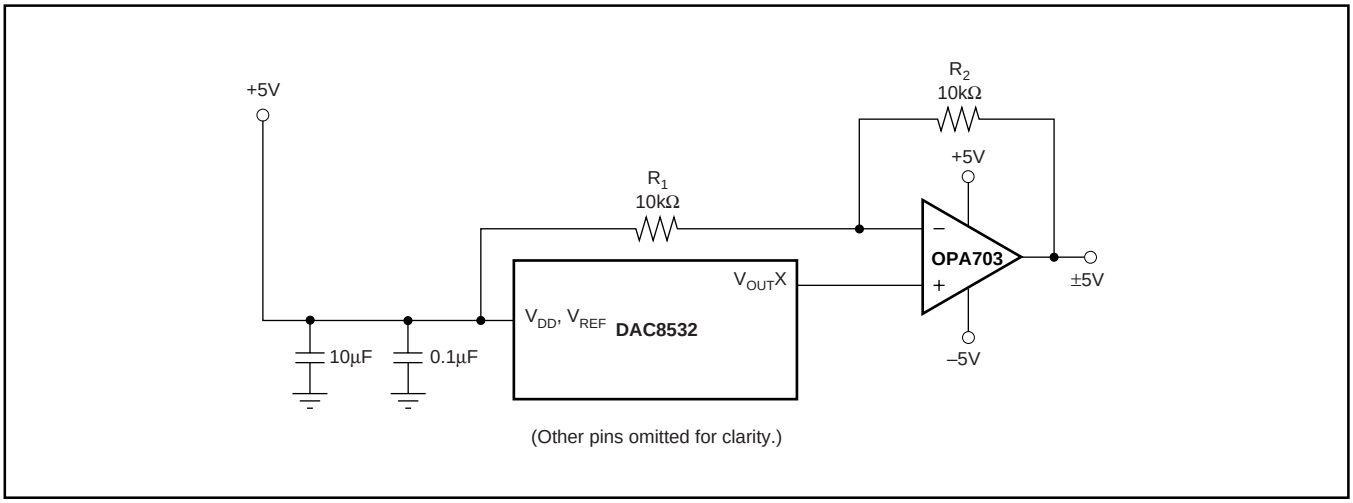


FIGURE 11. Bipolar Operation with the DAC8532.

The output voltage for any input code can be calculated as follows:

$$V_{OUT}X = \left[V_{REF} \bullet \left(\frac{D}{65536} \right) \bullet \left(\frac{R_1 + R_2}{R_1} \right) - V_{REF} \bullet \left(\frac{R_2}{R_1} \right) \right]$$

where D represents the input code in decimal (0–65535).

With V_{REF} = 5V, $R_1 = R_2$ = 10kΩ:

$$V_{OUT}X = \left(\frac{10 \bullet D}{65536} \right) - 5V$$

This is an output voltage range of ±5V with 0000_H corresponding to a –5V output and $FFFF_H$ corresponding to a +5V output. Similarly, using V_{REF} = 2.5V, a ±2.5V output voltage range can be achieved.

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The DAC8532 offers single-supply operation, and it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it will be to keep digital noise from appearing at the output.

Due to the single ground pin of the DAC8532, all return currents, including digital and analog return currents for the DAC, must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power entry point of the system.

The power applied to V_{DD} should be well regulated and low noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, V_{DD} should be connected to a positive power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. In addition, a 1µF to 10µF capacitor in parallel with a 0.1µF bypass capacitor is strongly recommended. In some situations, additional bypassing may be required, such as a 100µF electrolytic capacitor or even a “Pi” filter made up of inductors and capacitors—all designed to essentially low-pass filter the supply, removing the high-frequency noise.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DAC8532IDGK	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	Request Free Samples
DAC8532IDGKG4	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	Request Free Samples
DAC8532IDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	Purchase Samples
DAC8532IDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	Purchase Samples

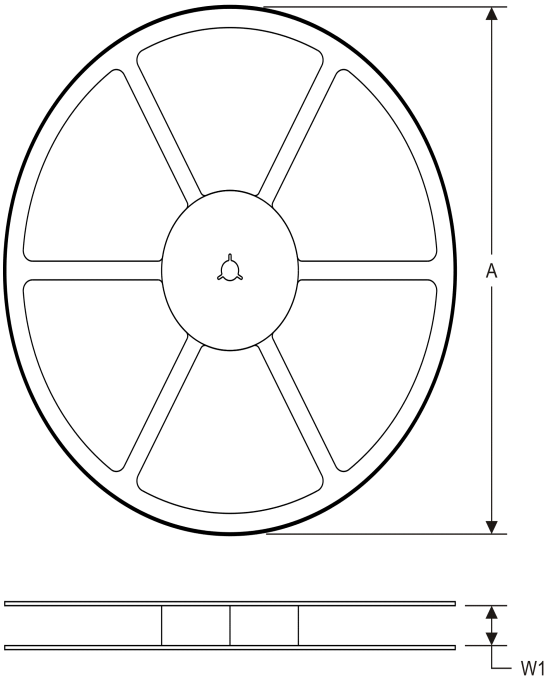
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

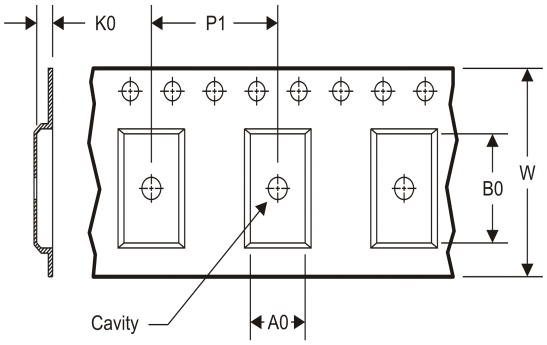
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



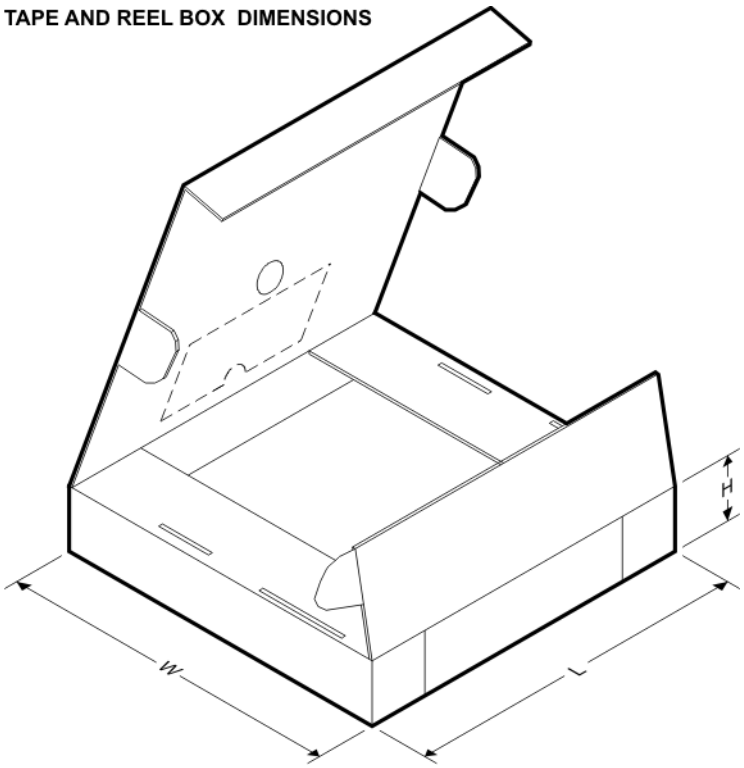
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8532IDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

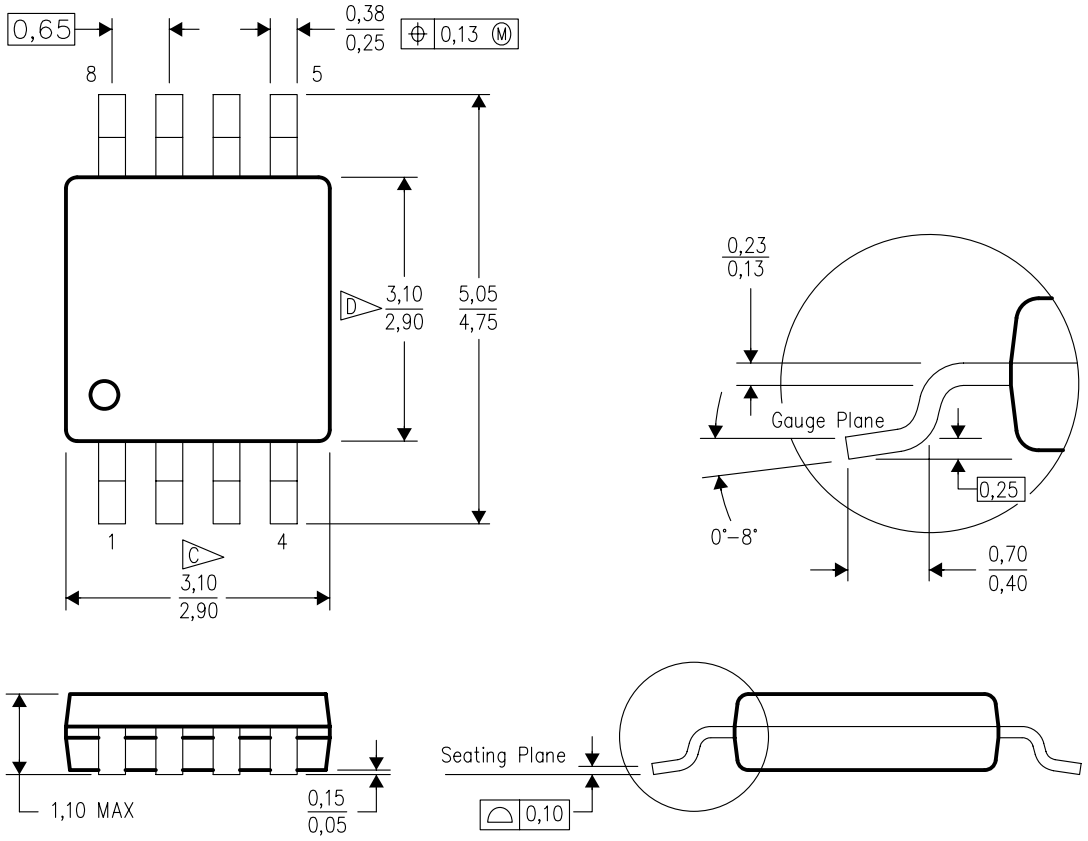
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8532IDGKR	MSOP	DGK	8	2500	346.0	346.0	29.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

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