



Dual, 12-Bit, Parallel Input, Multiplying Digital-to-Analog Converter

FEATURES

- ±1LSB INL
- 2.5V to 5.5V Supply Operation
- Fast Parallel Interface:
 17ns Write Cycle
- Update Rate of 20.4MSPS
- 10MHz Multiplying Bandwidth
- ±15V Reference Input
- Extended Temperature Range: -40°C to +125°C
- 40-Lead QFN
- 12-Bit Monotonic
- 4-Quadrant Multiplication
- Power-On Reset with Brownout Detection
- Readback Function
- Industry-Standard Pin Configuration
- Pin-Compatible with the AD5405

APPLICATIONS

- Portable Battery-Powered Instruments
- Waveform Generators
- Analog Processing
- Programmable Amplifiers and Attenuators
- Digitally-Controlled Calibration
- Programmable Filters and Oscillators
- Ultrasound

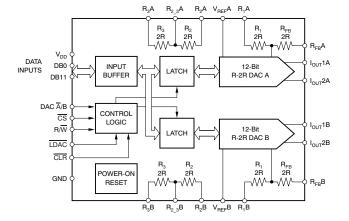
DESCRIPTION

The DAC7822 is a dual, CMOS, 12-bit, current output digital-to-analog converter (DAC). This device operates from a 2.5V to 5.5V power supply, making it suitable for battery-powered and many other applications.

The DAC7822 operates with a fast parallel interface. Data readback allows the user to read the contents of the DAC register via the DB pins. On power-up, the internal register and latches are filled with zeroes and the DAC outputs are at zero scale.

The DAC7822 offers excellent 4-quadrant multiplication characteristics, with large signal multiplying bandwidth of 10MHz. The applied external reference input voltage (V_{REF}) determines the full-scale output current. An integrated feedback resistor (R_{FB}) provides temperature tracking and full-scale voltage output when combined with an external current-to-voltage precision amplifier. The DAC7822 also includes the resistors necessary for 4-quadrant multiplication and other configuration modes.

The DAC7822 is available in a 40-lead QFN package.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

| | DAC7822 | UNIT |
|---|-------------------------------|------|
| V _{DD} to GND | -0.3 to +7.0 | V |
| Digital input voltage to GND | -0.3 to V _{DD} + 0.3 | V |
| V _{OUT} to GND | -0.3 to V _{DD} + 0.3 | V |
| Operating temperature range | -40 to +125 | °C |
| Storage temperature range | -65 to +150 | °C |
| Junction temperature (T _J max) | +150 | °C |
| ESD Rating, HBM | 2000 | V |
| ESD Rating, CDM | 1000 | V |

⁽¹⁾ Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



ELECTRICAL CHARACTERISTICS

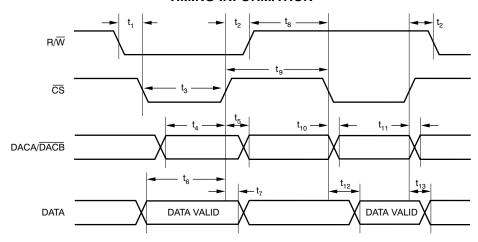
 V_{DD} = +2.5V to +5.5V; $I_{OUT}1$ = Virtual GND; $I_{OUT}2$ = 0V; V_{REF} = 10V; T_A = full operating temperature. All specifications -40°C to +125°C, unless otherwise noted.

| PARAMETER | | CONDITIONS | MIN | TYP MAX | | UNITS | |
|--|-----------------|--|-----|---------|------|--------------------|--|
| STATIC PERFORMANCE | | | | | ' | | |
| Resolution | | | 12 | | | Bits | |
| Relative accuracy | | | | | ±1 | LSB | |
| Differential nonlinearity | | | | | ±1 | LSB | |
| Output leakage current | | Data = 000h, T _A = +25°C | | | ±1 | nA | |
| Output leakage current | | Data = 000h, T _A = T _{MAX} | | | ±15 | nA | |
| Full-scale gain error | | All ones loaded to DAC register | | ±10 | ±25 | mV | |
| Full-scale tempco ⁽¹⁾ | | | | ±5 | | ppm/°C | |
| Bipolar zero-code error | | Circuit configuration as shown in Figure 41 | | | ±25 | mV | |
| Output capacitance | | DAC latches leaded with all 1s | | 25 | 30 | pF | |
| REFERENCE INPUT | | | | | ' | | |
| V _{REF} range | | | -15 | | 15 | V | |
| V _{REF} A, V _{REF} B, Input resistance | | | 8 | 10 | 12 | kΩ | |
| R ₁ , R _{FB} resistance | | | 17 | 20 | 25 | kΩ | |
| R ₂ , R ₃ resistance | | | 17 | 20 | 25 | kΩ | |
| V _{REF} A to V _{REF} B Input Mismatch | | | | 1.6 | 2.5 | % | |
| R ₂ to R ₃ Mismatch | | | | 0.06 | 0.18 | % | |
| LOGIC INPUTS AND OUTPUT ⁽¹⁾ | | | | | , | | |
| lament lancounting and | ., | V _{DD} = +2.5V | | | 0.6 | V | |
| Input low voltage | V_{IL} | $V_{DD} = +2.5V$ $V_{DD} = +5V$ | | | 0.8 | V | |
| lament binds coaltains | ., | Vpp = +2 5V | 2.1 | | | V | |
| Input high voltage | V_{IH} | $V_{DD} = +5V$ | 2.4 | | | V | |
| Input leakage current | I _{IL} | | | | 1 | μA | |
| Input capacitance | C_IL | | | | 10 | pF | |
| POWER REQUIREMENTS | | | | | ' | | |
| V_{DD} | | | 2.5 | | 5.5 | V | |
| I _{DD} (normal operation) | | Logic inputs = 0V | | | 5 | μA | |
| V _{DD} = +4.5V to +5.5V | | $V_{IH} = V_{DD}$ and $V_{IL} = GND$ | | 8.0 | 5 | μA | |
| $V_{DD} = +2.5V \text{ to } +3.6V$ | | $V_{IH} = V_{DD}$ and $V_{IL} = GND$ | | 0.4 | 2.5 | μA | |
| AC CHARACTERISTICS ⁽¹⁾ | | | | | ' | | |
| Output voltage settling time | | | | | 0.2 | μs | |
| Reference multiplying BW | | V _{REF} = 7V _{PP} , Data = FFFh | | 10 | | MHz | |
| DAC glitch impulse | | V _{REF} = 0V to 10V, Data = 7FFh to 800h to 7FFh | | 10 | | nV-s | |
| Feedthrough error V _{OUT} /V _{REF} | | Data = 000h, V _{REF} = 100kHz | | -70 | | dB | |
| Digital feedthrough | | | | 2 | | nV-s | |
| Total harmonic distortion | | | | -105 | | dB | |
| Output spot noise voltage | | | | 25 | | nV/√ Hz | |

⁽¹⁾ Specified by design and characterization; not production tested.



TIMING INFORMATION



TIMING REQUIREMENTS: 2.5V to 5.5V

At $t_r = t_f = 1$ ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$; $V_{DD} = 2.5V$ to 5.5V, $V_{REF} = 10V$, $I_{OUT}2 = 0V$. All specifications $-40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted.

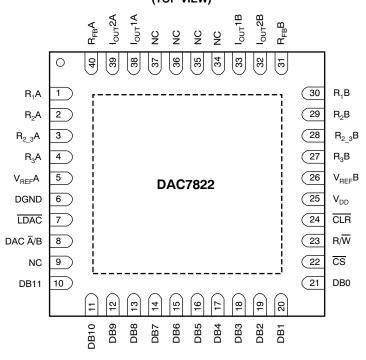
| | | DAC7822 | | | |
|-----------------|---------------------------------|---------|-----|-----|------|
| PARAMETER (1) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| t ₁ | R/W to CS setup time | 0 | | | ns |
| t ₂ | R/W to CS hold time | 0 | | | ns |
| t ₃ | CS low time (write cycle) | 10 | | | ns |
| t ₄ | Address setup time | 10 | | | ns |
| t ₅ | Address hold time | 0 | | | ns |
| t ₆ | Data setup time | 6 | | | ns |
| t ₇ | Data hold time | 0 | | | ns |
| t ₈ | R/W high to CS low | 5 | | | ns |
| t ₉ | CS minimum high time | 7 | | | ns |
| t ₁₀ | Address setup time (Read Cycle) | 0 | | | ns |
| t ₁₁ | Address hold time (Read Cycle) | 0 | | | ns |
| t ₁₂ | Data access time | | 5 | 35 | ns |
| t ₁₃ | Bus relinquish time | | 5 | 10 | ns |

⁽¹⁾ Ensured by design; not production tested.



DEVICE INFORMATION

RTA PACKAGE QFN-40 (TOP VIEW)



TERMINAL FUNCTIONS

| PIN NO. | PIN NAME | DESCRIPTION |
|----------|--|--|
| 1-4 | R ₁ A, R ₂ A, R _{2_3} A, R ₃ A | DAC A 4-Quadrant Resistors. Allows a number of configuration modes, including bipolar operation with minimum of external components. |
| 5, 26 | V _{REF} A, V _{REF} B | DAC Reference Voltage Input Terminals. |
| 6 | DGND | Digital Ground Pin. |
| 7 | LDAC | Load DAC Input. Allows asynchronous or synchronous updates to the DAC output. The DAC is asynchronously updated when this signal goes low. Alternatively, if this line is held permanently low, an automatic or synchronous update mode is selected whereby the DAC is updated on the rising edge of CS. |
| 8 | DAC A/B | Selects DAC A or B. Low selects DAC A, and high selects DAC B. |
| 9, 34-37 | NC | Not internally connected. |
| 10-21 | DB11 to DB0 | Parallel Data Bits 11 through 0. |
| 22 | <u>cs</u> | Chip Select Input; active low. Used in conjuction with R/W to load parallel data to the input latch or to read data from the DAC register. Edge sensitive; when pulled high, the DAC data is latched. |
| 23 | R/₩ | Read/Write. When low, used in conjunction with $\overline{\text{CS}}$ to load parallel data. When high, used in conjunction with $\overline{\text{CS}}$ to read back contents of DAC register. |
| 24 | CLR | Active Low Control Input. Clears DAC output and input and DAC registers. |
| 25 | V_{DD} | Positive Power Supply Input. These parts can be operated from a supply of 2.5V to 5.5V. |
| 27-30 | R ₃ B, R _{2_3} B, R ₂ B, R ₁ B | DAC B 4-Quadrant Resistors. Allow a number of configuration modes, including bipolar operation with a minimum of external components. |
| 31, 40 | R _{FB} B, R _{FB} A | External Amplifier Output. |
| 32 | I _{OUT} 2B | DAC A Analog Ground. This pin typically should be tied to the analog ground of the system, but can be biased to achieve single-supply operation. |
| 33 | I _{OUT} 1B | DAC B Current Output. |
| 38 | I _{OUT} 1A | DAC A Current Output. |
| 39 | I _{OUT} 2A | DAC A Analog Ground. This pin typically should be tied to the analog ground of the system, but can be biased to achieve single-supply operation. |



TYPICAL CHARACTERISTICS: V_{DD} = +5V

At $T_A = +25$ °C, $+V_{DD} = +5V$, unless otherwise noted.

Channel A

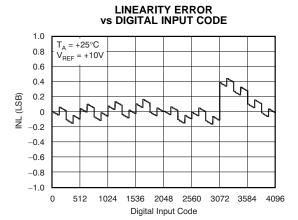


Figure 1.

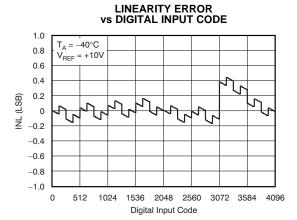


Figure 3.

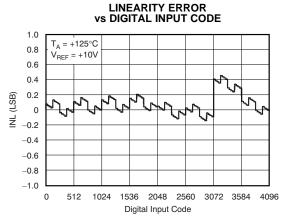


Figure 5.

DIFFERENTIAL LINEARITY ERROR VS DIGITAL INPUT CODE

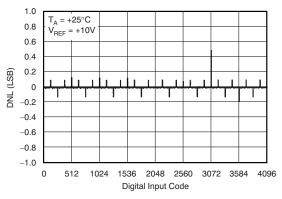


Figure 2.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

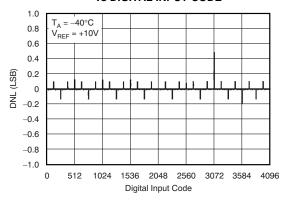


Figure 4.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

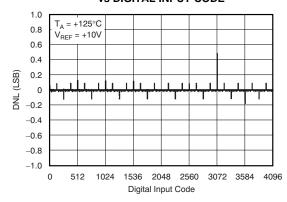


Figure 6.



TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At $T_A = +25$ °C, $+V_{DD} = +5V$, unless otherwise noted.

Channel B

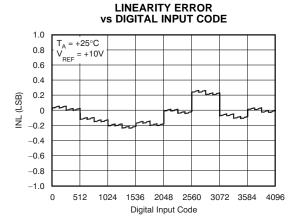


Figure 7.

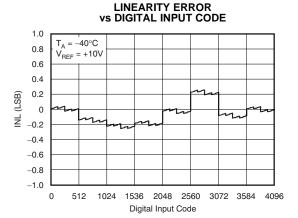


Figure 9.

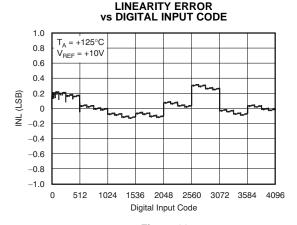


Figure 11.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

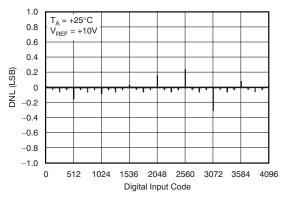


Figure 8.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

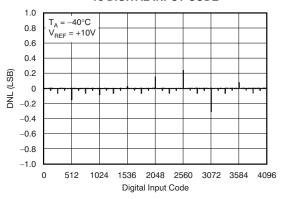


Figure 10.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

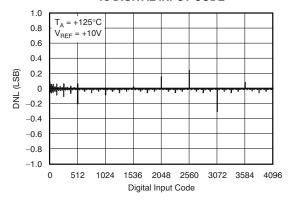


Figure 12.



TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At $T_A = +25$ °C, $+V_{DD} = +5V$, unless otherwise noted.

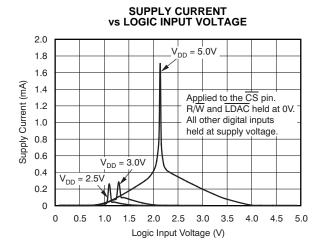


Figure 13.

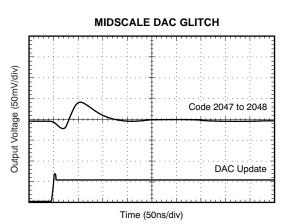


Figure 15.

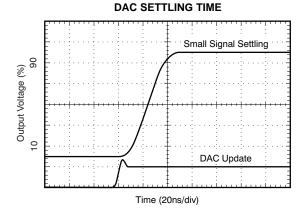


Figure 17.

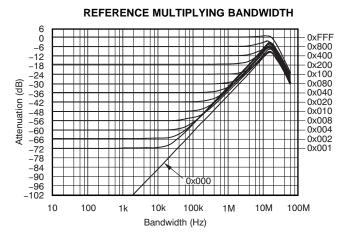


Figure 14.

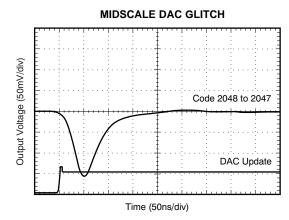


Figure 16.

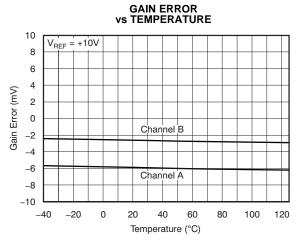


Figure 18.



TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At $T_A = +25$ °C, $+V_{DD} = +5V$, unless otherwise noted.

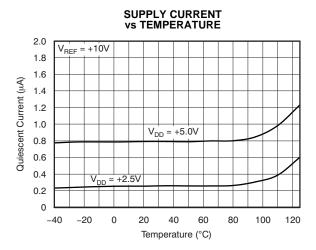


Figure 19.

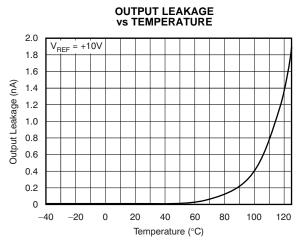


Figure 20.



TYPICAL CHARACTERISTICS: V_{DD} = +2.5V

At $T_A = +25^{\circ}C$, $+V_{DD} = +2.5V$, unless otherwise noted.

Channel A

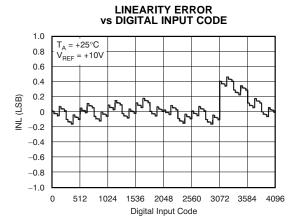


Figure 21.

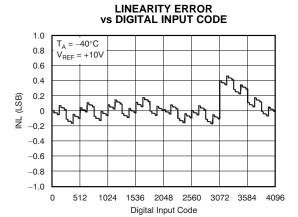


Figure 23.

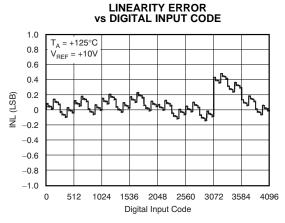


Figure 25.

DIFFERENTIAL LINEARITY ERROR VS DIGITAL INPUT CODE

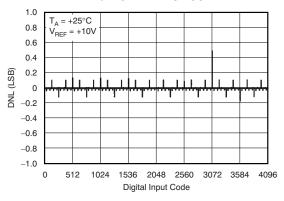


Figure 22.

DIFFERENTIAL LINEARITY ERROR VS DIGITAL INPUT CODE

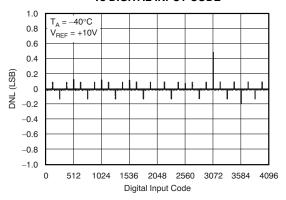


Figure 24.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

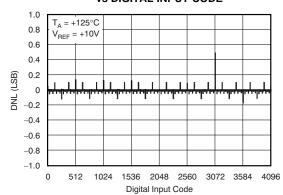


Figure 26.



TYPICAL CHARACTERISTICS: V_{DD} = +2.5V (continued)

At $T_A = +25$ °C, $+V_{DD} = +2.5$ V, unless otherwise noted.

Channel B

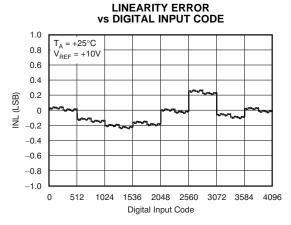


Figure 27.

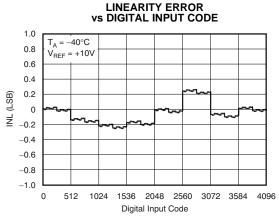


Figure 29.

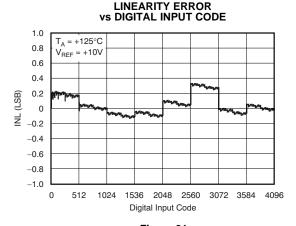


Figure 31.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

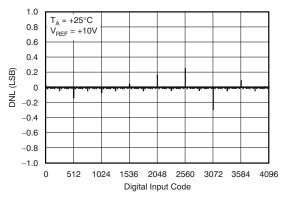


Figure 28.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

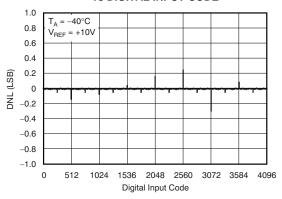


Figure 30.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

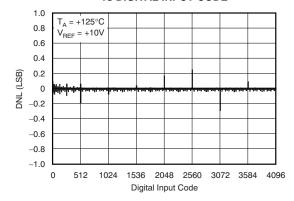


Figure 32.



TYPICAL CHARACTERISTICS: V_{DD} = +2.5V (continued)

At $T_A = +25$ °C, $+V_{DD} = +2.5$ V, unless otherwise noted.

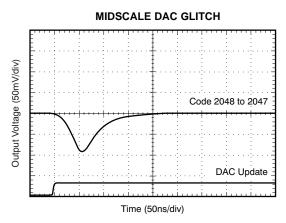


Figure 33.

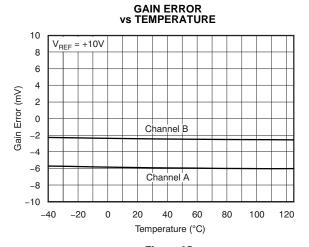


Figure 35.

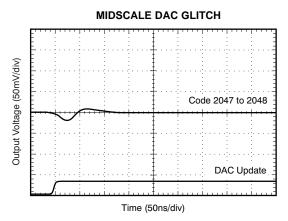


Figure 34.

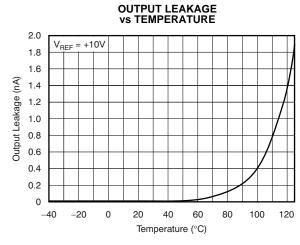


Figure 36.



THEORY OF OPERATION

The DAC7822 is a dual channel, current output, 12-bit, digital-to-analog converter (DAC). The architecture, illustrated in Figure 37, is an R-2R ladder configuration with the three MSBs segmented. Each 2R leg of the ladder is either switched to $I_{OUT}1$ or the $I_{OUT}2$ terminal. The $I_{OUT}1$ terminal of the DAC is held at a virtual GND potential by the use of an external I/V converter op amp. The R-2R ladder is connected to an external reference input V_{REF} that determines the DAC full-scale current. The R-2R ladder presents a code-independent load impedance to the external reference of $10k\Omega \pm 20\%$. The external reference voltage can vary over a range of -15V to +15V, thus providing bipolar I_{OUT} current operation. By using an external I/V converter and the DAC7822 R_{FB} resistor, output voltage ranges of $-V_{REF}$ to V_{REF} can be generated.

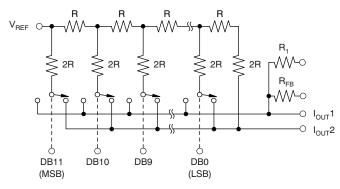


Figure 37. Equivalent R-2R DAC Circuit

When using an external I/V converter and the DAC7822 R_{FB} and R_1 resistors, the DAC output voltage is given by Equation 1:

$$V_{OUT} = -V_{REF} \times \frac{CODE}{4096}$$
 (1)

Each DAC code determines the 2R leg switch position to either GND or I_{OUT} . Because the DAC output impedance as seen looking into the $I_{OUT}1$ terminal changes versus code, the external I/V converter noise gain also changes. Because of this, the external I/V converter op amp must have a sufficiently low offset voltage such that the amplifier offset is not modulated by the DAC $I_{OUT}1$ terminal impedance change. External op amps with large offset voltages can produce INL errors in the transfer function of the DAC7822 as a result of offset modulation versus DAC code.

For best linearity performance of the DAC7822, a low input offset voltage op amp (such as the OPA277) is recommended (see Figure 38). This circuit allows V_{RFF} swinging from -10V to +10V.

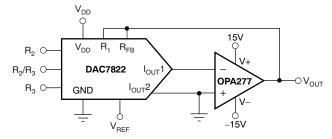


Figure 38. Voltage Output Configuration



APPLICATION INFORMATION

Stability Circuit

For a current-to-voltage design (see Figure 39), the DAC7822 current output (I_{OUT}) and the connection with the inverting node of the op amp should be as short as possible and according to correct printed circuit board (PCB) layout design practices. For each code change, there is a step function. If the gain bandwidth product (GBP) of the op amp is limited and parasitic capacitance is excessive at the inverting node, then gain peaking is possible. Therefore, for circuit stability, a compensation capacitor C_1 (1pF to 5pF typ) can be added to the design, as shown in Figure 39.

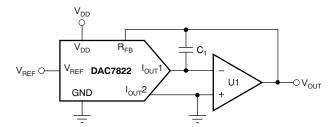


Figure 39. Gain Peaking Prevention Circuit with Compensation Capacitor

Amplifier Selection

There are many choices and many differences in selecting the proper operational amplifier for a multiplying DAC (MDAC). Making the analog signal out of the MDAC is one critical aspect. However, there are also other issues to take into account such as amplifier noise, input bias current, and offset voltage, as well as MDAC resolution and glitch energy. Table 1 and Table 2 suggest some suitable operational amplifiers for low power, fast settling, and high-speed applications. A greater selection of operational amplifiers can be found at www.ti.com/amplifer.

Table 1. Suitable Precision Operational Amplifiers from Texas Instruments

| PRODUCT | TOTAL SUPPLY VOLTAGE (V) (min) | TOTAL SUPPLY VOLTAGE (V) (max) | I _Q PER CHANNEL (max) (mA) | GBW (typ) (MHz) | SLEW RATE (typ) (V/µs) | OFFSET DRIFT (typ) (μV/°C) | I _{IB} (max) (pA) | CMRR (min) (dB) | PACKAGE/ LEAD | DESCRIPTION | |
|---------------|---|---|---|-----------------------|---------------------------------|-------------------------------------|----------------------------|-----------------------|-------------------------------|---|--|
| Low Power | | | | | | | | | | | |
| OPA703 | 4 | 12 | 0.2 | 1 | 0.6 | 4 | 10 | 70 | SOT5-23, PDIP-8, SOIC-8 | 12V, CMOS, Rail-to-Rail I/O, Operational Amplifier | |
| OPA735 | 2.7 | 12 | 0.75 | 1.6 | 1.5 | 0.01 | 200 | 115 | SOT5-23, SOIC-8 | 0.05µV/°C (max), Single-Supply CMOS Zero-Drift Series Operational Amplifier | |
| OPA344 | 2.7 | 5.5 | 0.25 | 1 | 1 | 2.5 | 10 | 80 | SOT5-23, PDIP-8, SOIC-8 | Low Power, Single-Supply, Rail-To-Rail Operational Amplifiers MicroAmplifier Series | |
| OPA348 | 2.1 | 5.5 | 0.065 | 1 | 0.5 | 2 | 10 | 70 | SC5-70, SOT5-23, SOIC-8 | 1MHz, 45µA, Rail-to-Rail I/O, Single Op Amp | |
| OPA277 | 4 | 36 | 0.825 | 1 | 0.8 | 0.1 | 1000 | 130 | PDIP-8, SOIC-8, SON-8 | High Precision Operational Amplifiers | |
| Fast Settling | | | J. | I | | | | | | | |
| OPA350 | 2.7 | 5.5 | 7.5 | 38 | 22 | 4 | 10 | 76 | MSOP-8, PDIP-8, SOIC-8 | High-Speed, Single-Supply, Rail-to-Rail Operational Amplifiers MicroAmplifier Series | |
| OPA727 | 4 | 12 | 6.5 | 20 | 30 | 0.6 | 500 | 86 | MSOP-8, SON-8 | e-trim 20MHz, High Precision CMOS Operational Amplifier | |
| OPA227 | 5 | 36 | 3.8 | 8 | 2.3 | 0.1 | 10000 | 120 | PDIP-8, SOIC-8 | High Precision, Low Noise Operational Amplifiers | |



| PRODUCT | SUPPLY VOLTAGE (V) | GBW PRODUCT (MHz) | VOLTAGE NOISE nV/√Hz | GBW (typ) (MHz) | SLEW RATE (V/µs) | V _{os} (typ) (μV) | V _{OS} (max) (μV) | CMRR (min) (dB) | PACKAGE/ LEAD | DESCRIPTION |
|--------------------|--------------------------|-------------------------|----------------------------|-----------------------|------------------------|----------------------------------|----------------------------------|-----------------------|-------------------------------|---|
| Single Chann | el | | | | | | | | | |
| THS4281 | ±2.7 to ±15 | 38 | 12.5 | 35 | 500 | 3500 | 500 | 1000 | SOT5-23, MSOP-8, SOIC-8 | Very Low-Power High Speed Rail-To-Rail Input/Output Voltage Feedback Operational Amplifier |
| THS4031 | ±4.5 to ±16.5 | 200 | 1.6 | 100 | 500 | 3000 | 3000 | 8000 | CDIP-8, MSOP-8, SOIC-8 | 100-MHz Low Noise Voltage-Feedback Amplifier |
| THS4631 | ±4.5 to ±16.5 | 210 | 7 | 900 | 260 | 2000 | 50pA | 2 | SOIC-8, MSOP-8 | High Speed FET-Input Operational Amplifier |
| OPA656 | ±4 to ±6 | 230 | 7 | 290 | 250 | 2600 | 2pA | 5pA | SOIC-8, SOT5-23 | Wideband, Unity Gain Stable FET-Input Operational Amplifier |
| OPA820 | ±2.5 to ±6 | 280 | 2.5 | 240 | 200 | 1200 | 900 | 23,000 | SOIC-8, SOT5-23 | Unity Gain Stable, Low Noise, Voltage Feedback Operational Amplifier |
| Dual Channe | | | | | | | | | | |
| THS4032 | ±4.5 to ±16.5 | 200 | 1.6 | 100 | 500 | 3000 | 3000 | 8000 | SOIC-8, MSOP-8 | 100-MHz Low Noise Voltage-Feedback Amplifier, Dual |
| OPA2822 | ±2 to ±6.3 | 220 | 2 | 170 | 200 | 1200 | 9600 | 12000 | SOIC-8, MSOP-8 | SpeedPlus Dual Wideband, Low-Noise Operational Amplifier |

Positive Voltage Output Circuit

As Figure 40 illustrates, in order to generate a positive voltage output, a negative reference is input to the DAC7822. This design is suggested instead of using an inverting amp to invert the output as a result of resistor tolerance errors. For a negative reference, V_{OUT} and GND of the reference are level-shifted to a virtual ground and a -2.5V input to the DAC7822 with an op amp.

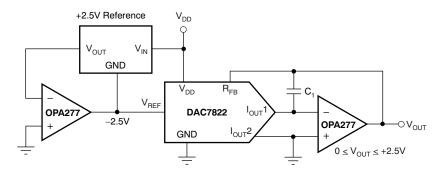


Figure 40. Positive Voltage Output Circuit

Bipolar Output Section

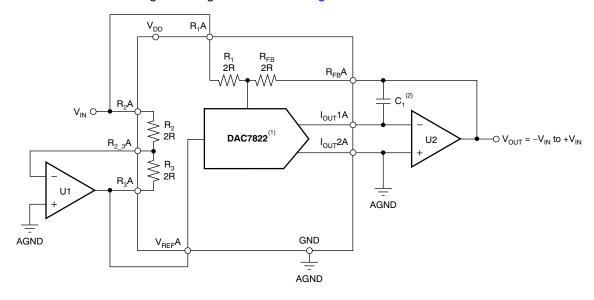
The DAC7822, as a 2-quadrant multiplying DAC, can be used to generate a unipolar output. The polarity of the full-scale output I_{OUT} is the inverse of the input reference voltage at V_{REF} .

Some applications require full 4-quadrant multiplying capabilities or bipolar output swing. As shown in Figure 41, external op amp U2 is added as a summing amp and has a gain of 2X that widens the output span to 5V. A 4-quadrant multiplying circuit is implemented by using a 2.5V offset of the reference voltage to bias U2. According to the circuit transfer equation given in Equation 2, input data (D) from code 0 to full-scale produce output voltages of $V_{OUT} = -2.5V$ to $V_{OUT} = +2.5V$.

$$V_{OUT} = \left(\frac{D}{0.5 \times 2^{N}} - 1\right) \times V_{REF}$$
 (2)



External resistance mismatching is the significant error in Figure 41.



NOTES: (1) Similar configuration for DAC B.

(2) C₁ phase compensation (1pF to 5pF) may be required if U2 is a high-speed amplifier.

Figure 41. Bipolar Output Circuit

Parallel Interface

Data are loaded to the DAC7822 as a 12-bit parallel word. The bi-directional bus is controlled with \overline{CS} and R/\overline{W} , allowing data to be written to or read from the DAC register. To write to the device, \overline{CS} and R/\overline{W} are brought low, and data available on the data lines fills the input register. The rising edge of \overline{CS} latches the data and transfers the latched data-word to the DAC register. The DAC latches are not transparent; therefore, a write sequence must consist of a falling and rising edge on \overline{CS} in order to ensure that data are loaded to the DAC register and its analog equivalent is reflected on the DAC output.

To read data stored in the device, R/\overline{W} is held high and \overline{CS} is brought low. Data are loaded from the DAC register back to the input register and out onto the data line, where it can be read back to the controller.

Cross-Reference

The DAC7822 has an industry-standard pinout. Table 3 provides the cross-reference information.

Table 3. Cross-Reference

| PRODUCT | INL (LSB) | DNL (LSB) | SPECIFIED TEMPERATURE RANGE | PACKAGE DESCRIPTION | PACKAGE OPTION | CROSS- REFERENCE PART |
|---------|-----------|-----------|-----------------------------------|------------------------|-------------------|--------------------------|
| DAC7822 | ±1 | ±1 | -40°C to +125°C | 40-Lead QFN | QFN-40 | AD5405 |





21-May-2010

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|--------------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| DAC7822IRTAR | ACTIVE | WQFN | RTA | 40 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| DAC7822IRTARG4 | ACTIVE | WQFN | RTA | 40 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| DAC7822IRTAT | ACTIVE | WQFN | RTA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| DAC7822IRTATG4 | ACTIVE | WQFN | RTA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION

REEL DIMENSIONS





TAPE DIMENSIONS



| A0 | Dimension designed to accommodate the component width |
|----|---|
| В0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

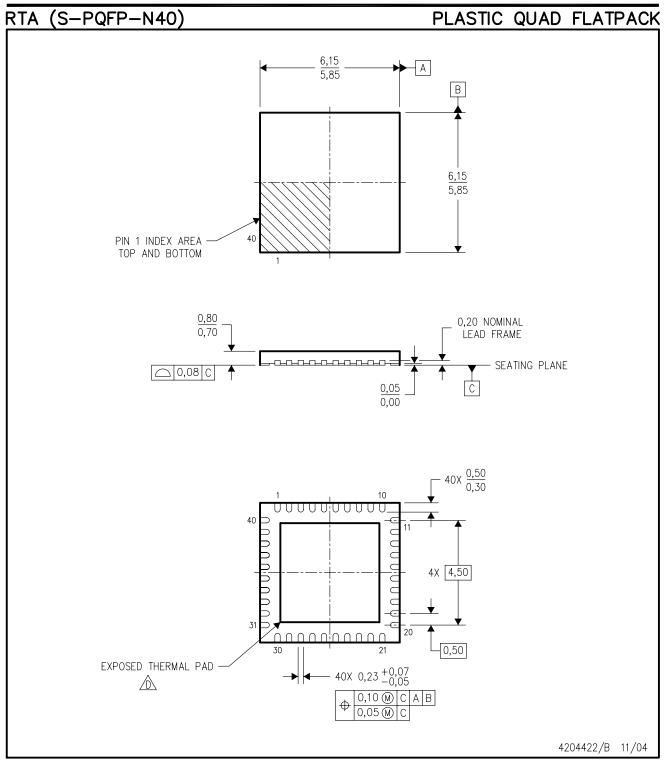
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|---------------------------------|-----------------|--------------------|----|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| Device | Package Type | Package Drawing | | | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
| DAC7822IRTAR | WQFN | RTA | 40 | 2000 | 330.0 | 16.4 | 6.3 | 6.3 | 1.5 | 12.0 | 16.0 | Q2 |
| DAC7822IRTAT | WQFN | RTA | 40 | 250 | 330.0 | 16.4 | 6.3 | 6.3 | 1.5 | 12.0 | 16.0 | Q2 |

www.ti.com 16-Feb-2012



*All dimensions are nominal

| Device | Package Type | Package Drawing Pins SPQ Lo | | Length (mm) | Width (mm) | Height (mm) | |
|--------------|--------------|-----------------------------|----|-------------|------------|-------------|------|
| DAC7822IRTAR | WQFN | RTA | 40 | 2000 | 336.6 | 336.6 | 28.6 |
| DAC7822IRTAT | WQFN | RTA | 40 | 250 | 336.6 | 336.6 | 28.6 |



- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.

 See the Product Data Sheet for details regarding the exposed thermal pad dimensions.



THERMAL PAD MECHANICAL DATA



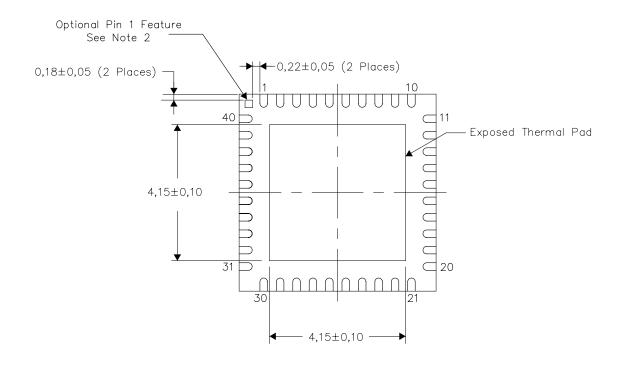
RTA (S-PWQFN-N40)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No—Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



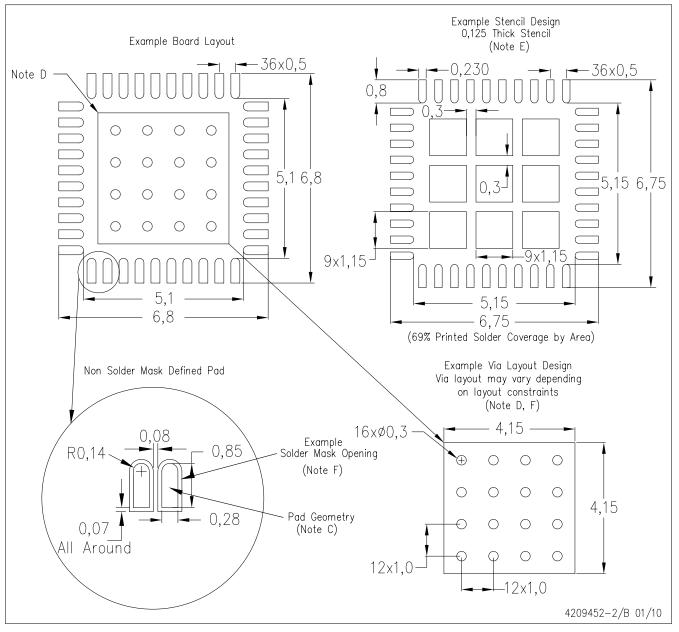
Bottom View

NOTES:

- 1) All linear dimensions are in millimeters
- 2) The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

Exposed Thermal Pad Dimensions

RTA (S-PWQFN-N40)



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.



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