



HIGH-SPEED, FULLY DIFFERENTIAL, CONTINUOUSLY VARIABLE GAIN AMPLIFIER

Check for Samples: THS7530

FEATURES

- Low Noise: V_n = 1.1 nV/√Hz,
 Noise Figure = 9 dB
- Low Distortion:
 - - HD₂ = -65 dBc, HD₃ = -61 dBc at 32 MHz
 - - IMD₃ = -62 dBc, OIP₃ = 21 dBm at 70 MHz
- 300 MHz Bandwidth
- Continuously Variable Gain Range: 11.6 dB to 46.5 dB
- Gain Slope: 38.8 dB/V
- · Fully Differential Input and Output
- Output Common-Mode Voltage Control
- Output Voltage Limiting

APPLICATIONS

- Time Gain Amplifiers in Ultra Sound, Sonar, and Radar
- Automatic Gain Control in Communication and Video
- System Gain Calibration in Communications
- Variable Gain in Instrumentation

DESCRIPTION

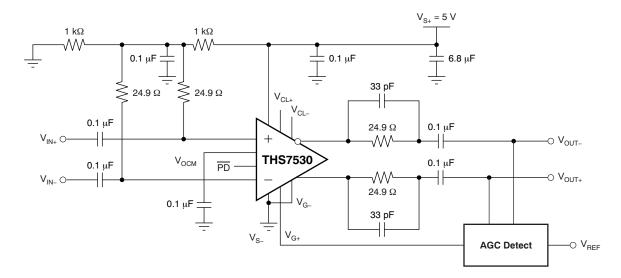
The THS7530 is fabricated using Texas Instruments' state-of-the-art BiCom III SiGe complementary bipolar process. The THS7530 is a dc-coupled, wide bandwidth amplifier with voltage-controlled gain. The amplifier has high-impedance differential inputs and low-impedance differential outputs with high bandwidth gain control, output common-mode control, and output voltage clamping.

Signal channel performance is exceptional with 300-MHz bandwidth, and third harmonic distortion of -61 dBc at 32 MHz with $1-V_{PP}$ output into $400~\Omega$.

Gain control is linear in dB with 0 V to 0.9 V varying the gain from 11.6 dB to 46.5 dB with 38.8-dB/V gain slope.

Output voltage limiting is provided to limit the output voltage swing, and prevent saturating following stages.

The device is characterized for operation over the industrial temperature range, -40°C to +85°C.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION(1)

PART NUMBER	PACKAGE TYPE	PACKAGE MARKING	TRANSPORT MEDIA, QUANTITY
THS7530PWP	T000D 44 DD	TH07520	Rails, 90
THS7530PWPR	TSSOP-14-PP THS7530	1 113/530	Tape and Reel, 2000

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

			THS7530
V _{S+} - V _{S-}	Supply	voltage	5.5 V
VI	Input vo	oltage	±V _S
Io	Output	current	65 mA
V_{ID}	Differer	ntial input voltage	±4 V
	Continu	ous power dissipation	See Dissipation Rating Table
+	Maximu	ım junction temperature	+150°C
T_J	Maximu	ım junction temperature for long term stability (2)	+125°C
T _{stg}	Storage	e temperature range	−65°C to +150°C
-		НВМ	3000 V
	ESD	CDM	1500 V
		MM	200 V

⁽¹⁾ The absolute maximum ratings under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

PACKAGE THERMAL DATA

PACKAGE	РСВ	θ _{JA} (°C/W)	(°C/W) ⁽¹⁾	T _A = 25°C POWER RATING ⁽²⁾
PWP (14-pin) ⁽³⁾	See Layout Considerations in the Application section of this data sheet.	37.5	2.07	3 W

- 1) This data was taken using the JEDEC High-K test printed circuit board (PCB).
- (2) This data was taken using 2 oz. trace and copper pad that is soldered directly to a 3 in x 3 in PCB.
- (3) The THS7530 incorporates a PowerPAD™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical briefs SLMA002 and SLMA004 for more information about using the PowerPAD thermally enhanced package.

RECOMMENDED OPERATING CONDITIONS

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$[V_{S-}$ to $V_{S+}]$	Supply voltage		4.5	5	5.5	V
T_A	Operating free-air temperature		-40		+85	ů
	Input common mode voltage	$[V_{S-} \text{ to } V_{S+}] = 5 \text{ V}$		2.5		V
	Output common mode voltage	$[V_{S-} \text{ to } V_{S+}] = 5 \text{ V}$		2.5		V

Product Folder Link(s): THS7530

⁽²⁾ The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.



SPECIFICATIONS: MAIN AMPLIFIER

 $V_{S+} = 5 \text{ V}$, $V_{S-} = 0 \text{ V}$, $V_{OCM} = 2.5 \text{ V}$, $V_{ICM} = 2.5 \text{ V}$, $V_{G-} = 0 \text{ V}$, $V_{G+} = 1 \text{ V}$ (maximum gain), $T_A = 25^{\circ}\text{C}$, ac performance measured using the ac test circuit shown in Figure 1 (unless otherwise noted). DC performance is measured using the dc test circuit shown in Figure 2 (unless otherwise noted)

		TYP	OVER TEMPERATURE				
PARAMETER	TEST CONDITIONS	+25°C	+25°C	-40°C to +85°C	UNITS	MIN/ MAX	
AC PERFORMANCE (See Figure 1)						,	
Small-signal bandwidth	All gains, P _{IN} = -45 dBm	300			MHz	Тур	
Slew rate ⁽¹⁾	1-V _{PP} Step, 25% to 75%, minimum gain	1250			V/µs	Тур	
Settling time to 1% (1)	1-V _{PP} Step, minimum gain	11			ns	Тур	
Harmonic distortion	$V_{O(PP)} = 1 \text{ V}, R_{L(diff)} = 400 \Omega$						
2nd Harmonic	f = 32 MHz	-65			dBc	Тур	
3rd Harmonic	f = 32 MHz	-61			dBc	Тур	
Third-order intermodulation distortion	$P_O = -10$ dBm each tone, $f_C = 70$ MHz, 200-kHz tone spacing	-62			dBc	Тур	
Third-order output intercept point	f _C = 70 MHz, 200-kHz tone spacing	21			dBm	Тур	
Noise figure (with input termination)	Source impedance: 50 Ω	9			dB	Тур	
Total input voltage noise	f > 100 kHz	1.1			nV/√ Hz	Тур	
DC PERFORMANCE—INPUTS (See Figure 2)		*	*		!		
Input bias current		20	39	40	μA	Max	
Input bias current offset		<150			pА	Тур	
Minimum input voltage	Minimum gain	1.5	1.6	1.7	V	Max	
Maximum input voltage	Minimum gain	3.5	3.35	3.2	V	Min	
Common-mode rejection ratio		114	56	44	dB	Min	
Differential input impedance		8.5 3.0			kΩ pF	Тур	
DC PERFORMANCE—OUTPUTS (See Figure	2)						
Output offset voltage	All gains	±100	±340	±480	mV	Max	
Maximum output voltage high		3.5	3.275	3.25	V	Min	
Minimum output voltage low		1.5	1.7	1.8	V	Max	
Output current		±37	±16	±16	mA	Min	
Output impedance		15			Ω	Тур	
OUTPUT COMMON-MODE VOLTAGE CONTR	OL (See Figure 2)						
Small-signal bandwidth		32			MHz	Тур	
Gain		1.00			V/V	Тур	
Common-mode offset voltage		4.5	12	13.8	mV	Max	
Minimum input voltage		1.75			V	Тур	
Maximum input voltage		3.25			V	Тур	
Input impedance		25 1			kΩ pF	Тур	
Default voltage, with no connect		2.5			V	Тур	
Input bias current		<1			μA	Тур	

⁽¹⁾ Slew rate and settling time measured at amplifier output.



SPECIFICATIONS: MAIN AMPLIFIER (continued)

 $V_{S+} = 5 \text{ V}$, $V_{S-} = 0 \text{ V}$, $V_{OCM} = 2.5 \text{ V}$, $V_{ICM} = 2.5 \text{ V}$, $V_{G-} = 0 \text{ V}$, $V_{G+} = 1 \text{ V}$ (maximum gain), $T_A = 25^{\circ}\text{C}$, ac performance measured using the ac test circuit shown in Figure 1 (unless otherwise noted). DC performance is measured using the dc test circuit shown in Figure 2 (unless otherwise noted)

		TYP	OVER TEMPERATURE				
PARAMETER	TEST CONDITIONS +2		+25°C	-40°C to +85°C	UNITS	MIN/ MAX	
GAIN CONTROL (See Figure 2)							
Gain control differential voltage range	V _{G+}	0 to 1			V	Тур	
Minus gain control voltage	V _{G-} - V _{S-}	-0.6 to 0.8			V	Тур	
Minimum gain	V _{G+} = 0 V	11.6			dB	Тур	
Maximum gain	V _{G+} = 0.9 V	46.5			dB	Тур	
Gain slope	V _{G+} = 0 V to 0.9 V	38.8			dB/V	Тур	
Gain slope variation	V _{G+} = 0 V to 0.9 V	±1.5			dB/V	Тур	
	V _{G+} = 0 V to 0.15 V	±4			dB	Тур	
Gain error	V _{G+} = 0.15 V to 0.9 V	±2.25			dB	Тур	
Gain control input bias current		<1			μA	Тур	
Gain control input resistance		40			kΩ	Тур	
Gain control bandwidth	Small signal –3 dB	15			MHz	Тур	
VOLTAGE CLAMPING (See Figure 2)		*				1	
Output voltages (V _{OUT±}) relative to clamp voltages (V _{CL±})	In voltage limiting mode	±25	±38	±60	mV	Max	
Input resistance		3.3			kΩ	Тур	
V _{CL±} Voltage limits		V _S - to V _{S+}			V	Тур	
POWER SUPPLY (See Figure 2)		•	•		•	,	
Specified operating voltage		5	5.5	5.5	V	Max	
Maximum quiescent current		40	48	49	mA	Max	
Power supply rejection (±PSRR)		77	70	45	dB	Min	
POWERDOWN (See Figure 2)							
Enable voltage threshold	TTL low = shut down	1.4		1.0	V	Min	
Disable voltage threshold	TTL high = normal operation	1.4		1.65	V	Max	
Power-down quiescent current		0.35	0.4	0.45	mA	Max	
Input current high		9	16	19	μA	Max	
Input current low		109	116	119	μA	Max	
Input impedance		50 1			kΩ pF	Тур	
Turn-on time delay	M 1, 500, 1	820			ns	Тур	
Turn-off time delay	Measured to 50% quiescent current	500			ns	Тур	
Forward isolation in power down		80			dB	Тур	
Input resistance in power down		> 1			ΜΩ	Тур	
Output resistance in power down		16			kΩ	Тур	



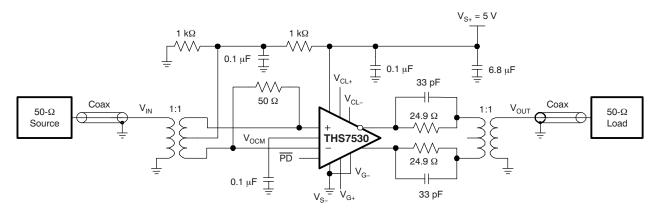


Figure 1. AC Test Circuit

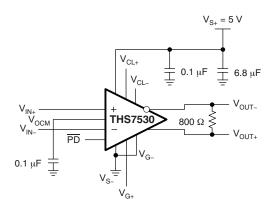


Figure 2. DC Test Circuit

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PIN ASSIGNMENTS

TSSOP PACKAGE PWP-14 (TOP VIEW)

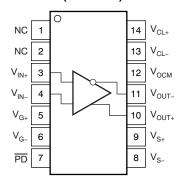


Table 1. Terminal Functions

TER	MINAL	DESCRIPTION
NO.	NAME	DESCRIPTION
1	NC	No internal connection
2	NC	No internal connection
3	V_{IN+}	Noninverting amplifier input
4	V_{IN-}	Inverting amplifier input
5	V_{G+}	Gain setting positive input
6	V_{G-}	Gain setting negative input
7	PD	Powerdown, \overline{PD} = logic low puts part into low power mode; \overline{PD} = logic high or open for normal operation
8	V_{S-}	Negative amplifier power-supply input
9	V_{S+}	Positive amplifier power-supply input
10	V_{OUT+}	Noninverted amplifier output
11	V_{OUT-}	Inverted amplifier output
12	V _{OCM}	Output common-mode voltage input
13	V _{CL}	Output negative clamp voltage input
14	V_{CL+}	Output positive clamp voltage input



TYPICAL CHARACTERISTICS

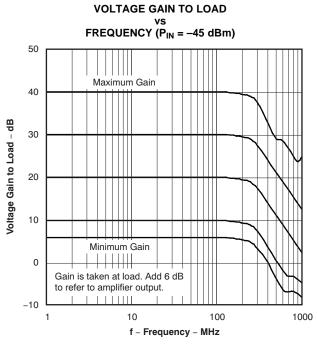
Table of Graphs

Measured using the ac test circuit shown in Figure 1 (unless otherwise noted).

		Figure
Voltage Gain to Load	vs Frequency (Input at 45 dBm)	Figure 3
Gain and Gain Error	vs V _{G+}	Figure 4
Noise Figure	vs Frequency	Figure 5
Output Intercept Point	vs Frequency	Figure 6
1-dB Compression Point	vs Frequency	Figure 7
Total Input Voltage Noise	vs Frequency	Figure 8
Intermodulation Distortion	vs Frequency	Figure 9
Harmonic Distortion	vs Frequency	Figure 10
S-Parameters	vs Frequency	Figure 11
Differential Input Impedance of Main Amplifier	vs Frequency	Figure 12
Differential Output Impedance of Main Amplifier	vs Frequency	Figure 13
V _{G+} Input Impedance	vs Frequency	Figure 14
V _{OCM} Input Impedance	vs Frequency	Figure 15
Common-Mode Rejection Ratio	vs Frequency	Figure 16
Step Response: 2 V _{PP}	vs Time	Figure 17
Step Response: Rising Edge	vs Time	Figure 18
Step Response: Falling Edge	vs Time	Figure 19



TYPICAL CHARACTERISTICS



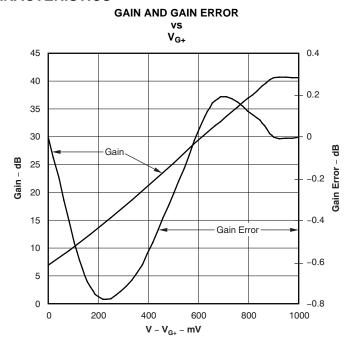
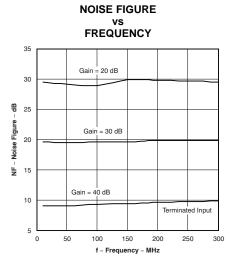
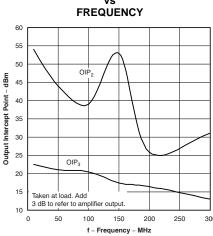


Figure 3.

Figure 4.





OUTPUT INTERCEPT POINT

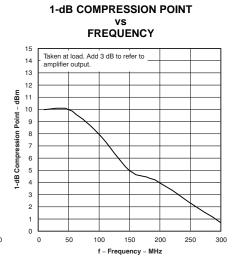


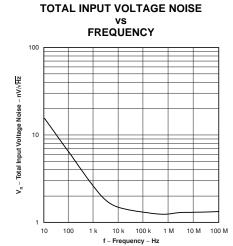
Figure 5.

Figure 6.

Figure 7.



TYPICAL CHARACTERISTICS (continued) INTERMODULATION DISTORTION



VS **FREQUENCY** -50 -55 -60 IMD₂ and IMD₃ IMD -65 -70 -75 $V_{G+} = 1 \text{ V, } V_{O} = 1 \text{ V}_{PP}$ (Composite), $R_{L} = 400 \ \Omega$

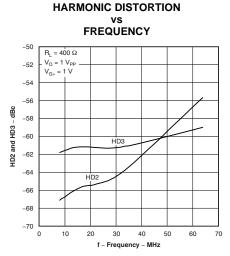


Figure 8.

Figure 9.

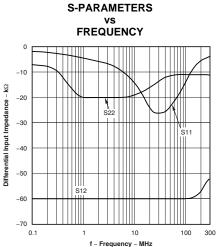
100

f - Frequency - MHz

150

50

Figure 10.





-80

0

DIFFERENTIAL INPUT IMPEDANCE OF MAIN AMPLIFIER **FREQUENCY**

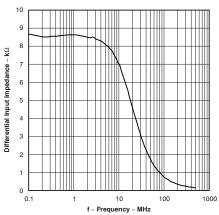


Figure 12.

DIFFERENTIAL OUTPUT IMPEDANCE OF MAIN AMPLIFIER

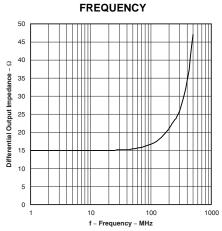


Figure 13.

Figure 11.



TYPICAL CHARACTERISTICS (continued)

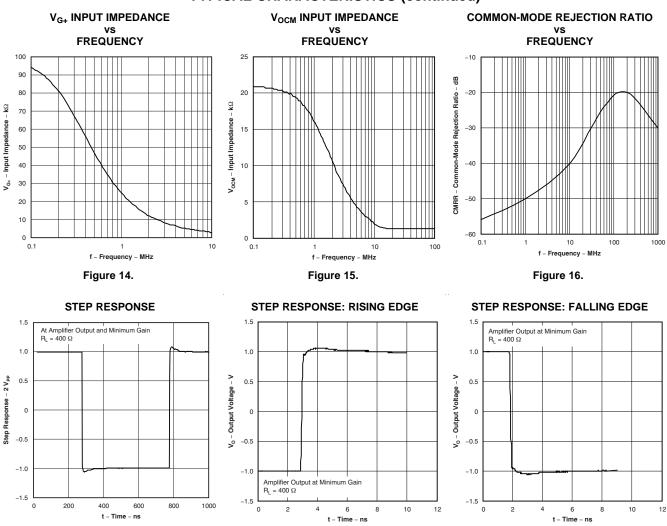


Figure 18.

Submit Documentation Feedback

Figure 17.

Figure 19.



APPLICATION INFORMATION

The THS7530 is designed for nominal 5-V power supply from V_{S+} to V_{S-} .

The amplifier has fully differential inputs, $V_{\text{IN+}}$ and $V_{\text{IN-}}$, and fully differential outputs, $V_{\text{OUT+}}$ and $V_{\text{OUT-}}$ The inputs are high impedance and outputs are low impedance. External resistors are recommended for impedance matching and termination purposes.

The inputs and outputs can be dc-coupled, but for performance, the input best and common-mode voltage should be maintained at the midpoint between the two supply pins. The output common-mode voltage is controlled by the voltage applied to V_{OCM}. Left unterminated, V_{OCM} is set to midsupply by internal resistors. A 0.1-µF bypass capacitor should be placed between V_{OCM} and ground to reduce common-mode noise. The input common-mode voltage defaults to midrail when left unconnected. For voltages other than midrail, V_{OCM}must be biased by external means. V_{IN+} and V_{IN} both require a nominal 30-µA bias current for proper operation. Therefore, ensure equal input impedance at each input to avoid generating an offset voltage that varies with gain.

Voltage applied from V_{G-} to V_{G+} controls the gain of the part with 38.8-dB/V gain slope. The input can be differential or single ended. V_{G-} must be maintained within -0.6 V and +0.8 V of V_{S-} for proper operation. The negative gain input should typically be tied directly to the negative power supply.

 $V_{\text{CL+}}$ and $V_{\text{CL-}}$ are inputs that limit the output voltage swing of the amplifier. The voltages applied set an absolute limit on the voltages at the output. Input voltages at $V_{\text{CL+}}$ and $V_{\text{CL-}}$ clamp the output, ensuring that neither output exceeds those values.

The power-down input is a TTL compatible input, referenced to the negative supply voltage. A logic low puts the THS7530 in power-saving mode. In power-down mode the part consumes less than 1-mA current, the output goes high impedance, and a high amount of isolation is maintained between the input and output.

Power-supply bypass capacitors are required for proper operation. A 6.8-µF tantalum bulk capacitor is recommended if the amplifier is located far from the power supply and may be shared among other devices. A ceramic 0.1-µF capacitor is recommended within 0.1-in of the device power pin. The ceramic capacitors should be located on the same layer as the amplifier to eliminate the use of vias between the capacitors and the power pin.

Figure 20 through Figure 24 show some basic circuit configurations.

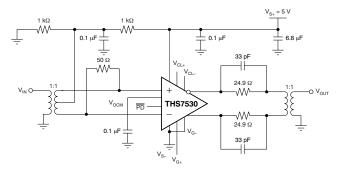


Figure 20. EVM Schematic: Designed for Use with Typical 50-Ω RF Test Equipment

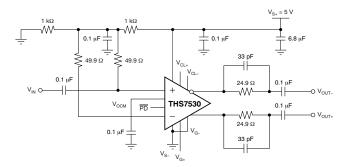


Figure 21. AC-Coupled Single-Ended Input with AC-Coupled Differential Output

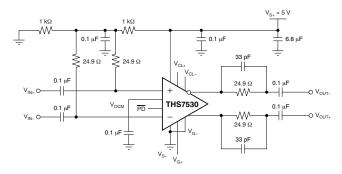


Figure 22. AC-Coupled Differential Input with AC-Coupled Differential Output



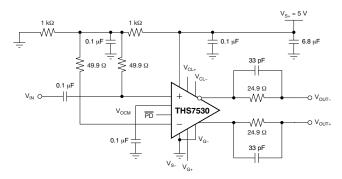


Figure 23. DC-Coupled Single-Ended Input with DC-Coupled Differential Output

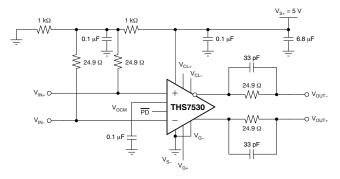


Figure 24. DC-Coupled Differential Input with DC-Coupled Differential Output

LAYOUT CONSIDERATIONS

The THS7530 comes in a thermally-enhanced PowerPAD™ package. Figure 25 shows the recommended number of vias and thermal land size recommended for best performance. Thermal vias connect the thermal land to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the thermal land on the surface of the board during solder reflow. The experiments conducted jointly with Solectron Texas indicate that a via drill diameter of 0,33 mm (13 mils, or .013 in) or smaller works well when 1-ounce copper is plated at the surface of the board and simultaneously plating the barrel of the via. If the thermal vias are not plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a dimension equal to the via diameter + 0,1 mm minimum. This prevents the solder from being wicked through the thermal via and potentially creating a solder void in the region between the package bottom and the thermal land on the surface of the PCB.

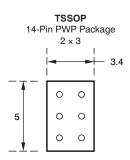


Figure 25. Recommended Thermal Land Size and Thermal Via Patterns (Dimensions in mm)

See TI's Technical Brief titled, $PowerPAD^{TM}$ Thermally Enhanced Package (SLMA002) for a detailed discussion of the PowerPADTM package, its dimensions, and recommended use.

THEORY OF OPERATION

Figure 26 shows a simplified schematic of the THS7530.

The input architecture is a modified Gilbert cell. The output from the Gilbert cell is converted to a voltage and buffered to the output as a fully-differential signal. A summing node between the outputs is used to compare the output common-mode voltage to the $V_{\rm OCM}$ input. The $V_{\rm OCM}$ error amplifier then servos the output common-mode voltage to maintain it equal to the $V_{\rm OCM}$ input. Left unterminated, $V_{\rm OCM}$ is set to midsupply by internal resistors.

The gain control input is conditioned to give linear-in-dB gain control (block H). The gain control input is a differential signal from 0 V to 0.9 V which varies the gain from 11.6 dB to 46.5 dB.

 $V_{\text{CL+}}$ and $V_{\text{CL-}}$ provide inputs that limit the output voltage swing of the amplifier.

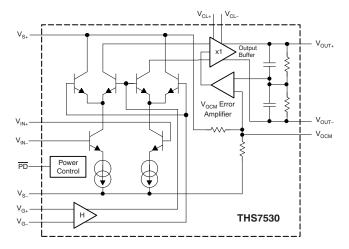


Figure 26. THS7530 Simplified Schematic



SPICE MODEL

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* THS7530 SUBCIRCUIT
 HIGH SPEED FULLY DIFFERENTIAL VARIABLE AMPLIFIER
  WRITTEN 11/26/02
  VG- is tied to VS- and output clamping is not modeled
 CONNECTIONS: IN+
    IN-
      VS+
        VS-
          OUT-
            OUT+
              VOCM
                VG+
.SUBCKT THS7530 1 2 3 4 5 6 7 8
*INPUT*
Q1 122 1 101 NPN_IN 16
Q2 123 2 102 NPN_IN 16
R1 102 101 25
I1 101 4 DC 4.85e-3
I2 102 4 DC 4.85e-3
*OUAD*
Q3 132 120 122 NPN 16
Q4 121 119 122 NPN 16
Q5 132 119 123 NPN 16
O6 121 120 123 NPN 16
R2 132 3 250
R3 121 3 250
*CURRENT AMP*
F1 128 129 VF1 6
VF1 132 121 0V
*Z NODE*
R4 128 129 2k
I3 129 4 DC 0.75e-3
I4 128 4 DC 0.75e-3
V9 128 328 0.7
```

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V10 129 329 0.7



```
*FREQUENCY SHAPING*
E3 131 0 329 0 1
R5 131 140 30
L3 140 133 7.5n
C6 133 0 24p
E4 130 0 328 0 1
R9 130 141 30
L4 141 125 10n
C7 125 0 27p
*OUTPUT BUFFER*
Q9 4 133 117 PNP 5.12
Q10 3 133 127 NPN 5.12
Q11 3 117 134 NPN 81.92
Q12 4 127 135 PNP 81.92
Q13 4 125 116 PNP 5.12
Q14 3 125 126 NPN 5.12
Q15 3 116 136 NPN 81.92
Q16 4 126 137 PNP 81.92
R6 138 134 5
R7 135 138 5
R10 139 136 5
R11 137 139 5
I5 3 117 DC 0.4e-3
I6 127 4 DC 0.4e-3
I7 3 116 DC 0.4e-3
I8 126 4 DC 0.4e-3
*OUTPUT Z*
R8 113 138 2
R12 115 139 2
L1 113 5 4n
L2 115 6 4n
C1 6 5 2p
*VOCM
Rcm1 115 114 8k
Ccm1 115 114 0.1p
Rcm2 114 113 8k
Ccm2 114 113 0.1p
E1 118 0 114 7 1e3
Rtop 3 7 50k
Rbot 4 7 50k
Q7 128 118 3 PNP 16
Q8 129 118 3 PNP 16
*GAIN CONTROL*
V8 235 8 0.454
E5 231 0 235 4 0.51
E6 232 0 POLY(1) 231 0 0.0 1 1 0.5 3.5
E7 233 0 232 0 0.115
E8 234 0 POLY(1) 233 0 0.0 0 1 0 0.333
E9 120 119 234 0 0.42
V7 3 120 1.6
Rsupply 3 4 310
.MODEL NPN_IN NPN
+ KF=1E-12
.MODEL NPN NPN
.MODEL PNP PNP
```

.ENDS



REVISION HISTORY

CI	hanges from Revision B (February, 2006) to Revision C	Page
•	Corrected polarity indication on input and output in front-page figure	1
•	Deleted lead temperature specification from Absolute Maximum Ratings table	<mark>2</mark>
•	Corrected Figure 2	5
•	Changed Figure 21 and Figure 22 to correct problem with output polarity indication	11
•	Changed Figure 23 and Figure 24 to correct problem with output polarity indication	12

PACKAGE OPTION ADDENDUM

www.ti.com 22-Feb-2010

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
THS7530PWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS7530PWPG4	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS7530PWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS7530PWPRG4	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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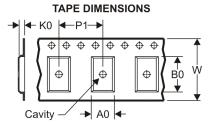
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

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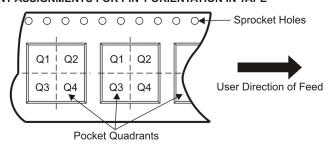
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS7530PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
I	THS7530PWPR	HTSSOP	PWP	14	2000	346.0	346.0	29.0

PWP (R-PDSO-G14)

PowerPAD ™ PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com http://www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.



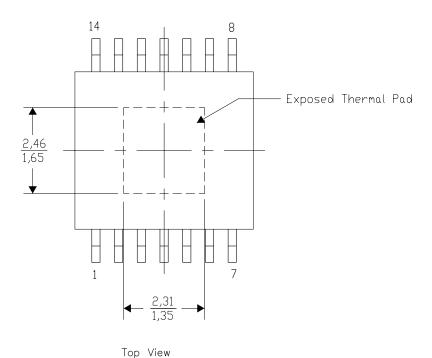
PWP (R-PDSO-G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD $^{\text{TM}}$ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206332-2/Y 10/11

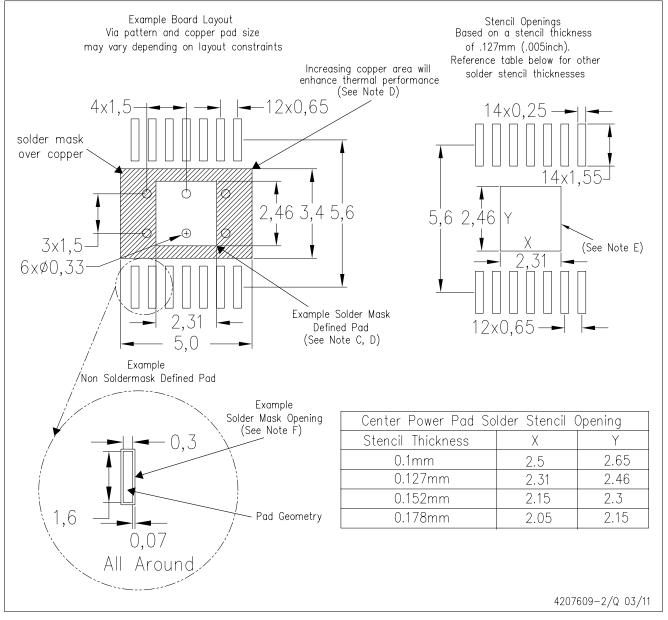
NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments



PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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