	SN74HC573A-Q1 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS SCLS600A – NOVEMBER 2004 – REVISED APRIL 2008
<ul> <li>Qualified for Automotive Applications</li> </ul>	DW OR PW PACKAGE
<ul> <li>Wide Operating Voltage Range of 2 V to 6 V</li> </ul>	(TOP VIEW)
<ul> <li>High-Current 3-State Outputs Drive Bus</li> </ul>	
Lines Directly or up to 15 LSTTL Loads	1D [2 19] 1Q
<ul> <li>Low Power Consumption, 80-μA Max I<sub>CC</sub></li> </ul>	2D [] 3 18 [] 2Q
<ul> <li>Typical t<sub>pd</sub> = 21 ns</li> </ul>	3D 4 17 3Q
• ±6-mA Output Drive at 5 V	
<ul> <li>Low Input Current of 1 μA Max</li> </ul>	5D [] 6 15 [] 5Q 6D [] 7 14 [] 6Q
Bus-Structured Pinout	7D [ 8 13] 7Q
	8D 9 12 8Q
	GND [ 10 11 ] LE
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### description/ordering information

This octal transparent D-type latch features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs respond to the data (D) inputs. When LE is low, the outputs are latched to retain the data that was set up.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

### **ORDERING INFORMATION<sup>†</sup>**

TA	PACKAGE <sup>‡</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SOIC – DW	Reel of 2500	SN74HC573AQDWRQ1	HC573AQ
–40°C to 125°C	TSSOP – PW	Reel of 2000	SN74HC573AQPWRQ1	HC573AQ

<sup>†</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

<sup>‡</sup>Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



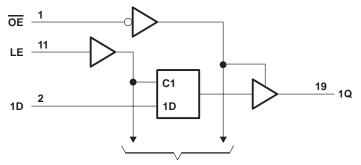
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## SN74HC573A-Q1 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

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FUNCTION TABLE (each latch)								
	OUTPUT							
OE	LE	D	Q					
L	Н	Н	Н					
L	Н	L	L					
L	L	Х	Q <sub>0</sub> Z					
Н	Х	Х	Z					

## logic diagram (positive logic)



To Seven Other Channels

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> ) (see Note 1)	
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	
Continuous current through V <sub>CC</sub> or GND	±70 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package	58°C/W
PW package	83°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



## SN74HC573A-Q1 **OCTAL TRANSPARENT D-TYPE LATCH** WITH 3-STATE OUTPUTS SCLS600A – NOVEMBER 2004 – REVISED APRIL 2008

## recommended operating conditions (see Note 3)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		2	5	6	V
		$V_{CC} = 2 V$	1.5			
VIH	High-level input voltage	$V_{CC} = 4.5 V$	3.15			V
		V <sub>CC</sub> = 6 V	4.2			
		$V_{CC} = 2 V$			0.5	
VIL	Low-level input voltage	$V_{CC} = 4.5 V$			1.35	V
		V <sub>CC</sub> = 6 V			1.8	
٧I	Input voltage		0		VCC	V
VO	Output voltage		0		VCC	V
		V <sub>CC</sub> = 2 V			1000	
tt	Input transition (rise and fall) time	$V_{CC} = 4.5 V$			500	ns
		V <sub>CC</sub> = 6 V			400	
Т <sub>А</sub>	Operating free-air temperature		-40		125	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		Vcc	T <sub>A</sub> = 25°C			T <sub>A</sub> = −40°C TO 125°C		T <sub>A</sub> = −40°C TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
			2 V	1.9	1.998		1.9		1.9		
		I <sub>OH</sub> = -20 μA	4.5 V	4.4	4.499		4.4		4.4		
∨он	$V_I = V_{IH} \text{ or } V_{IL}$		6 V	5.9	5.999		5.9		5.9		V
		$I_{OH} = -6 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
		I <sub>OH</sub> = -7.8 mA	6 V	5.48	5.8		5.2		5.34		
	V <sub>OL</sub> VI = VIH or VIL	l <sub>OL</sub> = 20 μA	2 V		0.002	0.1		0.1		0.1	
			4.5 V		0.001	0.1		0.1		0.1	
VOL			6 V		0.001	0.1		0.1		0.1	V
		I <sub>OL</sub> = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I <sub>OL</sub> = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
Ц	$V_{I} = V_{CC} \text{ or } 0$		6 V		±0.1	±100		±1000		±1000	nA
I <sub>OZ</sub>	$V_{O} = V_{CC} \text{ or } 0$		6 V		±0.01	±0.5		±10		±5	μΑ
ICC	$V_I = V_{CC} \text{ or } 0,$	IO = 0	6 V			8		160		80	μΑ
Ci			2 V to 6 V		3	10		10		10	pF



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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		Vcc	T <sub>A</sub> = 25°C		T <sub>A</sub> = −40°C TO 125°C		T <sub>A</sub> = −40°C TO 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
		2 V	80		120		100		
tw	Pulse duration, LE high	4.5 V	16		24		20		ns
		6 V	14		20		17		
		2 V	50		75		63		ns
t <sub>su</sub>	Setup time, data before LE $\downarrow$	4.5 V	10		15		13		
		6 V	9		13		11		
		2 V	20		24		24		
th	Hold time, data after LE $\downarrow$	4.5 V	5		5		5		ns
		6 V	5		5		5		

## switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	Vcc	Т	λ = 25°C	;	T <sub>A</sub> = - TO 12		T <sub>A</sub> = - TO 8		UNIT		
	(INPUT)					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
			2 V		77	175		265		220			
<sup>t</sup> pd	D	Q	4.5 V		26	35		53		44			
			6 V		23	30		45		38			
	LE		2 V		87	175		265		260	ns		
		Any Q	4.5 V		27	35		53		44			
							6 V		23	30		45	
		OE Any Q	2 V		68	150		225		190			
<sup>t</sup> en	OE		4.5 V		24	30		45		38	ns		
				6 V		21	26		38		32		
			2 V		47	150		225		190			
<sup>t</sup> dis	OE	Any Q	4.5 V		23	30		45		38	ns		
			, _		6 V		21	26		38		32	
			2 V		28	60		90		75			
tt		Any Q	4.5 V		8	12		18		15	ns		
			6 V		6	10		15		13			



## SN74HC573A-Q1 **OCTAL TRANSPARENT D-TYPE LATCH** WITH 3-STATE OUTPUTS SCLS600A - NOVEMBER 2004 - REVISED APRIL 2008

# switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	FROM TO (INPUT) (OUTPUT)	Vcc	T <sub>A</sub> = 25°C			T <sub>A</sub> = −40°C TO 125°C		T <sub>A</sub> = −40°C TO 85°C		UNIT
	(INPUT) (001PUT)			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
		Q	2 V		95	200		300		250	
<sup>t</sup> pd	D		4.5 V		33	40		60		50	
			6 V		21	34		51		43	
	LE	Any Q	2 V		103	225		335		285	ns
			4.5 V		33	45		67		57	
				6 V		29	38		57		48
			2 V		85	200		300		250	
<sup>t</sup> en	OE	Any Q	4.5 V		29	40		60		50	ns
		-	6 V		26	34		51		43	
	Any Q		2 V		60	210		315		265	
tt		Any Q	4.5 V		17	42		63		53	ns
			6 V		14	36		53		45	

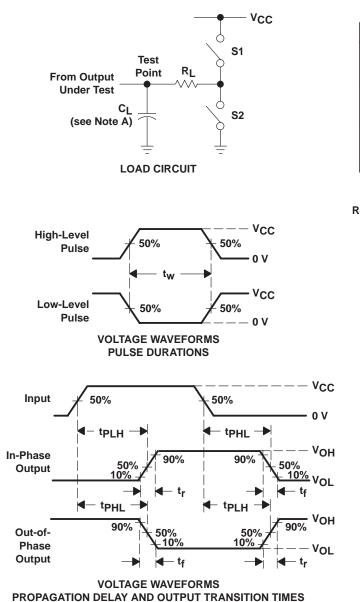
## operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
Cpd	Power dissipation capacitance per latch	No load	50	pF

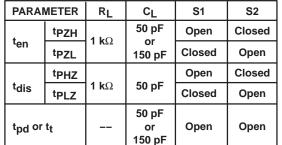


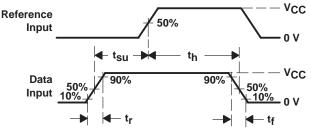
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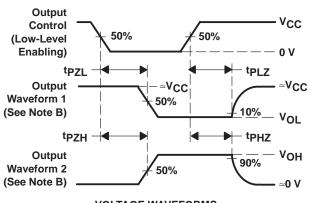


### PARAMETER MEASUREMENT INFORMATION



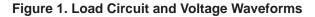


VOLTAGE WAVEFORMS SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

- NOTES: A. CL includes probe and test-fixture capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub> = 6 ns, t<sub>f</sub> = 6 ns.
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G. tPLH and tPHL are the same as tpd.





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#### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74HC573AQDWRQ1	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC573AQPWRG4Q1	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC573AQPWRQ1	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF SN74HC573A-Q1 :

Catalog: SN74HC573A

Military: SN54HC573A

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

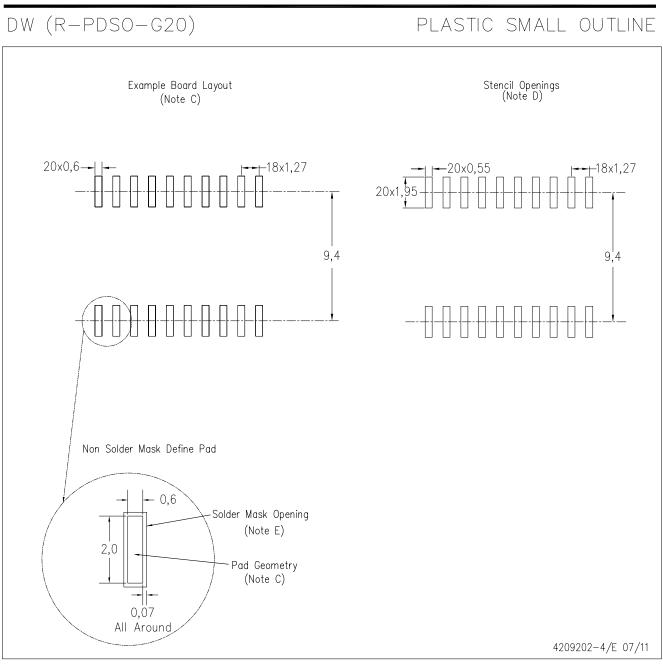
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AC.



## LAND PATTERN DATA



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  $\beta$ . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



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