SDLS006

D2634, JANUARY 1981 REVISED MARCH 1988

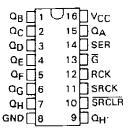
- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- Choice of 3-State ('LS595) or Open-Collector ('LS596) Parallel Outputs
- Shift Register Has Direct Clear
- Accurate Shift Frequency: DC to 20 MHz

description

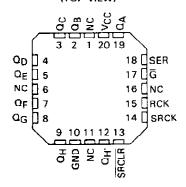
These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state ('LS595) or open-collector ('LS596) outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

SN54LS595, SN54LS596...J OR W PACKAGE SN74LS595, SN74LS596...N PACKAGE (TOP VIEW)

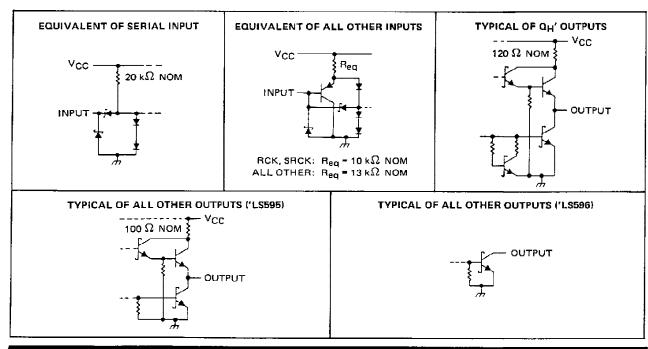


SN54LS595, SN54LS596 . . . FK PACKAGE (TOP VIEW)



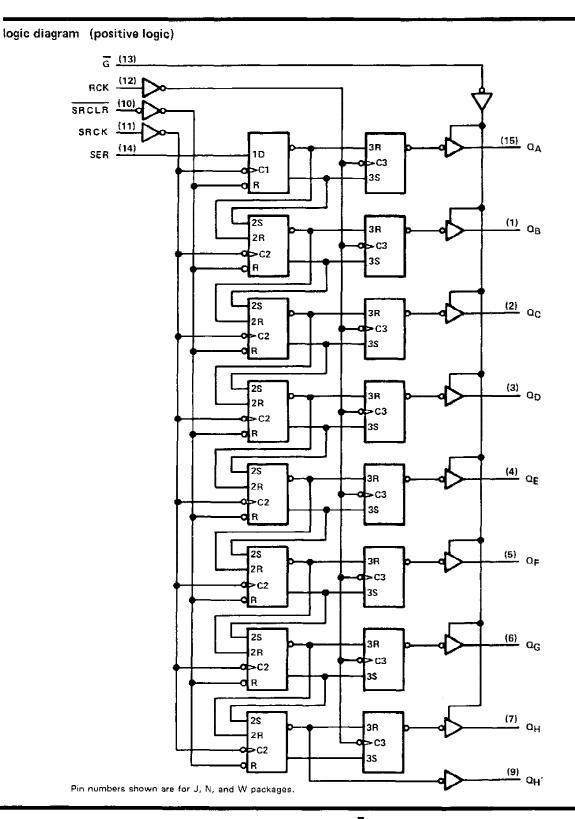
NC - No internal connection

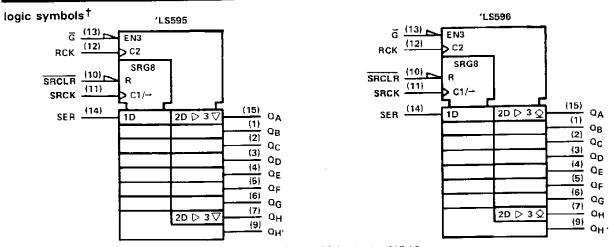
schematics of inputs and outputs



PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.







 $^{^{\}dagger}$ These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, Vcc (see Note 1)		
Input voltage		
Offictate output voltage		5.5 V
Operation free-air temperature range:	: SN54LS595.SN54LS596	55 C to 125 C
	SN741 S595, SN74LS596	0°C to /0°C
Storage temperature range		– 65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

				SN54LS	3'		SN74LS	s'	UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX	UNI	
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25		
ViH	High-level input voltage		2			2			V	
VIL	Low-level input voltage				0.7			0.8	V	
VOH	High-level output voltage	QA thru QH, 'LS596 only			5.5			5.5	٧	
		QH,			-1			<u>-1</u> m/	mA	
10H	High-level output current	Q _A thru Q _H , 'L\$595 only			- 1			- 2.6		
¹ OL	Low-level output current	OH'		8				16	mA	
		Q		_	12			24		
fSRCK	Shift clock frequency	1	0		20	0		20	МН	
tw(SRCK)	Duration of shift clock pulse		25			25			ns	
tw(RCK)	Duration of register clock pul	SE	20			20			ns	
tw(SRCLR)	Duration of shift clear pulse,	low level	20			20			ns	
77,0110 = 111		SRCLR inactive before SRCK 1	20			20			ns	
		SER before SRCK t	20			20				
t _{Sti}	Setup time	SRCK † before RCK † (see Note 2)				40] '''	
		SRCLR low before RCK t	40			40				
th	Hold time	SER after SRCK †	0			0			ns	
TA	Operating free-air temperatur	e	- 55		125	0		70	°C	

NOTE 2: This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together, in which case the storage register state will be one clock pulse behind the shift register.



SN54LS595, SN54LS596, SN74LS595, SN74LS596 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS †			SN54LS	;;		SN74LS	ş'	UNIT	
FARA	TAICIEN	I EST CONL	THOMS '	MIN	TYP#	MAX	MIN	TYP\$	MAX	OIGIT	
Vik		V _{CC} = MIN, I ₁ = - 18 mA				- 1.5			– 1.5	V	
	'LS595 Q	V _{CC} = MIN, V _{IH} = 2 V,	lOH = - 1 mA	2.4	3.2						
∨он		V)[= MAX	I _{OH} 2.6 mA	-			2.4	3.1		V	
	QH'		1 _{OH} = -1 mA	2.4	3.2		2.4	3.2			
IОН	'L\$596 Q	$V_{CC} = MIN, V_{IH} = 2 V, V_{I}$	L = MAX, V _{OH} = 5.5 V			0.1			0.1	mΑ	
	α		I _{OL} = 12 mA		0.25	0.4		0.25	0.4		
VOL		V _{CC} = MIN, V _{IH} = 2 V,	I _{OL} = 24 mA					0.35	0.5	v	
*UŁ	QH'	VIL = MAX	10L = 8 mA		0.25	0.4		0,25	0.4	•	
			I _{QL} ≈ 16 mA					0.35	0,5		
lozh	'LS595 Q	VCC = MAX, VIH = 2 V, VI	L = MAX, V _{OH} = 2.7 V			20			20	μA	
IOZL	'LS595 Q	VCC = MAX, VIH = 2 V, VI	L = MAX, VOH = 0.4 V			- 20			- 20	μА	
l ₁		VCC = MAX, VI = 7 V				0.1			0.1	mA	
ЧН		V _{CC} - MAX, V ₁ = 2.7 V				20			20	μА	
1	SER	Vcc = MAX, V1 = 0.4 V				- 0.4			- 0.4	mΑ	
1 L	All others	VCC MAX, V) "GA V	Ì		- 0.2			- 0.2	,117		
les X	'LS595 Q	V _{CC} = MAX, V _C = 0 V		- 30		130	- 30		- 130	^	
los §	Q _H ′	VCC - WAX, VO - 0 V		- 20		- 100	- 20		- 100	mA	
lance	'LS595	-			33	50		33	50	mΑ	
ICCH	'LS596	V _{CC} = MAX,			30	45		30	45	mA	
loo	'LS595	All possible inputs grounded,		_	42	65		42	65		
CCL	'LS596	All outputs open		36	55		36	55	mA		
¹ccz	'L S 595				44	65		44	65	mΑ	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions,

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

SN54LS595, SN54LS596, SN74LS595, SN74LS596 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

switching characteristics, VCC = 5 V, TA = 25° C (see note 3)

DADAMETER	FROM	то	TEST ODA	'LS595				UNIT			
PARAMETER	(INPUT)	(OUTPUT)	TEST CON	MIN	TYP	MAX	MIN	TYP	MAX	3,411	
tPLH	SRCK1		5 46	C _L = 30 pF		12	18		14	21	ns
^t PHL	SHUKT	QH'	R_{\perp} = 1k Ω ,			17	25		20	30	ns
^t PLH	RCK 1	Q _A thru Q _H		C _L = 45 pF	1	12	18		28	42	ns
^t PHL	, nck '	ag und da	R ₁ = 667 Ω,			24	35		24	35	ns
tPZH	Ğ↓	Q _A thru Q _H	11 - 007 12,			20	30				ns
tPZL	1 3 .	QA IIII GH				25	38				ns
^t PHZ	<u>G</u> ↑	O a show O	B 667 C	C _L = 5 pF		20	30				ns
tPLZ	1 3 '	Q _A thru Q _H	R _L = 667 Ω,			25	38				ns
tPLH .	Ğ١	Qд thru Qн	$R_1 = 667 \Omega_s$	0 45 5			·		40	60	ns
tPHL	Ğ∔	Q _A thru Q _H	1 11 - 00/12,	C _L = 45 pF					25	38	ns
^t PHL	SRCLR +	QH'	$R_{L} = 1 k\Omega$,	CL = 30 pF		24	35		24	35	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

5-Sep-2011

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login
5962-86717012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8671701EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
5962-8671701EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
5962-8671701FA	ACTIVE	CFP	W	16	1	TBD	Call TI	Call TI	
5962-8671701FA	ACTIVE	CFP	W	16	1	TBD	Call TI	Call TI	
SN54LS595J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN54LS595J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN74LS595D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS595D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS595DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS595DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS595DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS595DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS595DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS595DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS595DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS595DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS595DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS595DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS595N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS595N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	





www.ti.com 5-Sep-2011

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LS595N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	
SN74LS595N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	
SN74LS595NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS595NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS596D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	
SN74LS596D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	
SN74LS596N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS596N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS596NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS596NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SNJ54LS595FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS595FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS595J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54LS595J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54LS595W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
SNJ54LS595W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.





5-Sep-2011

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OTHER QUALIFIED VERSIONS OF SN54LS595, SN74LS595:

Catalog: SN74LS595

Military: SN54LS595

NOTE: Qualified Version Definitions:

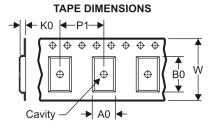
- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

www.ti.com 29-Jul-2009

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS595DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 29-Jul-2009



*All dimensions are nominal

Ī	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
	SN74LS595DR	SOIC	D	16	2500	333.2	345.9	28.6

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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OMAP Mobile Processors www.ti.com/omap

Interface

Wireless Connctivity www.ti.com/wirelessconnectivity

TI E2E Community Home Page <u>e2e.ti.com</u>

www.ti.com/security