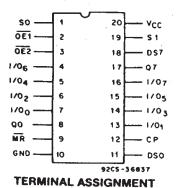


Data sheet acquired from Harris Semiconductor SCHS288



8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

CD54/74AC/ACT299 - Asynchronous Reset CD54/74AC/ACT323 - Synchronous Reset

Type Features:

- Buffered inputs
- Typical propagation delay: 6 ns @ Vcc = 5 V, T_A = 25° C, C_L = 50 pF

The RCA CD54/74AC299 and CD54/74AC323 and the CD54/74ACT299 and CD54/74ACT323 are 3-state, 8-input universal shift/storage registers with common parallel I/O pins. These devices use the RCA ADVANCED CMOS technology. These registers have four synchronous-operating modes controlled by the two select inputs as shown in the Mode Select (S0, S1) table. The Mode Select, the Serial Data (DSO, DS7), and the Parallel Data (I/O $_0$ - I/O $_7$) respond only to the LOW-TO-HIGH transition of the clock (CP) pulse. S0, S1 and Data inputs must be present one setup time prior to the positive transition of the clock.

With the CD54/74AC/ACT299, the Master Reset (MR) is an asynchronous active-LOW input. When MR is LOW, the register is cleared regardless of the status of all other inputs. With the CD54/74AC/ACT323, the Master Reset (MR) clears the register in sync with the clock input. The register can be expanded by cascading same units by tying the serial output (QO) to the serial data (DS7) input of the preceding register, and tying the serial output (Q7) to the serial data (DSO) input of the following register. Recirculating the (n x 8) bits is accomplished by tying the Q7 of the last stage to the DSO of the first stage.

The 3-state input/output (I/O) port has three modes of operation:

- Both Output Enable (OE1 and OE2) inputs are LOW and S0 or S1 or both are LOW; the data in the register is present at the eight outputs.
- When both S0 and S1 are HIGH, I/O terminals are in the high-impedance state but being input ports, ready for parallel data to be loaded into eight registers with one clock transition regardless of the status of OE1 and OE2.

Family Features:

- Exceeds 2-kV ESD Protection MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- ± 24-mA output drive current
 - Fanout to 15 FAST* ICs
 - Drives 50-ohm transmission lines

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

 Either one of the two Output Enable inputs being HIGH will force I/O terminals to be in the off state. It is noted that each I/O terminal is a 3-state output and a CMOS buffer input.

The CD74AC/ACT299 and CD74AC/ACT323 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT299 and CD54AC/ACT323, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

MODE SELECT — FUNCTION TABLE REGISTER OPERATING MODES

				INPUT	S			REGISTER OUTPUTS				
FUNCTION	MŘ	СР	S0	S1	DS0	DS7	I/O _n	Q0	Q1		Q6	Q 7
Reset (Clear)	L	X.	Х	Х	X	Х	Х	L	L		L	L
Shift Right	Н	— /_	h:	ı	Ī	Х	Х	L	qo		Q ₅	Q ₆
	н		h	1	h	×	×	Н	\mathbf{q}_{o}		q_5	Q_6
Shift Left	Н	-/-	1	h ·	X	1	X	q ₁	q ₂		Q7	L
•	H-		1	h	Х	h	Х	q ₁	q_2		q ₇	Н
Hold (do nothing)	Н	_/_	ı	1	Х	Х	Х	q _o	q,		Q ₆	Q ₇
Parallel Load	Н		h	h	X	X	I	L	L		L	L
	Н		h	h	Х	Х	h	Н	Н		Н	Н

^{*}On CD54/74AC/ACT323, CP must be in transition from the LOW-to-HIGH state to Reset (Clear).

MODE SELECT — FUNCTION TABLE 3-STATE I/O PORT OPERATING MODE

FUNCTION				INPUTS		INPUTS/OUTPUTS
FUNCTION	OE1	OE2	S0	S 1	Qn (Register)	I/O ₀ I/O ₇
Read Register	L	L	L	Х	L	L .
	L	L	L	X	Н	Н
	L	L	х	L	L	L
	L	L	x	L	Н	Н
Load Register	X	Х	Н	Н	Qn = 1/O _n	I/O _n = Inputs
Disable I/O	Н	Х	X	Х	X	(Z)
	×	н	х	X	Χ	(Z)

H = Input voltage high level.

h = Input voltage high one set-up time prior clock transition.

L = Input voltage low level.

I = Input voltage low one set-up time prior clock transition.

q_n = Lower case letters indicate the state of the referenced output one set-up time prior clock transition.

X = Voltage level on logic status don't care.

Z = Output in high-impedance state. = Low-to-high clock transition. 3-STATE CONTROL 13 -O 1/01 14 -O 1/03 3-STATE OUTPUTS BUS LINE BUS LINE 15 -O 1/05 16 -0 1/07 17 O Q7 STANDARD OUTPUT STANDARD OUTPUT QO so O MODE SELECTION 92CM-36996RI 050 O 18 GND 10

Fig. 1 - Functional diagram

MAXIMUM RATINGS, Absolute-Maximum Values:
DC SUPPLY-VOLTAGE (V _{CC}) -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{iK} (for $V_1 < -0.5$ V or $V_1 > V_{CC} + 0.5$ V)
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_0 (for $V_0 > -0.5$ V or $V_0 < V_{cc} + 0.5$ V) ±50 mA
DC V_{∞} or GROUND CURRENT (I_{∞} or I_{GND})
POWER DISSIPATION PER PACKAGE (P₀):
For $T_A = -55$ to $+100^{\circ}$ C (PACKAGE TYPE E)
For $T_A = +100$ to $+125$ °C (PACKAGE TYPE E)
For $T_A = -55$ to $+70$ °C (PACKAGE TYPE M)
For T _A = +70 to +125°C (PACKAGE TYPE M)
OPERATING-TEMPERATURE RANGE (T _A)55 to +125°C
STORAGE TEMPERATURE (Tsig)65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 \pm 1/32 in. (1.59 \pm 0.79 mm) from case for 10 s maximum+265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only +300°C
*For up to 4 outputs per device; add \pm 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERIOTICS	LIA	AITS	LIMITO
CHARACTERISTICS	MIN.	MAX.	UNITS
Supply-Voltage Range, V _{CC} *: (For T _A = Full Package-Temperature Range)	_		
AC Types ACT Types	1.5 4.5	5.5 5.5	V
DC Input or Output Voltage, V _i , V ₀	0	Vcc	V
Operating Temperature, T _A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

^{*}Unless otherwise specified, all voltages are referenced to ground.

Technical Data _

CD54/74AC299, CD54/74AC323 CD54/74ACT299, CD54/74ACT323

STATIC ELECTRICAL CHARACTERISTICS: AC Series

	 .					AMBIEN'	T TEMPE	RATURE	(T _A) - °	С	
CHARACTERIST	ICS	TEST COI	NDITIONS	V _{cc}	+	25	-40 t	o +85.	-55 to	+125	V V V μA
		V, (V)	l _o (mA)	(V)	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.]
High-Level Input Voltage	V _{IH}			1.5 3 5.5	1.2 2.1 3.85		1.2 2.1 3.85	=	1.2 2.1 3.85		V
Low-Level Input Voltage	ViL			1.5 3 5.5	_	0.3 0.9 1.65	_	0.3 0.9 1.65	_	0.3 0.9 1.65	V
High-Level Output			-0.05	1.5	1.4		1.4		1.4		
Voltage	V _{OH}	VIH	-0.05	3	2.9	l —	2.9	_	2.9	_]
		or	-0.05	4.5	4.4		4.4	_	4.4	_]
		V _{IL}	-4	3	2.58	_	2.48	_	2.4	_	\ \
			-24	4.5	3.94		3.8		3.7		
		#, * {	-75	5.5		_	3.85	_		_	
		" ' }	-50	5.5		_			3.85		
Low-Level Output			0.05	1.5	_	0.1		0.1	_	0.1	
Voltage	Vol	ViH	0.05	3	_	0.1		0.1		0.1	
		or	0.05	4.5	_	0.1		0.1		0.1]
		Vil	12	3		0.36	_	0.44		0.5	V
			24	4.5	_	0.36		0.44		0.5	
		#, * {	75	5.5		_		1.65			
		"· l	50	5.5			_			1.65	
Input Leakage Current	t ₁	V _{cc} or GND		5.5	_	±0.1		±1	_	±1	μА
3-Stage Leakage Current	loz	VIH Or VIL Vo= Vcc Or GND		5.5		±0.5	_	±5		±10	μΑ
Quiescent Supply Current, MSI	tcc	V _{cc} or GND	0	5.5	_	8	· <u>-</u>	80	-	160	μΑ

[#]Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

	***************************************				[,	AMBIEN	T TEMPE	RATURE	E (T _A) - °	С	
CHARACTERISTIC	cs	TEST CO	NDITIONS	V _{cc}	+:	25	-40 t	o +85	-55 to	+125	UNITS
		V, (V)	l _o (mA)	(V)	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V _{iH}			4.5 to 5.5	2	_	2	_	2	_	v
Low-Level Input Voltage	VIL			4.5 to 5.5		0.8	_	0.8	_	0.8	V
High-Level Output		V _{IH}	-0.05	4.5	4.4	<u> </u>	4.4	_	4.4	_	
Voltage	V _{OH}	or V _{IL}	-24	4.5	3.94		3.8		3.7	l –]
		#, * {	-75	5.5	_	_	3.85	_	_	_	1 v
		"' !	-50	5.5	_				3.85		
Low-Level Output		V _{IH}	0.05	4.5		0.1	–	0.1	-	0.1	
Voltage	Vol	or V _{IL}	24	4.5		0.36	_	0.44	_	0.5	v
		#, * {	75	5.5	_	_	_	1.65	_	_	
		", " [50	5.5		_			_	1.65	
Input Leakage Current	lı .	V _{cc} or GND		5.5		±0.1	_	±1		±1	μΑ
3-State Leakage Current	loz	V _{IH} or V _{IL} V _O or GND		5.5		±0.5		±5	_	±10	μΑ
Quiescent Supply Current, MSI	lcc	V _{cc} or GND	0	5.5	_	8	_	80	_	160	μΑ
Additional Quiescent S Current per Input Pin TTL Inputs High 1 Unit Load		V _{cc} -2.1		4.5 to 5.5		2.4		2.8	_	3	mA

[#]Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

ACT INPUT LOADING TABLE

14.00.17	UNIT LOADS*				
INPUT	299	323			
S1, S0, OE1, OE2	0.83	0.83			
1/O ₀ - 1/O ₇ , CP, DS0, DS7	0.67	0.67			
MR	1.33	0.67			

^{*}Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

THE STATE OF STATE OF

CD54/74AC299, CD54/74AC323 CD54/74ACT299, CD54/74ACT323

PREREQUISITE FOR SWITCHING: AC Series

			AMBI	ENT TEMPE	RATURE (1	'A) - °C	Ţ,
CHARACTERISTICS	SYMBOL	V _{cc}	-40 t	o +85	-55 to	+125	UNITS
		(V)	MIN.	MAX.	MIN.	MAX.	1
Setup Time S1, S0, to CP	tsu	1.5 3.3* 5†	99 11.1 7.9	=	113 12.6 9		ns
Hold Time S1, S0 to CP	tн	1.5 3.3 5	0 0	=	0 0		ns
Setup Time (I/O)n, DS0, DS7 to CP	t _{su}	1.5 3.3 5	49 5.5 3.9	-	56 6.3 4.5	-	ns
Hold Time (I/O)n, DS0, DS7 to CP	tsu	1.5 3.3 5	0 0 0		0 0 0	_ _ _	ns
Setup Time MR to CP (323)	tsu	1.5 3.3 5	61 6.8 4.8	=	69 7.8 5.5		ńs
Hold Time MR to CP (323)	ţн	1.5 3.3 5	0 0 0		0 0 0	_ _ _	ns
Maximum CP Frequency	fmax	1.5 3.3 5	9 78 108	=	8 68 95	— —	MHz
CP Pulse Width	tw	1.5 3.3 5	57 6.4 4.6		65 7.3 5.2		ns
MR Pulse Width	tw	1.5 3.3 5	55 6.1 4.4		63 7 5	<u>-</u>	ns
Recovery Time MR to CP 299	t _{REC}	1.5 3.3 5	55 6.1 4.4	<u>-</u> -	63 7 5	- - -	ns

*3.3 V: min. is @ 3 V †5 V: min is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

	.		AMBI	ENT TEMPE	RATURE (Γ _Λ) - °C	T
CHARACTERISTICS	SYMBOL	V _{cc}		o +85		0 +125	UNITS
		(V) .	MIN.	MAX.	MIN.	MAX.	7
Propagation Delays: CP to Q0, Q7	t _{PLH} t _{PHL}	1.5 3.3* 5†	4.7 3.3	147 16.5 11.7	 4.5 3.2	162 18.1 12.9	ns
CP to (I/O)n	t _{PLH} t _{PHL}	1.5 3.3 5	4.9 3.5	154 17.2 12.3	4.7 3.4	169 18.9 13.5	ns
MR to Q0, Q7 (299 only)	tpin tphi	1.5 3.3 5	- 4 2.9	127 14.3 10.2	 3.9 2.8	140 15.7 11.2	ns
MR to (I/O)n	telн teнl	1.5 3.3 5	5 3.6	158 17.7 12.6	 4.9 3.5	174 19.5 13.9	ns
Enable and Disable Times	tpzl tpzh tplz tphz	1.5 3.3 5	5.8 3.8	169 20.4 13.5	 5.6 3.7	186 22.4 14.9	ns
Power Dissipation Capacitance	C _{PD} §		280	Тур.	280	Тур.	pF
Input Capacitance	Cı	_	_	10		10	pF
3-State Output Capacitance	Co		_	15		15	pF

*3.3 V: min. is @ 3.6 V max. is @ 3 V

†5 V: min. is @ 5.5 V max. is @ 4.5 V $\ensuremath{\mbox{\$C}_{\mbox{\tiny PD}}}$ is used to determine the dynamic power consumption, per function.

 $P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where $f_i = input$ frequency

f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

PREREQUISITE FOR SWITCHING: ACT Series

		.,	AMBI	ENT TEMPI	ERATURE (T _A) - °C		
CHARACTERISTICS	SYMBOL	V _{cc} (V)		o +85	T	o +125	UNITS	
		(*/	MIN.	MAX.	MIN.	MAX.		
Setup Time S1, S0 to CP	tsu	5*	7.9	_	9	_	ns	
Hold Time S1, S0 to CP	ŧн	5	0	_	0	_	ns	
Setup Time (I/O)n, DS0, DS7 to CP	tsu	5	3.9	_	4.5	_	ns	
Hold Time (I/O)n, DS0, DS7 to CP	ŧн	5	0	_	0	_	ns	
Setup Time MR to CP (323)	tsu	5*	4.8		5.5	_	ns	
Hold Time MR to CP (323)	tн	5	0		0	_	ns	
Maximum CP Frequency	f _{max}	5	103	_	90		MHz	
CP Pulse Width	tw	5	4.8		5.5		ns	
MR Pulse Width	tw	5	4.4	_	5	_	ns	
Recovery Time MR to CP (299)	trec	5	4.4	_	5		ns	

^{*5} V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t, t, = 3 ns, CL = 50 pF

			AMBI	A) - °C			
CHARACTERISTICS	SYMBOL	V _{CC} (V)	-401	o +85	-55 to	+125	UNITS
		(')	MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Q0, Q7	t _{PLH} t _{PHL}	5*	3.3	11.7	3.2	12.9	ns
CP to (I/O)n	t _{PLH}	5	43.7	13.2	3.6	14.5	ns
MR to Q0, Q7 (299 only)	t _{PLH} t _{PHL}	5	3.1	11.1	3.1	12.2	ns
MR to (I/O)n	t _{PLH} t _{PHL}	5	4.8	16.9	4.7	18.6	ns
Enable and Disable Times	telz tenz tezl tezn	5	3.8	13.5	3.7	14.9	ns
Power Dissipation Capacitance	C _{PD} §	_	280	Тур.	280	Тур.	pF
Input Capacitance	Cı		—	10		10	pF
3-State Output Capacitance	Co			15		15	pF

*5 V: min. is @ 5.5 V max. is @ 4.5 V C_{PD} is used to determine the dynamic power consumption, per function. $P_D = C_{PD} V_{CC}^2 \, f_i + \Sigma \, (C_L V_{CC}^2 \, f_o) + V_{CC} \Delta I_{CC} \, \text{where} \quad f_i = \text{input frequency}$

f_o = output frequency C_L = output load capacitance

 V_{cc} = supply voltage.

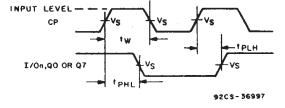


Fig. 2 - Clock prerequisite and propagation delays.

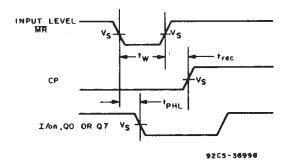


Fig. 3 - Master Reset prerequisite and propagation delays.

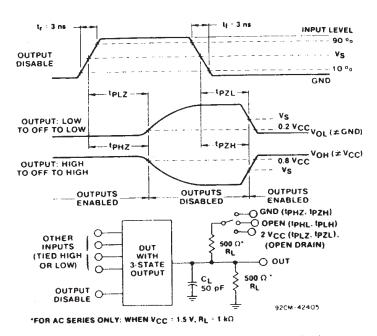


Fig. 4 - Three-state propagation delay times and test circuit.

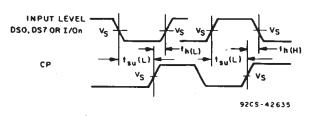


Fig. 5 - Data prerequisite times.

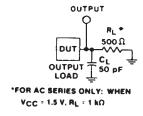


Fig. 6 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	Vcc	3 V
Input Switching Voltage, Vs	0.5 V _{cc}	1.5 V
Output Switching Voltage, Vs	0.5 V _{cc}	0.5 V _{CC}

PACKAGE OPTION ADDENDUM

www.ti.com 15-Oct-2009

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp (3)
CD54AC299F3A	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
CD54ACT299F3A	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
CD74AC299M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC299M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC299M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC323M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC323MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT299M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT299M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT299M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT299M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT299MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE OPTION ADDENDUM

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to Customer on an annual basis.



TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC299M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CD74ACT299M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC299M96	SOIC	DW	20	2000	346.0	346.0	41.0
CD74ACT299M96	SOIC	DW	20	2000	346.0	346.0	41.0

14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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