

# SN54F299, SN74F299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

SDFS071B – MARCH 1987 – REVISED APRIL 2004

The SN54F299 is obsolete and no longer supplied.

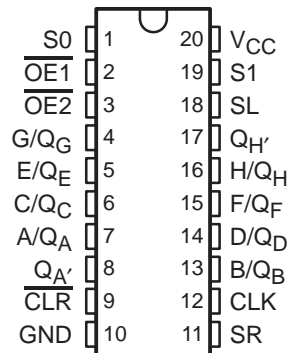
- **Four Modes of Operation:**
  - Hold (Store)
  - Shift Right
  - Shift Left
  - Load Data
- **Operates With Outputs Enabled or at High Impedance**
- **3-State Outputs Drive Bus Lines Directly**
- **Can Be Cascaded for N-Bit Word Lengths**
- **Direct Overriding Clear**
- **Applications:**
  - Stacked or Pushdown Registers
  - Buffer Storage
  - Accumulator Registers

## description/ordering information

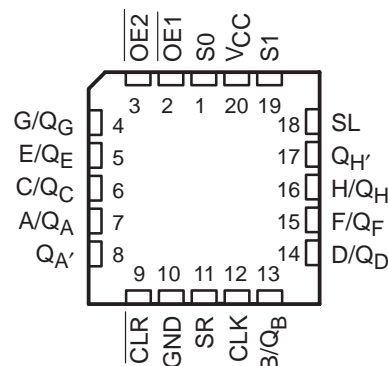
These 8-bit universal shift/storage registers feature multiplexed I/O ports to achieve full 8-bit data handling in a single 20-pin package. Two function-select ( $S_0, S_1$ ) inputs and two output-enable ( $\overline{OE1}, \overline{OE2}$ ) inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both  $S_0$  and  $S_1$  high. This places the 3-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs when the clear ( $\overline{CLR}$ ) input is low. Taking either  $\overline{OE1}$  or  $\overline{OE2}$  high disables the outputs but has no effect on clearing, shifting, or storage of data.

SN54F299 . . . J PACKAGE  
SN74F299 . . . DW, N, OR NS PACKAGE  
(TOP VIEW)



SN54F299 . . . FK PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube of 20	SN74F299N	SN74F299N
	SOIC – DW	Tube of 25	SN74F299DW	F299
		Reel of 2000	SN74F299DWR	
	SOP – NS	Reel of 2000	SN74F299NSR	74F299

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# SN54F299, SN74F299

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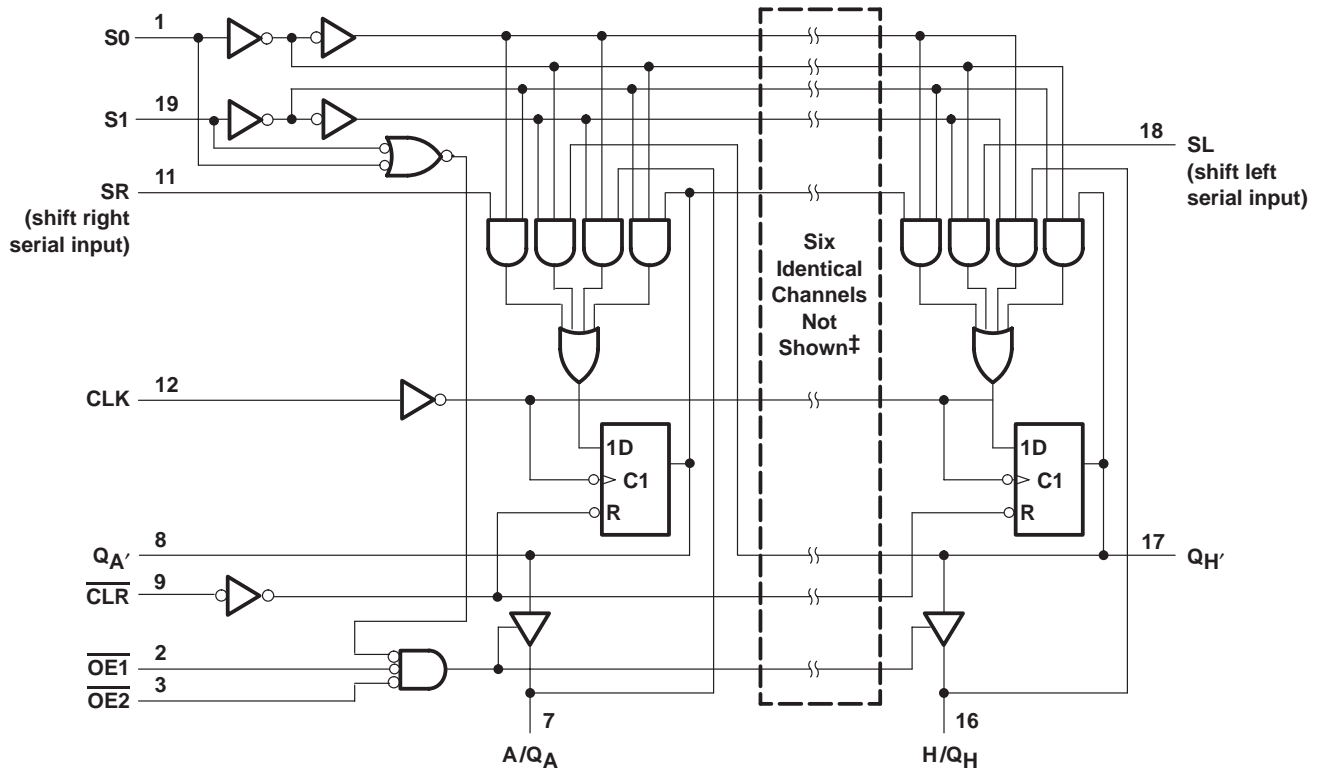
FUNCTION TABLE

MODE	INPUTS								I/O PORTS								OUTPUTS			
	CLR	S1	S0	OE1†	OE2†	CLK	SL	SR	A/QA	B/QB	C/QC	D/QD	E/QE	F/QF	G/QG	H/QH	QA'	QH'		
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0	QA0	QH0
	H	X	X	L	L	L	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0	QA0	QH0
Shift Right	H	L	H	L	L	↑	X	H	H	QAn	QBn	QCn	QDn	QEn	QFn	QGn	H	QGn	H	QGn
	H	L	H	L	L	↑	X	L	L	QAn	QBn	QCn	QDn	QEn	QFn	QGn	L	QGn	L	QGn
Shift Left	H	H	L	L	L	↑	H	X	QBn	QCn	QDn	QEn	QFn	QGn	QHn	H	QBn	H	QBn	H
	H	H	L	L	L	↑	L	X	QBn	QCn	QDn	QEn	QFn	QGn	QHn	L	QBn	L	QBn	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h	a	h

NOTE: a . . . h = the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

† When one or both output-enable inputs are high, the eight I/O terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

### logic diagram (positive logic)



‡ I/O ports not shown: B/QB (13), C/QC (6), D/QD (14), E/QE (5), F/QF (15), and G/QG (4).

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# SN54F299, SN74F299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–1.2 V to 7 V
Input current range .....	–30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state .....	–0.5 V to 5.5 V
Voltage range applied to any output in the high state .....	–0.5 V to $V_{CC}$
Current into any output in the low state: $Q_{A'}$ or $Q_{H'}$ .....	40 mA
SN54F299 ( $Q_A$ thru $Q_H$ ) .....	40 mA
SN74F299 ( $Q_A$ thru $Q_H$ ) .....	48 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package .....	58°C/W
N package .....	69°C/W
NS package .....	60°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input voltage ratings may be exceeded provided the input current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

		SN54F299			SN74F299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{IK}$	Input clamp current			–18			–18	mA
$I_{OH}$	High-level output current	$Q_{A'}$ or $Q_{H'}$		–1	$Q_{A'}$ or $Q_{H'}$		–1	mA
		$Q_A$ thru $Q_H$		–3	$Q_A$ thru $Q_H$		–3	
$I_{OL}$	Low-level output current	$Q_{A'}$ or $Q_{H'}$		20	$Q_{A'}$ or $Q_{H'}$		20	mA
		$Q_A$ thru $Q_H$		20	$Q_A$ thru $Q_H$		24	
$T_A$	Operating free-air temperature	–55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# SN54F299, SN74F299

## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F299			SN74F299			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA		-1.2			-1.2			V
V <sub>OH</sub>	Q <sub>A</sub> ' or Q <sub>H</sub> '	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -1 mA	2.5	3.4		2.5	3.4	V	
	Q <sub>A</sub> thru Q <sub>H</sub>		I <sub>OH</sub> = -1 mA	2.5	3.4		2.5	3.4		
			I <sub>OH</sub> = -3 mA	2.4	3.3		2.4	3.3		
Any output		V <sub>CC</sub> = 4.75 V,	I <sub>OH</sub> = -1 mA to -3 mA				2.7			
V <sub>OL</sub>	Q <sub>A</sub> ' or Q <sub>H</sub> '	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 20 mA	0.3		0.5	0.3		0.5	V
	Q <sub>A</sub> thru Q <sub>H</sub>		I <sub>OL</sub> = 20 mA	0.3		0.5				
			I <sub>OL</sub> = 24 mA				0.35	0.5		
I <sub>I</sub>	A thru H	V <sub>CC</sub> = 5.5 V	V <sub>I</sub> = 5.5 V	1			1			mA
	Any other		V <sub>I</sub> = 7 V	0.1			0.1			
I <sub>IH</sub> ‡	A thru H	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V	70			70			μA
	Any other			20			20			
I <sub>IL</sub> ‡	A thru H	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.5 V	-0.65			-0.65			mA
	S0 or S1			-1.2			-1.2			
	Any other			-0.6			-0.6			
I <sub>OS</sub> §		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0	-60	-150		-60	-150		mA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V,	See Note 4	68		95	68		95	mA

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ For I/O ports (Q<sub>A</sub> thru Q<sub>H</sub>), the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 4: I<sub>CC</sub> is measured with  $\overline{OE1}$ ,  $\overline{OE2}$ , and CLK at 4.5 V.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54F299		SN74F299		UNIT	
				'F299							
				MIN	MAX	MIN	MAX	MIN	MAX		
f <sub>clock</sub>	Clock frequency			70		65		70		MHz	
t <sub>w</sub>	Pulse duration		CLK high or low		7		8		7		ns
			$\overline{CLR}$ low		7		8		7		
t <sub>su</sub>	Setup time before CLK↑		S0 or S1	High or low	8.5		9.5		8.5		ns
			A/Q <sub>A</sub> thru H/Q <sub>H</sub> , SR, or SL		High or low	5.5		6.5		5.5	
	Inactive-state setup time before CLK↑†		$\overline{CLR}$	High	7		13		7		
t <sub>h</sub>	Hold time after CLK↑		S0 or S1	High or low	0		0		0		ns
			A/Q <sub>A</sub> thru H/Q <sub>H</sub> , SR, or SL		High or low	2		2		2	

† Inactive-state setup time also is referred to as recovery time.



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## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = 25°C			V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			'F299			SN54F299		SN74F299		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			70	100		65		70	MHz	
t <sub>PLH</sub>	CLK	Q <sub>A</sub> ' or Q <sub>H</sub> '	3.2	6.6	9	2.7	10.5	3.2	10	ns
t <sub>PHL</sub>			2.7	6.1	8.5	2.2	10	2.7	9.5	
t <sub>PLH</sub>	CLK	Q <sub>A</sub> thru Q <sub>H</sub>	3.2	6.6	9	2.7	11	3.2	10	ns
t <sub>PHL</sub>			4.2	8.1	11	3.7	12.5	4.2	12	
t <sub>PHL</sub>	$\overline{\text{CLR}}$	Q <sub>A</sub> ' or Q <sub>H</sub> '	3.7	7.1	9.5	3.2	11.5	3.7	10.5	ns
		Q <sub>A</sub> thru Q <sub>H</sub>	5.7	10.6	14	5	15.5	5.7	15	
t <sub>PZH</sub>	$\overline{\text{OE1}}$ or $\overline{\text{OE2}}$	Q <sub>A</sub> thru Q <sub>H</sub>	2.7	5.6	8	2.2	10.5	2.7	9	ns
t <sub>PZL</sub>			3.2	6.6	10	2.7	12	3.2	11	
t <sub>PHZ</sub>	$\overline{\text{OE1}}$ or $\overline{\text{OE2}}$	Q <sub>A</sub> thru Q <sub>H</sub>	1.7	4.1	6	1.7	9	1.7	7	ns
t <sub>PLZ</sub>			1.2	3.6	5.5	1.2	7.5	1.2	6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

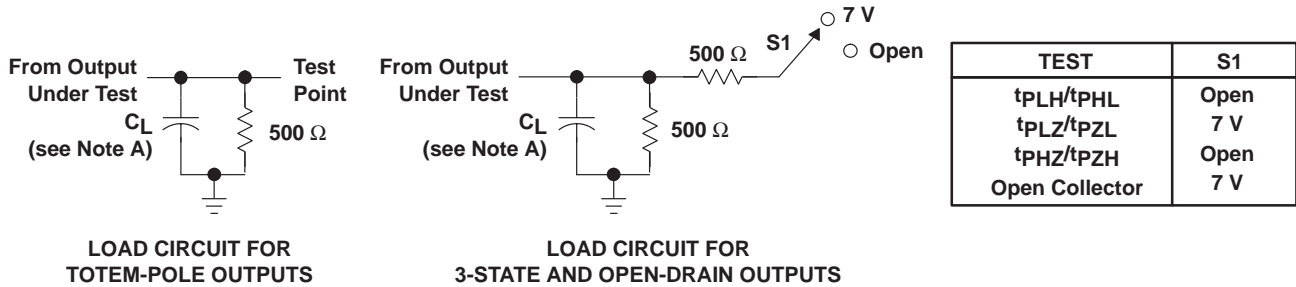


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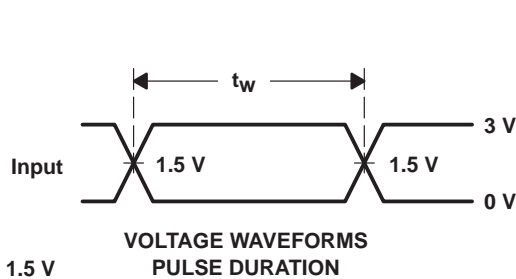
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## PARAMETER MEASUREMENT INFORMATION

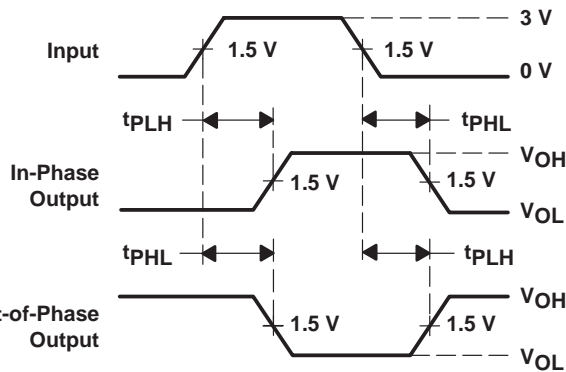
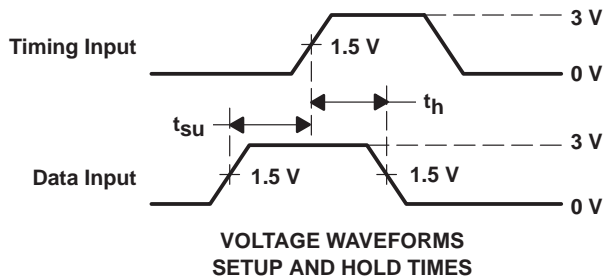


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

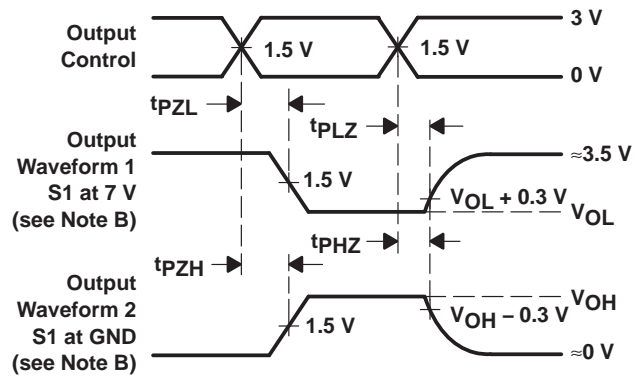
LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



1.5 V



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns, duty cycle = 50%.
  - The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74F299DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F299DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F299DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F299DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F299DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F299N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74F299N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	
SN74F299NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F299DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F299DWR	SOIC	DW	20	2000	346.0	346.0	41.0

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DW (R-PDSO-G20)

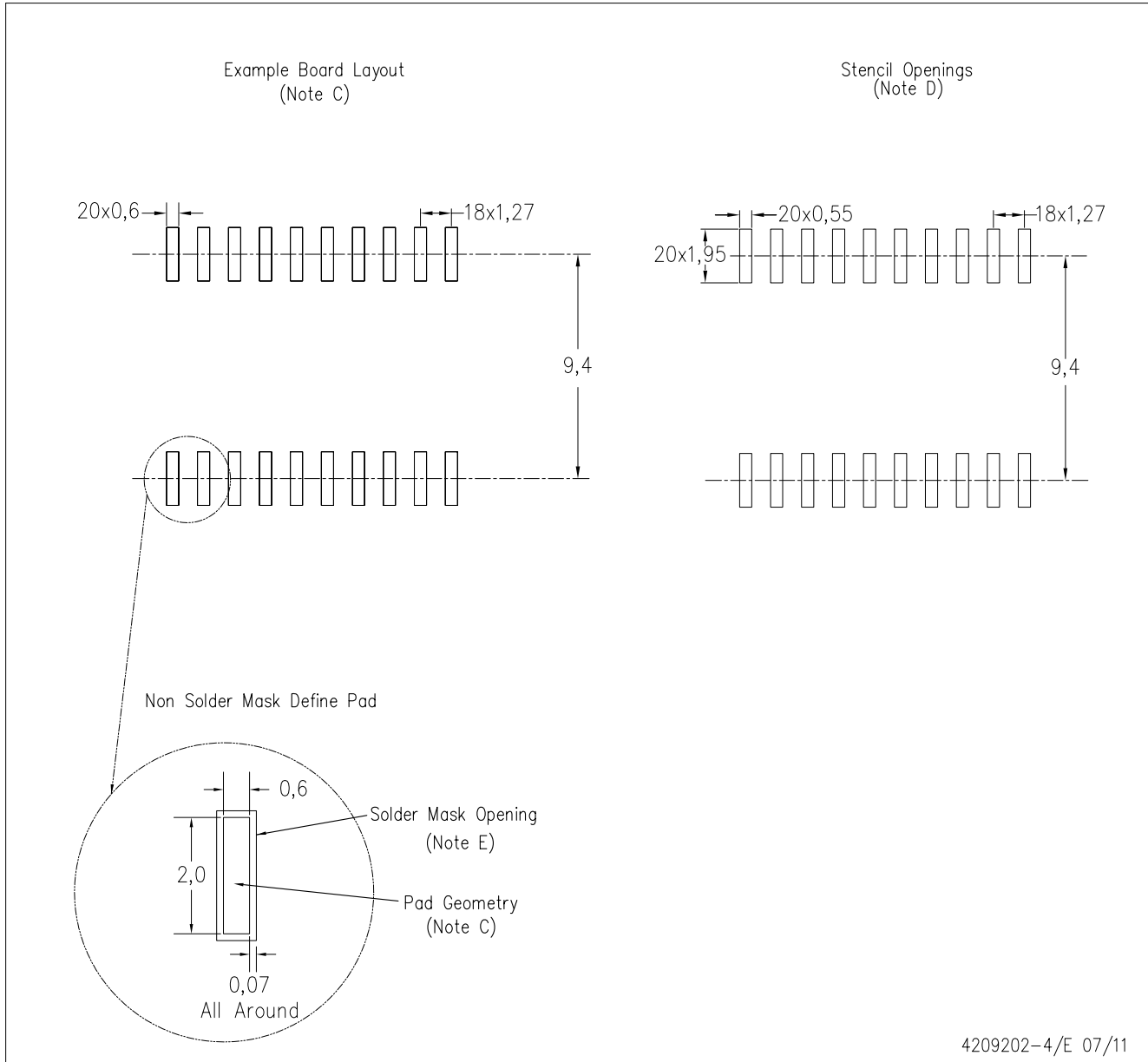
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4209202-4/E 07/11

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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