## SN54ALS299, SN74ALS299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

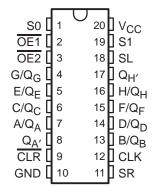
SDAS220B - DECEMBER 1982 - REVISED DECEMBER 1994

- Multiplexed I/O Ports Provide Improved Bit Density
- Four Modes of Operation:
  - Hold (Store)
  - Shift Right
  - Shift Left
  - Load Data
- Operate With Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for n-Bit Word Lengths
- Direct Overriding Clear
- Applications:
  - Stacked or Push-Down Registers
  - Buffer Storage
  - Accumulator Registers
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

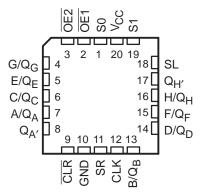
#### description

These 8-bit universal shift/storage registers feature multiplexed I/O ports to achieve full 8-bit data handling in a single 20-pin package. Two function-select (S0, S1) inputs and two outputenable (OE1, OE2) inputs can be used to choose the modes of operation listed in the function table.

SN54ALS299 . . . J PACKAGE SN74ALS299 . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS299 . . . FK PACKAGE (TOP VIEW)



Synchronous parallel loading is accomplished by taking both S0 and S1 high. This places the 3-state outputs in the high-impedance state and permits data applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously when the clear (CLR) input is low. Taking either OE1 or OE2 high disables the outputs, but has no effect on clearing, shifting, or storing data.

The SN54ALS299 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to  $125^{\circ}$ C. The SN74ALS299 is characterized for operation from  $0^{\circ}$ C to  $70^{\circ}$ C.

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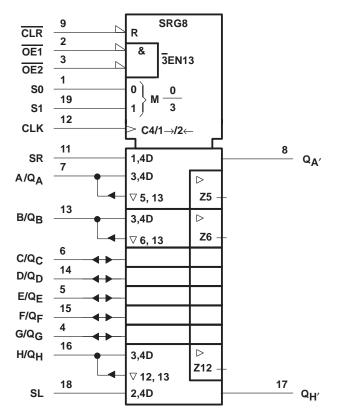
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#### **FUNCTION TABLE**

MODE				INP	JTS				I/O PORTS							OUTI	PUTS	
MODE	CLR	S1	S0	OE1†	OE2†	CLK	SL	SR	A/Q <sub>A</sub>	B/QB	C/QC	D/QD	E/QE	F/Q <sub>F</sub>	G/Q <sub>G</sub>	H/Q <sub>H</sub>	$Q_{A'}$	$Q_{H'}$
Clear	L L L	X L H	L X H	L L X	L L X	X X X	X X X	X X X	L L X	L L L	Г Г							
Hold	H H	L X	L X	L L	L L	X L	X X	X X	Q <sub>A0</sub> Q <sub>A0</sub>	Q <sub>B0</sub> Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub> Q <sub>D0</sub>	Q <sub>E0</sub> Q <sub>E0</sub>	Q <sub>F0</sub> Q <sub>F0</sub>	Q <sub>G0</sub> Q <sub>G0</sub>	Q <sub>H0</sub> Q <sub>H0</sub>	Q <sub>A0</sub> Q <sub>A0</sub>	Q <sub>H0</sub> Q <sub>H0</sub>
Shift Right	H H	L L	H H	L L	L L	<b>↑</b>	X X	H L	H L	Q <sub>An</sub> Q <sub>An</sub>	Q <sub>Bn</sub> Q <sub>Bn</sub>	Q <sub>Cn</sub> Q <sub>Cn</sub>	Q <sub>Dn</sub> Q <sub>Dn</sub>	Q <sub>En</sub> Q <sub>En</sub>	Q <sub>Fn</sub> Q <sub>Fn</sub>	Q <sub>Gn</sub> Q <sub>Gn</sub>	H L	Q <sub>Gn</sub> Q <sub>Gn</sub>
Shift Left	H H	H H	L L	L L	L L	↑ ↑	H L	X X	Q <sub>Bn</sub> Q <sub>Bn</sub>	Q <sub>Cn</sub> Q <sub>Cn</sub>	Q <sub>Dn</sub> Q <sub>Dn</sub>	Q <sub>En</sub> Q <sub>En</sub>	Q <sub>Fn</sub> Q <sub>Fn</sub>	Q <sub>Gn</sub> Q <sub>Gn</sub>	Q <sub>Hn</sub> Q <sub>Hn</sub>	H L	Q <sub>Bn</sub> Q <sub>Bn</sub>	H L
Load	Н	Н	Н	Χ	Χ	1	Х	Χ	а	b	С	d	е	f	g	h	а	h

NOTE: a . . . h = the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

## logic symbol‡



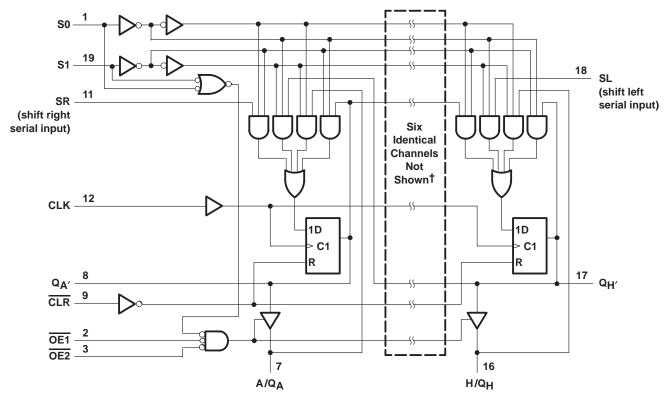
<sup>&</sup>lt;sup>‡</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



<sup>†</sup> When one or both output-enable inputs are high, the eight I/O terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

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## logic diagram (positive logic)



 $\dagger$  I/O ports not shown: B/QB (13), C/QC (6), D/QD (14), E/QE (5), F/QF (15), and G/QG (4).

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V <sub>CC</sub>		7 V
Input voltage, V <sub>I</sub> : All inputs		7 V
I/O ports		5.5 V
Operating free-air temperature range, T <sub>A</sub> : \$	SN54ALS299	. −55°C to 125°C
	SN74ALS299	0°C to 70°C
Storage temperature range		. −65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## SN54ALS299, SN74ALS299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

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### recommended operating conditions

			SN	54ALS2	99	SN	74ALS2	99	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
la	High-level output current	Q <sub>A</sub> ' or Q <sub>H</sub> '			-0.4			-0.4	mA
IOH	r light-level output current	$Q_A - Q_H$			-1			-2.6	IIIA
la.	Low lovel output current	Q <sub>A</sub> ' or Q <sub>H</sub> '			4			8	mA
IOL	Low-level output current	Q <sub>A</sub> – Q <sub>H</sub>			12			24	IIIA
TA	Operating free-air temperature		-55		125	0		70	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	ARAMETER	TEST CO	MOITIONS	SN	54ALS2	99	SN	74ALS2	99	UNIT
	ARAWETER	1251 00	NDITIONS	MIN	TYP†	MAX	MIN	TYP <sup>†</sup>	MAX	UNII
٧ıK		V <sub>CC</sub> = 4.5 V,	$I_{I} = -18 \text{ mA}$			-1.5			-1.5	V
	All outputs	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V <sub>CC</sub> -2	2		V <sub>CC</sub> -2	2		
Vон	Q <sub>A</sub> – Q <sub>H</sub>	V <sub>CC</sub> = 4.5 V	$I_{OH} = -1 \text{ mA}$	2.4	3.3					V
	QA - QH	VCC = 4.5 V	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
V <sub>OL</sub>	Q <sub>A</sub> ' or Q <sub>H</sub> '	V <sub>CC</sub> = 4.5 V	$I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	
	QA' OI QH'	VCC = 4.5 V	$I_{OL} = 8 \text{ mA}$					0.35	0.5	V
	Q <sub>A</sub> – Q <sub>H</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 12 mA		0.25	0.4		0.25	0.4	V
	QA - QH	VCC = 4.5 V	I <sub>OL</sub> = 24 mA					0.35	0.5	
1.	A – H	V <sub>CC</sub> = 5.5 V	V <sub>I</sub> = 5.5 V			0.1			0.1	mA
Ħ	Any others	VCC = 5.5 V	V <sub>I</sub> = 7 V			0.1			0.1	IIIA
l <sub>IH</sub> ‡		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			20			20	μΑ
. +	S0, S1, SR, SL	V 55V	V: 0.4.V			-0.2			-0.2	A
I <sub>IL</sub> ‡	Any others	$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = 0.4 V			-0.1			-0.1	mA
	Q <sub>A</sub> ' or Q <sub>H</sub> '	Vac 55V	Va 2.25 V	-15		-70	-15		-70	mA
IO§	Q <sub>A</sub> – Q <sub>H</sub>	V <sub>CC</sub> = 5.5 V,	$V_0 = 2.25 \text{ V}$	-20		-112	-30		-112	mA
			Outputs high		15	28		15	28	
ICC		V <sub>CC</sub> = 5.5 V	Outputs low		22	38		22	38	mA
			Outputs disabled		23	40		23	40	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

 $<sup>\</sup>ddagger$  For I/O ports (Q<sub>A</sub>-Q<sub>H</sub>), the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

<sup>\$</sup> The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

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# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				SN54A	LS299	SN74A	LS299	UNIT
				MIN	MAX	MIN	MAX	UNIT
fclock	Clock frequency (at 50% duty cycle)			0	17	0	30	MHz
	Pulse duration	CLK high or low		22		16.5		
t <sub>W</sub>	Fulse duration	CLR low	12		10		ns	
		S0 or S1	25		20			
l.	Setup time before CLK↑	0	High	18		16		
t <sub>su</sub>		Serial or parallel data	15		6		ns	
	Inactive-state setup time before CLK↑†	CLR	15		15			
+.	Hold time after CLK↑	S0 or S1	0		0			
<sup>t</sup> h	Hold time after CLK	Serial or parallel data		0		0		ns

<sup>†</sup> Inactive-state setup time is also referred to as recovery time.

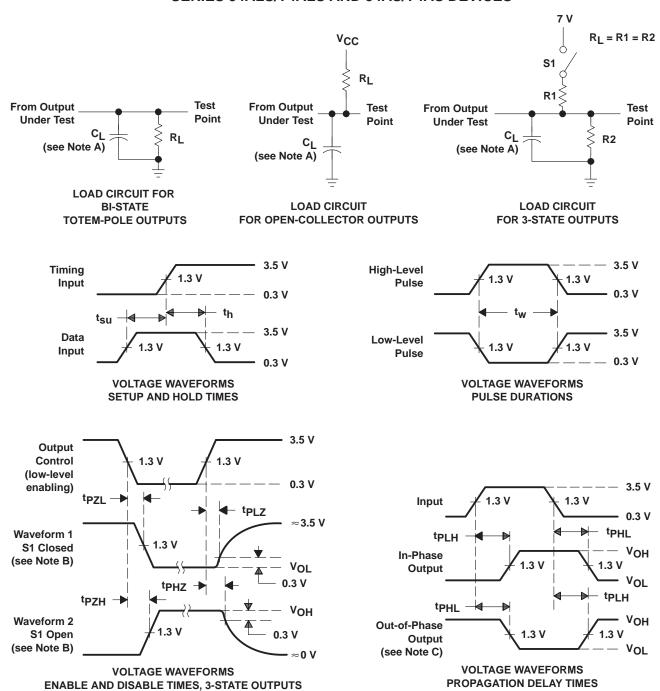
#### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C <sub>L</sub> R1 R2	= 50 pF = 500 £ = 500 £	2,		UNIT
			SN54A	LS299	SN74A		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>			17		30		MHz
<sup>t</sup> PLH	CLK	0.00	2	19	4	13	ns
<sup>t</sup> PHL	CLK	Q <sub>A</sub> –Q <sub>H</sub>	4	25	7	19	ris
t <sub>PLH</sub>	CLK	00**0	2	21	5	15	ns
t <sub>PHL</sub>	CLK	Q <sub>A</sub> ′ or Q <sub>H</sub> ′	4	25	8	18	115
4	CLR	Q <sub>A</sub> -Q <sub>H</sub>	6	29	6	22	20
<sup>t</sup> PHL	CLR	Q <sub>A</sub> ′ or Q <sub>H</sub> ′	6	29	6	22	ns
<sup>t</sup> PZH	OE1, OE2	0 0	5	22	6	16	ns
t <sub>PZL</sub>	OE1, OE2	$Q_A-Q_H$	6	27	8	22	115
<sup>t</sup> PZH	CO C4	0 . 0	5	27	7	17	ns
tPZL	S0, S1	$Q_A-Q_H$	6	26	8	22	115
t <sub>PHZ</sub>	OF4 OF2	0.0.	1	15	1	8	20
t <sub>PLZ</sub>	OE1, OE2	$Q_A-Q_H$	4	38	5	15	ns
<sup>t</sup> PHZ	S0, S1	Q <sub>A</sub> -Q <sub>H</sub>	1	16	1	12	ns
<sup>t</sup> PLZ	30, 31	ΨΑ <sup>-</sup> ΨΗ	4	34	8	25	115

<sup>‡</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR  $\leq$  1 MHz,  $t_{\Gamma}$  =  $t_{f}$  = 2 ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



5-Sep-2011

#### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
83021012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
8302101RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
8302101SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
SN54ALS299J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SN74ALS299DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS299DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS299DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS299DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS299DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS299DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS299N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS299NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS299NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS299NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS299NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54ALS299FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54ALS299J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SNJ54ALS299W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	

<sup>(1)</sup> The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.



## PACKAGE OPTION ADDENDUM

5-Sep-2011

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF SN54ALS299, SN74ALS299:

Catalog: SN74ALS299

www.ti.com

Military: SN54ALS299

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications



#### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS299DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74ALS299NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1





\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS299DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74ALS299NSR	SO	NS	20	2000	346.0	346.0	41.0

## 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## W (R-GDFP-F20)

## CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

### PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



### **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

## 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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