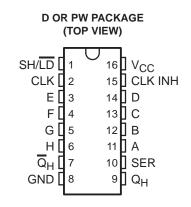
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- Controlled Baseline
 One Assembly/Test Site, One Fabrication
- Site Extended Temperature Performance of Lin
- Extended Temperature Performance of Up To -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree[†]
- 2-V to 6-V V_{CC} Operation
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80-μA Max I_{CC}
- Typical t_{pd} = 13 ns

[†] Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

description/ordering information

- ±4-mA Output Drive at 5 V
- Low Input Current of 1 μA Max
- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion



The SN74HC165 is an 8-bit parallel-load shift register that, when clocked, shifts the data toward a serial (Q_H) output. Parallel-in access to each stage is provided by eight individual direct data (A–H) inputs that are enabled by a low level at the shift/load (SH/LD) input. The SN74HC165 device also features a clock-inhibit (CLK INH) function and a complementary serial (\overline{Q}_H) output.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/LD is held high and CLK INH is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH also accomplish clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/LD is held high. While SH/LD is low, the parallel inputs to the register are enabled independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

TA	PACKAGE [‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
4000 10 40500	SOIC – D	Tape and reel	SN74HC165QDREP	HC165EP
–40°C to 125°C	TSSOP – PW	Tape and reel	SN74HC165QPWREP	HC165EP
–55°C to 125°C	SOIC – D	Tape and reel	SN74HC165MDREP	HC165MEP

ORDERING INFORMATION

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

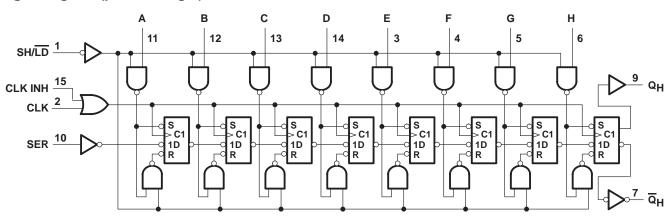


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FUNCTION TABLE										
	INPUT									
SH/LD	CLK	CLK INH	FUNCTION							
L	Х	Х	Parallel load							
н	Н	Х	No change							
н	Х	Н	No change							
н	L	\uparrow	Shift [†]							
н	\uparrow	L	Shift [†]							

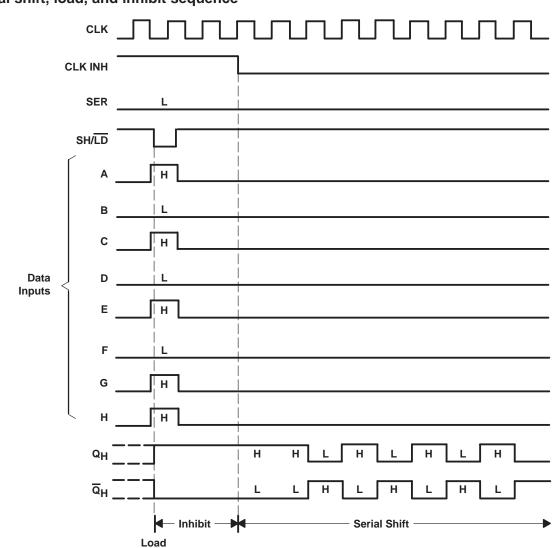
[†] Shift = content of each internal register shifts toward serial output Q_H. Data at SER is shifted into the first register.



logic diagram (positive logic)



SCLS473A - APRIL 2003 - REVISED JANUARY 2004



typical shift, load, and inhibit sequence



SCLS473A - APRIL 2003 - REVISED JANUARY 2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	
Output clamp current, I_{OK} (V _O < 0 or V _O > V _{CC}) (see Note 1)	
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Package thermal impedance, θ _{JA} (see Note 2):D package	73°C/W
PW package	108°C/W
Storage temperature range, T _{stg}	. −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	NOM	MAX	UNIT	
VCC	Supply voltage		2	5	6	V	
		$V_{CC} = 2 V$	1.5				
VIH	High-level input voltage	$V_{CC} = 4.5 V$	3.15			V	
		$V_{CC} = 6 V$	4.2				
		$V_{CC} = 2 V$			0.5		
VIL	Low-level input voltage	$V_{CC} = 4.5 V$			1.35	V	
		$V_{CC} = 6 V$			1.8		
VI	Input voltage		0		VCC	V	
VO	Output voltage		0		VCC	V	
		$V_{CC} = 2 V$			1000		
$\Delta t / \Delta v^{\ddagger}$	Input transition rise/fall time	$V_{CC} = 4.5 V$			500	ns	
		VCC = 6 V			400		
т.	Operating free or temperature	Q-suffix device	-40		125	°C	
Τ _Α	Operating free-air temperature	M-suffix device	-55		125	ъС	

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

[‡] If this device is used in the threshold region (from $V_{IL}max = 0.5$ V to $V_{IH}min = 1.5$ V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_t = 1000$ ns and $V_{CC} = 2$ V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.



SCLS473A - APRIL 2003 - REVISED JANUARY 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		V	Т	A = 25°C	;			
PARAMETER	TEST CONDITI	ONS	VCC	MIN	TYP	MAX	MIN	MAX	UNIT
			2 V	1.9	1.998		1.9		
		l _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		
∨он	$V_I = V_{IH} \text{ or } V_{IL}$		6 V	5.9	5.999		5.9		V
		$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.7		
		$I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.8		5.2		
		l _{OL} = 20 μA	2 V		0.002	0.1		0.1	
			4.5 V		0.001	0.1		0.1	
VOL	VI = VIH or VIL		6 V		0.001	0.1		0.1	V
		$I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26		0.4	
		I _{OL} = 5.2 mA	6 V		0.15	0.26		0.4	
Ц	$V_{I} = V_{CC} \text{ or } 0$		6 V		±0.1	±100		±1000	nA
Icc	$V_{I} = V_{CC} \text{ or } 0,$	IO = 0	6 V			8		160	μA
Ci			2 V to 6 V		3	10		10	pF



SCLS473A - APRIL 2003 - REVISED JANUARY 2004

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			VCC	T _A = 25°0		MIN	MAX	UNIT
				MIN M	AX	WIIIN	IIIAA	UNIT
			2 V		6		4.2	
^f clock	Clock frequency		4.5 V		31		21	MHz
			6 V		36		25	
			2 V	80		120		
		SH/LD low	4.5 V	16		24		
tw	Pulse duration		6 V	14		20		ns
٩			2 V	80		120		115
		CLK high or low	4.5 V	16		24		
			6 V	14		20		
			2 V	80		120		
		SH/LD high before CLK↑	4.5 V	16		24		
			6 V	14		20		
			2 V	40		60		
		SER before CLK↑	4.5 V	8		12		
				7		10		
				100		150		
t _{su}	Setup time	CLK INH low before CLK↑	4.5 V	20		30		ns
			6 V	17		25		
			2 V	40		60		
		CLK INH high before CLK1	4.5 V	8		12		
			6 V	7		10		
			2 V	100		150		
		Data before SH/LD \downarrow	4.5 V	20		30		
			6 V	17		26		
			2 V	5		5		
		SER data after CLK1	4.5 V	5		5		ns
+.	Hold time		6 V	5		5		
^t h			2 V	5		5		
		PAR data after SH/LD \downarrow	4.5 V	5		5		
			6 V	5		5		



SCLS473A - APRIL 2003 - REVISED JANUARY 2004

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

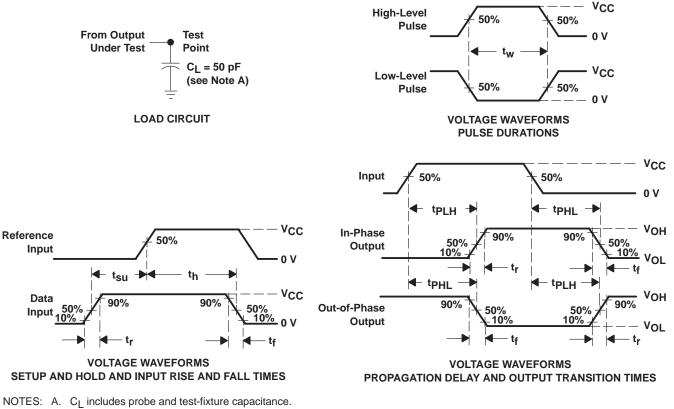
DADAMETER	FROM	то		T,	ຊ = 25 °C	;			
PARAMETER	(INPUT)	(OUTPUT)	VCC	MIN	TYP	MAX	MIN	MAX	UNIT
			2 V	6	13		4.2		
fmax			4.5 V	31	50		21		MHz
			6 V	36	62		25		
SH/LD			2 V		80	150		225	
	Q _H or Q _H	4.5 V		20	30		45		
			6 V		16	26		38	
	CLK	Q _H or Q _H	2 V		75	150		225	ns
^t pd			4.5 V		15	30		45	
			6 V		13	26		38	
			2 V		75	150		225	
	н	Q _H or Q _H	4.5 V		15	30		45	1
			6 V		13	26		38	
			2 V		38	75		110	
tt		Any	4.5 V		8	15		22	ns
			6 V		6	13		19	

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
Cpd	Power dissipation capacitance	No load	75	pF



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PARAMETER MEASUREMENT INFORMATION

- - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_r = 6 ns, t_f = 6 ns.
 - C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74HC165QDREP	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC165QPWREP	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04689-01XE	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04689-01YE	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74HC165-EP :

- Catalog: SN74HC165
- Automotive: SN74HC165-Q1
- Military: SN54HC165

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military QML certified for Military and Defense Applications

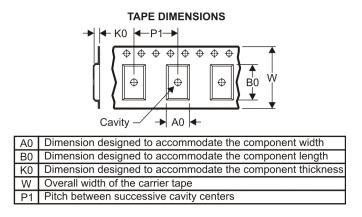
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC165QDREP	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC165QPWREP	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

30-Jul-2010



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC165QDREP	SOIC	D	16	2500	333.2	345.9	28.6
SN74HC165QPWREP	TSSOP	PW	16	2000	346.0	346.0	29.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



4211283-4/D 06/11

D (R-PDSO-G16) PLASTIC SMALL OUTLINE Stencil Openings (Note D) Example Board Layout (Note C) -16x0,55 - 14x1,27 -14x1,27 16x1,95 4,80 4,80 Example Non Soldermask Defined Pad Example Pad Geometry (See Note C) 0,60 Example 2,00 Solder Mask Opening

(See Note E)

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

← 0,07 All Around

- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. β . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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