SCLS239M - OCTOBER 1995 - REVISED JULY 2003

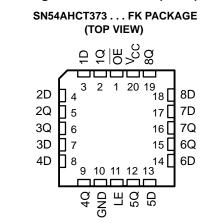
- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17

SN54AHCT373 . . . J OR W PACKAGE SN74AHCT373 . . . DB, DGV, DW, N, NS, OR PW PACKAGE (TOP VIEW)

OE [	1 U	20	] v <sub>cc</sub>
1Q [	2	19	] 8Q
1D [	3	18	] 8D
2D [		17	]7D
2Q [	5	16	] 7Q
3Q [	6	15	] 6Q
3D [	7	14	] 6D
4D [	8	13	] 5D
4Q [	9	12	] 5Q
GND [	10	11	] LE



- 200-V Machine Model (A115-A)
- 1000-V Charged-Device Model (C101)



### description/ordering information

The 'AHCT373 devices are octal-transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

TA	PACK	AGE <sup>†</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
	PDIP – N	Tube	SN74AHCT373N	SN74AHCT373N		
	SOIC - DW	Tube	SN74AHCT373DW	AHCT373		
	3010 - 010	Tape and reel	SN74AHCT373DWR	And 1373		
-40°C to 85°C	SOP – NS	Tape and reel	SN74AHCT373NSR	AHCT373		
-40°C 10 85°C	SSOP – DB	Tape and reel	SN74AHCT373DBR	HB373		
	TSSOP – PW	Tube	SN74AHCT373PW	HB373		
	1330F - FW	Tape and reel	SN74AHCT373PWR	пв <i>эг</i> э		
	TVSOP – DGV	Tape and reel	SN74AHCT373DGVR	HB373		
	CDIP – J	Tube	SNJ54AHCT373J	SNJ54AHCT373J		
–55°C to 125°C	CFP – W Tube		SNJ54AHCT373W	SNJ54AHCT373W		
	LCCC – FK	Tube	SNJ54AHCT373FK	SNJ54AHCT373FK		

**ORDERING INFORMATION** 

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

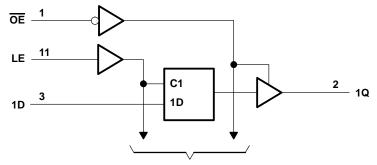


Copyright © 2003, Texas Instruments Incorporated On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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		FUNCTION TABLE (each latch)											
	INPUTS		OUTPUT										
OE	LE	D	Q										
L	Н	Н	Н										
L	н	L	L										
L	L	Х	Q <sub>0</sub>										
н	Х	Х	Z										

## logic diagram (positive logic)



To Seven Other Channels

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) ±25 mA   Continuous current through $V_{CC}$ or GND ±75 mA   Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package 70°C/W   DGV package 92°C/W   DW package 58°C/W   N package 69°C/W   NS package 60°C/W   PW package 83°C/W
Storage temperature range, T <sub>stg</sub> –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



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#### recommended operating conditions (see Note 3)

		SN54AHCT373		SN74AH	CT373	UNIT
		MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2		2		V
VIL	Low-level input voltage		0.8		0.8	V
VI	Input voltage	0	5.5	0	5.5	V
Vo	Output voltage	0	VCC	0	VCC	V
ЮН	High-level output current		-8		-8	mA
IOL	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
Τ <sub>Α</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vee	Т	λ = 25°C	;	SN54AH	CT373	SN74AH	CT373	UNIT
PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
Veu	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.5		4.4		4.4		V
VOH	I <sub>OH</sub> = –8 mA	4.5 V	3.94			3.8		3.8		v
Vei	I <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1		0.1	V
VOL	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44		0.44	v
I <sub>OZ</sub>	$V_{O} = V_{CC}$ or GND	5.5 V			±0.25		±2.5		±2.5	μA
lj	VI = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*		±1	μA
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40		40	μA
∆ICC‡	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5		1.5	mA
Ci	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4	10				10	pF
Co	$V_{O} = V_{CC} \text{ or } GND$	5 V		9						pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

<sup>†</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

# timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

		T <sub>A</sub> = 2	25°C	SN54AH	CT373	SN74AH	CT373	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
tw	Pulse duration, LE high	6.5		6.5		6.5		ns
t <sub>su</sub>	Setup time, data before $\overline{LE}\downarrow$	1.5		1.5		1.5		ns
t <sub>h</sub>	Hold time, data after $\overline{LE}\downarrow$	3.5		3.5		3.5		ns



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# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	Τį	λ = 25°C	>	SN54AH	ICT373	SN74AH	ICT373	UNIT	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
<sup>t</sup> PLH	D	Q	C <sub>I</sub> = 15 pF		5.1*	8.5*	1*	9.5*	1	9.5	00	
<sup>t</sup> PHL		Q	0L = 13 pr		5.1*	8.5*	1*	9.5*	1	9.5	5 ns	
<sup>t</sup> PLH	LE	Q	C <sub>L</sub> = 15 pF		7.7*	12.3*	1*	13.5*	1	13.5	ns	
<sup>t</sup> PHL		Q	0L = 15 pr		7.7*	12.3*	1*	13.5*	1	13.5	115	
<sup>t</sup> PZH		Q	C <sub>L</sub> = 15 pF		6.3*	10.9*	1*	12.5*	1	12.5	20	
<sup>t</sup> PZL	UE	Q	0L = 15 pr		6.3*	10.9*	1*	12.5*	1	12.5	ns	
<sup>t</sup> PHZ		Q	C <sub>1</sub> = 15 pF		6*	10.2*	1*	11*	1	11	ns	
<sup>t</sup> PLZ		<u>v</u>	0L = 10 pi		6*	10.2*	1*	11*	1	11	11	
<sup>t</sup> PLH	D	Q	C <sub>L</sub> = 50 pF		5.9	9.5	1	10.5	1	10.5	20	
<sup>t</sup> PHL		Q	CL = 30 pr		5.9	9.5	1	10.5	1	10.5	0.5 ns	
<sup>t</sup> PLH	LE	Q	C <sub>1</sub> = 50 pF		8.5	13.3	1	14.5	1	14.5	ns	
<sup>t</sup> PHL		Q	0L = 30 pi		8.5	13.3	1	14.5	1	14.5	115	
<sup>t</sup> PZH		Q	C <sub>1</sub> = 50 pF		7.1	11.9	1	13.5	1	13.5	ns	
<sup>t</sup> PZL	UE	Q	0L = 30 pi		7.1	11.9	1	13.5	1	13.5	113	
<sup>t</sup> PHZ		Q	$C_1 = 50 \text{ pF}$		6.8	11.2	1	12	1	12	ns	
<sup>t</sup> PLZ	UE		CL = 50 pr	C <sub>L</sub> = 50 pF		6.8	11.2	1	12 1	12	2 ns	
<sup>t</sup> sk(o)			CL = 50 pF			1**				1	ns	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

\*\* On products compliant to MIL-PRF-38535, this parameter does not apply.

# noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

	PARAMETER	SN7	UNIT		
		MIN	TYP	MAX	UNIT
VOL(P)	Quiet output, maximum dynamic V <sub>OL</sub>		0.8	1.2	V
VOL(V)	Quiet output, minimum dynamic V <sub>OL</sub>		-0.8	-1.2	V
V <sub>OH(V)</sub>	Quiet output, minimum dynamic V <sub>OH</sub>	4.1			V
V <sub>IH(D)</sub>	High-level dynamic input voltage	2			V
V <sub>IL(D)</sub>	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are for surface-mount packages only.

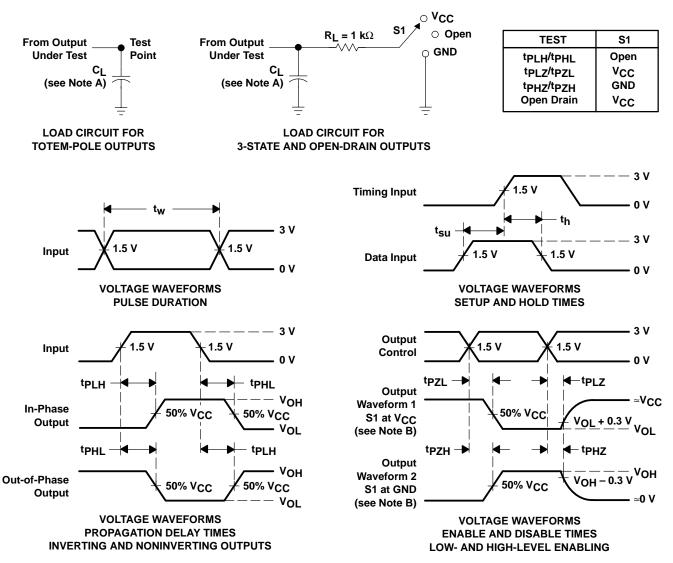
# operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

	PARAMETER	TEST CO	ONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load,	f = 1 MHz	17	pF



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#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. CL includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  3 ns, t<sub>f</sub>  $\leq$  3 ns.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E. All parameters and waveforms are not applicable to all devices.

#### Figure 1. Load Circuit and Voltage Waveforms





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5-Sep-2011

## **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-9686701Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9686701QRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
5962-9686701QSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
SN74AHCT373DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	
SN74AHCT373DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT373DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT373DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT373DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT373DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT373DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT373DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT373DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT373DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT373N	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AHCT373NE4	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AHCT373NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT373NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT373NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT373PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

5-Sep-2011

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74AHCT373PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT373PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT373PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	
SN74AHCT373PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT373PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT373PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54AHCT373FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54AHCT373J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SNJ54AHCT373W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF SN54AHCT373, SN74AHCT373 :

• Catalog: SN74AHCT373

• Military: SN54AHCT373

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

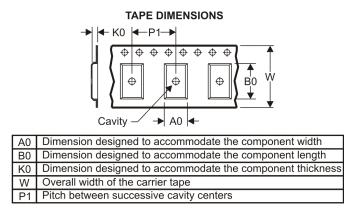
# PACKAGE MATERIALS INFORMATION

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## TAPE AND REEL INFORMATION





## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT373DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHCT373DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74AHCT373NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74AHCT373PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

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# PACKAGE MATERIALS INFORMATION

5-May-2011



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT373DBR	SSOP	DB	20	2000	346.0	346.0	33.0
SN74AHCT373DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74AHCT373NSR	SO	NS	20	2000	346.0	346.0	41.0
SN74AHCT373PWR	TSSOP	PW	20	2000	346.0	346.0	33.0

J (R-GDIP-T\*\*) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20



LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N\*\*) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a metal lid.

D. Falls within JEDEC MS-004



# N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- $\triangle$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AC.



PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  $\beta$ . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



# MECHANICAL DATA

### PLASTIC SMALL-OUTLINE PACKAGE

#### 0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 $\bigcirc$ Gage Plane ₽ 0,25 7 1 1,05 0,55 0-10 Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS \*\* 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G\*\*)

**14-PINS SHOWN** 

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



# **MECHANICAL DATA**

MSSO002E - JANUARY 1995 - REVISED DECEMBER 2001

# DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150



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