## 32-Channel Serial to Parallel Converter With High Voltage Push-Pull Outputs

## Features

- Processed with HVCMOS ${ }^{\text {® }}$ technology
- Output voltages up to 80 V
- Low power level shifting
- Shift register speed 8.0 MHz
- Latched data outputs
- 5.0 V CMOS compatible inputs
- Forward and reverse shifting options
- Diode to $\mathrm{V}_{\mathrm{Pp}}$ allows efficient power recovery


## General Description

The HV9808 is a low voltage serial to high voltage parallel converters with push-pull outputs. This device has been designed for use as a driver for AC-electroluminescent displays. It can also be used in any application requiring multiple output, high voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays. The inputs are fully CMOS compatible.

This device consists of a 32-bit shift register, 32 latches, and control logic to perform the polarity select and blanking of the outputs. $\mathrm{HV}_{\text {out }} 1$ is connected to the first stage of the shift register through the polarity and blanking logic. Data is shifted through the shift register on the logic low to high transition of the clock. The HV9808 shifts data in the counter-clockwise direction when viewed from the top of the package. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register ( $\mathrm{HV}_{\text {out }} 32$ ). Operation of the shift register is not affected by the $\overline{\mathrm{LE}}$ (latch enable), $\overline{\mathrm{BL}}$ (blanking), or the $\overline{\mathrm{POL}}$ (polarity) in-puts. Transfer of data from the shift register to the latch occurs when the $\overline{\operatorname{LE}}$ (latch enable) input is high. The data in the latch is stored when $\overline{L E}$ is low.

## Block Diagram



## Ordering Information

| Device | Package Options |
| :---: | :---: |
|  | 44-Lead Quad |
|  | Plastic Chip Carrier |
| .653x.653in body |  |
|  | .180in height (max) |
| .050in pitch |  |

-G indicates package is RoHS compliant ('Green')


## Absolute Maximum Ratings

| Parameter | Value |
| :--- | ---: |
| Supply voltage, $\mathrm{V}_{\mathrm{DD}}$ | -0.5 V to +7.0 V |
| Supply voltage, $\mathrm{V}_{\mathrm{PP}}$ | -0.5 V to +90 V |
| Logic input levels | -0.5 V to $\mathrm{V}_{\mathrm{DD}}+0.5 \mathrm{~V}$ |
| Ground current ${ }^{1}$ | 1.5 A |
| Continuous total power dissipation ${ }^{2}$ | 1200 mW |
| Operating temperature range | -40 to $+85^{\circ} \mathrm{C}$ |
| Storage temperature range | -65 to $+150^{\circ} \mathrm{C}$ |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

## Notes:

1. Duty cycle is limited by the total power dissipated in the package.
2. For operation above $25^{\circ} \mathrm{C}$ ambient derate linearly to maximum operating temperature at $20 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$.

## Pin Configuration



44-Lead Quad Plastic Chip Carrier (PJ)

## Product Marking

Top Marking
 HV9808PJ LLLLLLLLLL

Bottom Marking


YY = Year Sealed
WW = Week Sealed
L = Lot Number
A = Assembler ID
C = Country of Origin* = "Green" Packaging
*May be part of top marking

Package may or may not include the following marks: Si or $\$ 7$ 44-Lead Quad Plastic Chip Carrier (PJ)

Recommended Operating Conditions

| Sym | Parameter | Min | Max | Units |
| :---: | :--- | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{DD}}$ | Logic voltage supply | 4.5 | 5.5 | V |
| $\mathrm{~V}_{\mathrm{PP}}$ | High voltage supply | 8.0 | 80 | V |
| $\mathrm{~V}_{\mathrm{IH}}$ | Input high voltage | $\mathrm{V}_{\mathrm{DD}}-0.5$ | $\mathrm{~V}_{\mathrm{DD}}$ | V |
| $\mathrm{V}_{\mathrm{IL}}$ | Input low voltage | 0 | 0.5 | V |
| $\mathrm{f}_{\mathrm{CLK}}$ | Clock frequency | 0 | 8.0 | MHz |
| $\mathrm{T}_{\mathrm{A}}$ | Operating free-air temperature | -40 | +85 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics ( $\left.V_{P P}=60 \mathrm{~V}, V_{D 0}=5.0 \mathrm{~V}, T_{A}=25^{\circ} \mathrm{C}\right)$
DC Characteristics

| Sym | Parameter | Min | Max | Units | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\text {PP }}$ | $\mathrm{V}_{\text {PP }}$ supply current | - | 100 | $\mu \mathrm{A}$ | HV outputs high to low |
| $\mathrm{I}_{\text {DD }}$ | $\mathrm{I}_{\text {DD }}$ supply current (quiescent) | - | 100 | $\mu \mathrm{A}$ | All inputs $=\mathrm{V}_{\mathrm{DD}}$ or GND |
| $\mathrm{I}_{\text {D }}$ | $\mathrm{I}_{\text {DD }}$ supply current (operating) | - | 15 | mA | $\mathrm{V}_{\mathrm{DD}}=\mathrm{V}_{\mathrm{DD}} \mathrm{max}, \mathrm{f}_{\mathrm{CLK}}=8.0 \mathrm{MHz}$ |
| $\mathrm{V}_{\mathrm{OH}}$ (Data) | Shift register output voltage | $V_{D D}-0.5$ | - | V | $\mathrm{I}_{0}=-100 \mu \mathrm{~A}$ |
| $\mathrm{V}_{\text {OL }}$ (Data) | Shift register output voltage | - | 0.5 | V | $\mathrm{I}_{0}=100 \mu \mathrm{~A}$ |
| $\mathrm{I}_{\mathrm{H}}$ | Current leakage, any input | - | 1.0 | $\mu \mathrm{A}$ | Input $=\mathrm{V}_{\mathrm{DD}}$ |
| $1{ }_{\text {IL }}$ | Current leakage, any input | - | -1.0 | $\mu \mathrm{A}$ | Input $=$ GND |
| $\mathrm{V}_{\text {oc }}$ | HV output clamp diode voltage | - | -1.5 | V | $\mathrm{I}_{\mathrm{oc}}=-5.0 \mathrm{~mA}$ |
| $\mathrm{V}_{\mathrm{OH}}$ | HV output when sourcing | 52 | - | V | $\mathrm{I}_{\mathrm{OH}}=-20 \mathrm{~mA}, 0$ to $70^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\text {OL }}$ | HV output when sinking | - | 4.0 | V | $\mathrm{I}_{\mathrm{oL}}=5.0 \mathrm{~mA}, 0$ to $70^{\circ} \mathrm{C}$ |

## AC Characteristics

| Sym | Parameter | Min | Max | Units | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{f}_{\text {CLK }}$ | Clock frequency | - | 8.0 | MHz | --- |
| $t_{\text {wL }}$ or $t_{\text {wH }}$ | Clock width, high or low | 62 | - | ns | --- |
| $\mathrm{t}_{\text {su }}$ | Setup time before CLK rises | 25 | - | ns | --- |
| $\mathrm{t}_{\mathrm{H}}$ | Hold time after CLK rises | 10 | - | ns | --- |
| $t_{\text {DLH }}$ (Data) | Data output delay after L to H CLK | - | 110 | ns | $C L=15 p F$ |
| $\mathrm{t}_{\mathrm{DHL}}$ (Data) | Data output delay after H to L CLK | - | 110 | ns | $C L=15 p F$ |
| $\mathrm{t}_{\text {DLE }}$ | $\overline{\text { LE }}$ delay after L to H CLK | 50 | - | ns | --- |
| $\mathrm{t}_{\text {WLE }}$ | Width of $\overline{\mathrm{LE}}$ pulse | 50 | - | ns | --- |
| $\mathrm{t}_{\text {SLE }}$ | $\overline{\text { LE }}$ setup time before $L$ to H CLK | 50 | - | ns | --- |
| $\mathrm{t}_{\mathrm{ON}}$ | Delay from $\overline{L E}$ to $\mathrm{HV}_{\text {OUT }}$, L to H | - | 500 | ns | --- |
| $\mathrm{t}_{\text {OFF }}$ | Delay from $\overline{L E}$ to $\mathrm{HV}_{\text {OUT }}, \mathrm{H}$ to L | - | 500 | ns | --- |

## Power-Up Sequence

1. Connect ground
2. Apply $V_{D D}$
3. Set all inputs (Data, CLK, Enable, etc.) to a known state
4. Apply $\mathrm{V}_{\mathrm{Pp}}$

Power-down sequence should be the reverse of the above.
The $V_{P P}$ should not drop below $V_{D D}$ during operations.

## Input and Output Equivalent Circuits



## Switching Waveforms



Function Table

| Function | Inputs |  |  |  |  | Outputs |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Data | CLK | $\overline{\text { LE }}$ | $\overline{B L}$ | $\overline{\mathrm{POL}}$ | Shift Reg <br> 1 2... 8 | HV Outputs <br> 1 2... 8 | Data Out |
| All on | X | X | X | L | L | - -... | H H... H | $\bullet$ |
| All off | X | X | X | L | H | - -... | L L...L | $\bullet$ |
| Invert mode | $X$ | X | L | H | L | - -... $\bullet$ | - •... | $\bullet$ |
| Load S/R | H OR L | $\uparrow$ | L | H | H | H or L •... | - -... | $\bullet$ |
| Load latches | X | X | $\uparrow$ | H | H | - •... | - -... | $\bullet$ |
|  | X | X | $\uparrow$ | H | L | - •... | - $\bullet \ldots$ | $\bullet$ |
| Transparent latch mode | L | $\uparrow$ | H | H | H | L •... | L •... | - |
|  | H | $\uparrow$ | H | H | H | H •... | H •... | $\bullet$ |

Notes:
$H=$ high level, $L=$ low level, $X=$ irrelevant, $\uparrow=$ low-to-high transition
$\cdot=$ dependent on previous stage's satte before the last CLK or last $\overline{L E}$ high.
Pin Description

| Pin | Function | Function |
| :---: | :---: | :---: |
| 1 | HV ${ }_{\text {OUT }} 16$ | High voltage outputs. <br> High voltage push-pull outputs, which, depending on controlling low voltage data, can drive loads either to a GND, or to $\mathrm{V}_{\mathrm{PP}}$ rail levels. |
| 2 | HV ${ }_{\text {OUT }} 17$ |  |
| 3 | HV ${ }_{\text {OUT }} 18$ |  |
| 4 | HV ${ }_{\text {OUT }} 19$ |  |
| 5 | HV ${ }_{\text {out }} 20$ |  |
| 6 | HV out ${ }^{21}$ |  |
| 7 | $\mathrm{HV}_{\text {out }} 22$ |  |
| 8 | HV ${ }_{\text {OUT }} 23$ |  |
| 9 | HV out 24 |  |
| 10 | HV ${ }_{\text {out }} 25$ |  |
| 11 | HV ${ }_{\text {out }} 26$ |  |
| 12 | HV ${ }_{\text {OUT }} 27$ |  |
| 13 | HV ${ }_{\text {OUT }} 28$ |  |
| 14 | HV ${ }_{\text {OUT }} 29$ |  |
| 15 | HV ${ }_{\text {OUT }} 30$ |  |
| 16 | $\mathrm{HV}_{\text {OUT }} 31$ |  |
| 17 | $\mathrm{HV}_{\text {OUT }} 32$ |  |
| 18 | Data Out | Serial data output <br> Data output for cascading to the data input of the next device. |

Pin Description (cont.)

| Pin | Function | Function |
| :---: | :---: | :---: |
| 19 | N/C | No connect. |
| 20 | N/C |  |
| 21 | Polarity | --- |
| 22 | CLK | Data shift register clock. <br> Input are shifted into the shift register on the positive edge of the clock. |
| 23 | GND | Logic and high voltage ground. |
| 24 | VPP | High voltage power rail. |
| 25 | VDD | Low voltage logic power rail. |
| 26 | Latch Enable | Latch enable input. <br> When $\overline{L E}$ is high, shift register data is transferred into a data latch. When $\overline{L E}$ is low, data is latched, and new data can be clocked into the shift register. |
| 27 | Data In | Serial data input. <br> Data needs to be present before each rising edge of the clock. |
| 28 | $\overline{\text { Blanking }}$ | --- |
| 29 | N/C | No connect. |
| 30 | $\mathrm{HV}_{\text {out }} 1$ | High voltage outputs. <br> High voltage push-pull outputs, which, depending on controlling low voltage data, can drive loads either to a GND, or to $\mathrm{V}_{\mathrm{Pp}}$ rail levels. |
| 31 | HV $\mathrm{out}^{2}$ |  |
| 32 | $\mathrm{HV}_{\text {OUT }}{ }^{3}$ |  |
| 33 | $\mathrm{HV}_{\text {OUT }} 4$ |  |
| 34 | $\mathrm{HV}_{\text {OUT }} 5$ |  |
| 35 | $\mathrm{HV}_{\text {OUT }} 6$ |  |
| 36 | $\mathrm{HV}_{\text {OUT }} 7$ |  |
| 37 | $\mathrm{HV}_{\mathrm{ouT}} 8$ |  |
| 38 | $\mathrm{HV}_{\text {OUT }} 9$ |  |
| 39 | $\mathrm{HV}_{\text {OUT }} 10$ |  |
| 40 | $\mathrm{HV}_{\text {Out }} 11$ |  |
| 41 | $\mathrm{HV}_{\text {Out }} 12$ |  |
| 42 | $\mathrm{HV}_{\text {out }} 13$ |  |
| 43 | $\mathrm{HV}_{\text {OUT }} 14$ |  |
| 44 | $\mathrm{HV}_{\text {Out }} 15$ |  |

## 44-Lead PLCC Package Outline (PJ)

## .653x.653in body, .180in height (max), .050in pitch



Top View


Horizontal Side View


Vertical Side View


View B

## Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Actual shape of this feature may vary.

| Symbol |  | A | A1 | A2 | b | b1 | D | D1 | E | E1 | e | R |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Dimension (inches) | MIN | . 165 | . 090 | . 062 | . 013 | . 026 | . 685 | . 650 | . 685 | . 650 | $\begin{aligned} & .050 \\ & \text { BSC } \end{aligned}$ | . 025 |
|  | NOM | . 172 | . 105 | - | - | - | . 690 | . 653 | . 690 | . 653 |  | . 035 |
|  | MAX | . 180 | . 120 | . 083 | . 021 | . $036{ }^{+}$ | . 695 | . 656 | . 695 | . 656 |  | . 045 |

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.
$\dagger$ This dimension differs from the JEDEC drawing.

## Drawings not to scale.

Supertex Doc. \#: DSPD-44PLCCPJ, Version F031111.
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

[^0]
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