SDAS059C – DECEMBER 1983 – REVISED JANUARY 1995

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Provide Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses With Parity
- Buffered Control Inputs to Reduce dc Loading Effects
- Power-Up High-Impedance State
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs

description

These 10-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type latches. The SN74ALS841 and SN74AS841A have noninverting data (D) inputs. The SN74ALS842 has inverting \overline{D} inputs.

A buffered output-enable (\overline{OE}) input places the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

OE does not affect the internal operation of the latches. Previously stored data can be retained or new data can be entered while the outputs are off.

The SN74ALS841, SN74AS841A, and SN74ALS842 are characterized for operation from 0°C to 70°C.

SN74ALS841, SN74AS841A DW OR NT PACKAGE (TOP VIEW)					
OE [1 1D [2 2D [3 3D [4 4D [5 5D [6 6D [7 7D [8 8D [9 9D [10 10D [11 GND [12	14 10Q				

SN74ALS842... DW OR NT PACKAGE (TOP VIEW)

OE [1	U	24	vcc
1D [2		23] 1Q
2D [3		22] 2Q
3D [4		21] 3Q
4D [20] 4Q
5D [19] 5Q
6D [18] 6Q
7D [8		17]7Q
8D [9		16] 8Q
9D [15] 9Q
10D [11		14] 10Q
GND [12		13	LE

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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Function Tables

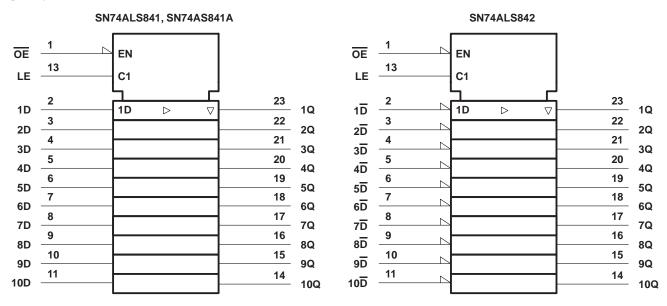
SN74ALS841, SN74AS841A

	INPUTS		OUTPUT
OE	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Х	Q ₀
н	Х	Х	Z

SN74ALS842

	INPUTS		OUTPUT
OE	LE	D	Q
L	Н	Н	L
L	н	L	н
L	L	Х	Q ₀
Н	Х	Х	Z

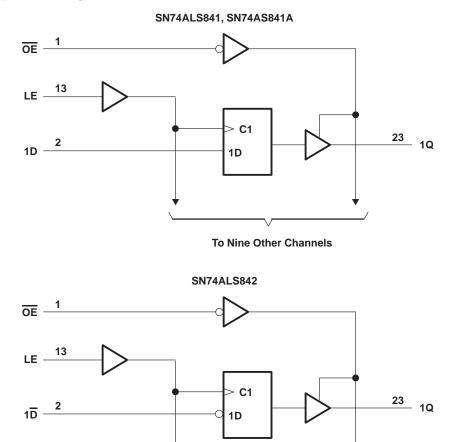
logic symbols[†]

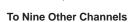


[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagrams (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{CC}	7 V
Input voltage, V _I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T _A : SN74ALS841, SN74ALS842	0°C to 70°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



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recommended operating conditions

		SN74ALS841 SN74ALS842			UNIT
		MIN	NOM	MAX	
VCC	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2			V
VIL	Low-level input voltage			0.8	V
ЮН	High-level output current			-2.6	mA
IOL	Low-level output current			24	mA
tw	Pulse duration, LE high	20			ns
t _{su}	Setup time, data before LE \downarrow	10			ns
t _h	Hold time, data after LE \downarrow	5			ns
TA	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST COND	DITIONS	-	74ALS84 74ALS84		UNIT
				MIN	TYP [†]	MAX	
VIK		V _{CC} = 4.5 V,	lı = – 18 mA			-1.2	V
Val		$V_{CC} = 4.5 V \text{ to } 5.5 V,$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2			V
Vон		V _{CC} = 4.5 V,	I _{OH} = -2.6 mA	2.4	3.2		v
Mar			I _{OL} = 12 mA		0.25	0.4	V
VOL		$V_{CC} = 4.5 V$	I _{OL} = 24 mA		0.35	0.5	v
IOZH		V _{CC} = 5.5 V,	V _O = 2.7 V			20	μA
IOZL		V _{CC} = 5.5 V,	V _O = 0.4 V			-20	μΑ
Ц		V _{CC} = 5.5 V,	$V_{I} = 7 V$			0.1	mA
IIН		V _{CC} = 5.5 V,	VI = 2.7 V			20	μΑ
۱ _{IL}		V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1	mA
IO‡		V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	mA
			Outputs high		19	30	
	SN74ALS841	$V_{CC} = 5.5 V$	Outputs low		38	62	
ICC			Outputs disabled		23	40	
			Outputs high		20	35	mA
	SN74ALS842	$V_{CC} = 5.5 V$	Outputs low		48	74	
			Outputs disabled		27	44	

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5$ $C_L = 50 \text{ pF}$ $R1 = 500 \Omega$ $R2 = 500 \Omega$ $T_A = \text{MIN tr}$ SN74A	^{2,} 0 MAX†	UNIT	
				MIN	MAX	
^t PLH	D	0	2	13	ns	
^t PHL		Q	2	13	115	
^t PLH	LE	0	7	21		
^t PHL	LE	Q	8	26	ns	
^t PZH			2	12		
tPZL	OE	Q	2	12	ns	
^t PHZ	ŌĒ	0	2	10		
^t PLZ	0E	Q	2	12	ns	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 C _L = 50 pF R1 = 500 Ω R2 = 500 Ω T _A = MIN tr SN74A	; <u>2,</u> 0 MAX†	UNIT	
				MIN	MAX]
^t PLH	D		4	18		
^t PHL		Q	3	13	ns	
^t PLH	LE		8	27		
^t PHL	LE	Q	6	20	ns	
^t PZH			2	12		
^t PZL	OE	Q	2	12	ns	
^t PHZ	ŌĒ	0	1	10		
^t PLZ	UE UE	Q	2	12	ns	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, V _{CC}	
Input voltage, V _I	7V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T _A : SN74AS841A	0°C to 70°C
Storage temperature range	−65°C to 150°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



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recommended operating conditions

		SN74AS841A		UNIT	
		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2			V
VIL	Low-level input voltage			0.8	V
IOH	High-level output current			-24	mA
IOL	Low-level output current			48	mA
tw	Pulse duration, LE high	4			ns
t _{su}	Setup time, data before LE \downarrow	2.5			ns
t _h	Hold time, data after LE \downarrow	2.5			ns
ТА	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN	74AS841	A	UNIT
PARAMETER			MIN	TYP†	MAX	UNIT
VIK	V _{CC} = 4.5 V,	l _l = – 18 mA			-1.2	V
	$V_{CC} = 4.5 V \text{ to } 5.5 V,$	$I_{OH} = -2 \text{ mA}$	V _{CC} -2			
VOH	V _{CC} = 4.5 V	I _{OH} = -15 mA	2.4	3.2		V
	VCC = 4.5 V	I _{OH} = -24 mA	2			
Vol	V _{CC} = 4.5 V,	I _{OL} = 48 mA		0.35	0.5	V
IOZH	V _{CC} = 5.5 V,	V _O = 2.7 V			50	μA
lozl	V _{CC} = 5.5 V,	V _O = 0.4 V			-50	μA
li li	V _{CC} = 5.5 V,	$V_{I} = 7 V$			0.1	mA
ЦΗ	V _{CC} = 5.5 V,	VI = 2.7 V			20	μΑ
ΙIL	V _{CC} = 5.5 V,	VI = 0.4 V			-0.5	mA
IO‡	V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	mA
		Outputs high		36	60	
lcc	$V_{CC} = 5.5 V$	Outputs low		58	94	mA
		Outputs disabled		56	93	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$. [‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



SN74ALS841, SN74AS841A, SN74ALS842 10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS SDAS059C – DECEMBER 1983 – REVISED JANUARY 1995

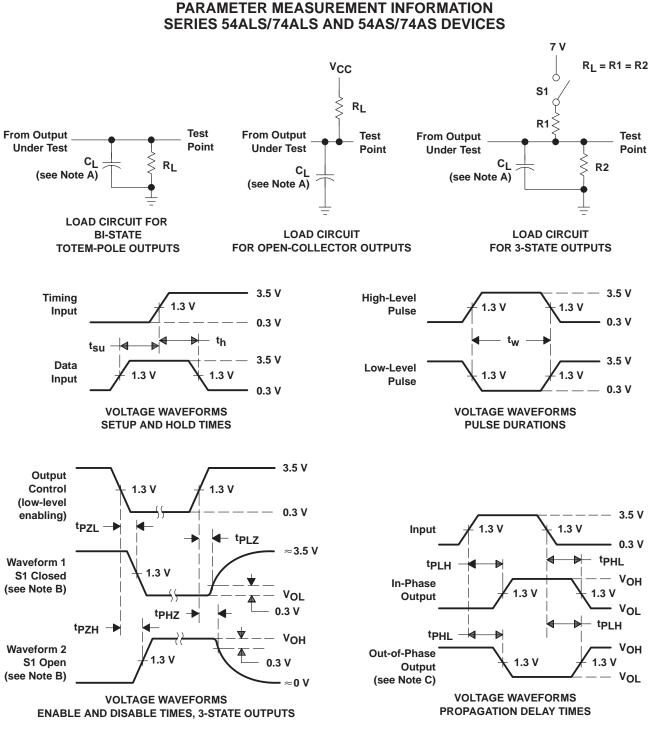
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5$ $C_L = 50 \text{ pF}$ $R1 = 500 \Omega$ $R2 = 500 \Omega$ $T_A = \text{MIN tr}$ SN74A	<u>2,</u> o MAX [†] S841A	UNIT
			MIN	MAX	
^t PLH	D	â	1	6.5	ns
^t PHL	d	Q	1	10.5	
^t PLH	LE	0	2	12	ns
^t PHL	LE	Q	2	12	
^t PZH			2	14	ns
tPZL	OE	Q	2	16	
^t PHZ	OE	0	1	8	ns
^t PLZ	0E	Q	1	8	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR \leq 1 MHz, t_{f} = t_{f} = 2 ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74ALS841DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS841DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS841DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS841NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74ALS841NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74ALS842DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	Samples Not Available
SN74ALS842NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	Samples Not Available
SN74AS841ADW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	Samples Not Available
SN74AS841ADWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	Samples Not Available
SN74AS841ANT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	Samples Not Available

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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NT (R-PDIP-T**) 24 pins shown

PLASTIC DUAL-IN-LINE PACKAGE



All integrations are in minimeters. Dimensioning and toil
B. This drawing is subject to change without notice.

The 28 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AD.



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