SN54AC373 ... J OR W PACKAGE

SN74AC373

SCAS540D - OCTOBER 1995 - REVISED OCTOBER 2003

- 2-V to 6-V V_{CC} Operation
- Inputs Accept Voltages to 6 V
- Max t_{pd} of 9.5 ns at 5 V
- 3-State Noninverting Outputs Drive Bus Lines Directly
- Full Parallel Access for Loading

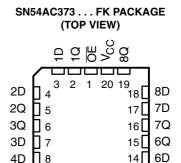
description/ordering information

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are D-type transparent latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines in bus-organized systems without need for interface or pullup components.

	, DW, N, (TOP VI		, OR PW PACKAGE
OE [1Q [1D 2D [2Q 2Q 2 3D [4D [4Q 2] 6ND [1 2 3 4 5 6 7 8 9 10	20 19 18 17 16 15 14 13 12 12	V _{CC} 8Q 8D 7D 7Q 6Q 6D 5D 5Q
1			



9 10 11 12 13

GND

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

	•			
T _A	PACKAG	Et	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube	SN74AC373N	SN74AC373N
		Tube	SN74AC373DW	40070
	SOIC – DW	Tape and reel	SN74AC373DWR	AC373
–40°C to 85°C	SOP – NS	Tape and reel	SN74AC373NSR	AC373
	SSOP – DB	Tape and reel	SN74AC373DBR	AC373
	TOOOD DW	Tube	SN74AC373PW	40070
	TSSOP – PW	Tape and reel	SN74AC373PWR	AC373
	CDIP – J	Tube	SNJ54AC373J	SNJ54AC373J
–55°C to 125°C	CFP – W	Tube	SNJ54AC373W	SNJ54AC373W
	LCCC – FK	Tube	SNJ54AC373FK	SNJ54AC373FK

ORDERING INFORMATION

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



 $Copyright @ 2003, Texas Instruments Incorporated \\ On products compliant to MIL-PRF-3853s, all parameters are tested \\ unless otherwise noted. On all other products, production \\ processing does not necessarily include testing of all parameters. \\$

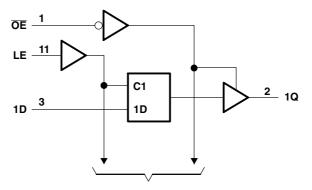
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description/ordering information (continued)

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

	FUNCTION TABLE (each latch)										
	INPUTS		OUTPUT								
ŌE	LE	D	Q								
L	Н	Н	Н								
L	Н	L	L								
L	L	Х	Q ₀								
Н	Х	Х	Z								

logic diagram (positive logic)



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	–0.5 V to 7 V
Input voltage range, V _I (see Note 1)	–0.5 V to V _{CC} + 0.5 V
Output voltage range, V _O (see Note 1)	–0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} (V _I < 0 or V _I > V _{CC})	±20 mA
	±20 mA
	±50 mA
Continuous current through V _{CC} or GND	±200 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package
	DW package 58°C/W
	N package 69°C/W
	NS package 60°C/W
	PW package
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Note 3)

			SN54	AC373	SN74AC373		
			MIN	MAX	MIN	MAX	UNIT
V _{CC}	Supply voltage		2	6	2	6	V
		$V_{CC} = 3 V$	2.1		2.1		
VIH	High-level input voltage	$V_{CC} = 4.5 V$	3.15		3.15		V
		V _{CC} = 5.5 V	3.85		3.85		
		V _{CC} = 3 V		0.9		0.9	
V _{IL}	Low-level input voltage	$V_{CC} = 4.5V$		1.35		1.35	V
		V _{CC} = 5.5 V		1.65		1.65	
VI	Input voltage		0	V _{CC}	0	V _{CC}	V
Vo	Output voltage		0	V _{CC}	0	V _{CC}	V
		V _{CC} = 3 V		-12		-12	
I _{OH}	High-level output current	V _{CC} = 4.5 V		-24		-24	mA
		V _{CC} = 5.5 V		-24		-24	
		V _{CC} = 3 V		12		12	
l _{OL}	Low-level output current	$V_{CC} = 4.5 V$		24		24	mA
		V _{CC} = 5.5 V		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	·		8		8	ns/V
T _A	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		V	٦	Γ _A = 25°	C	SN54	AC373	SN74	AC373	
PARAMETER	TEST CONDITIONS	v _{cc}	MIN	TYP	MAX	MIN	MAX	MIN	МАХ	UNIT
		3 V	2.9			2.9		2.9		
	l _{OH} = -50 μA	4.5 V	4.4			4.4		4.4		
N/		5.5 V	5.4			5.4		5.4		v
V _{OH}	I _{OH} = –12 mA	3 V	2.56			2.4		2.46		v
		4.5 V	3.86			3.7		3.76		
	I _{OH} = -24 mA	5.5 V	4.86			4.7		4.76		
		3 V			0.1		0.1		0.1	
	l _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
V _{OL}	I _{OL} = 12 mA	3 V			0.36		0.5		0.44	V
	1 04 m 1	4.5 V			0.36		0.5		0.44	
	I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44	
l _l	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μA
I _{OZ}	$V_{O} = V_{CC}$ or GND	5.5 V			±0.25		±5		±2.5	μA
Icc	$V_{I} = V_{CC} \text{ or } GND, \qquad I_{O} = 0$	5.5 V			4		80		40	μA
Ci	V _I = V _{CC} or GND	5 V		4.5						pF



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timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54AC373		SN74AC373		
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
tw	Pulse duration, LE high	5.5		6.5		6		ns
t _{su}	Setup time, data before LE \downarrow	5.5		6.5		6		ns
t _h	Hold time, data after LE \downarrow	1		1		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54AC373		SN74AC373		
		MIN	MAX	MIN	MAX	MIN	МАХ	UNIT
tw	Pulse duration, LE high	4		5		4.5		ns
t _{su}	Setup time, data before LE \downarrow	4		5		4.5		ns
t _h	Hold time, data after LE \downarrow	1		1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

DADAMETER	то	то	T _A = 25°C			SN54	AC373	SN74AC373			
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
t _{PLH}	C	0	1.5	10	13.5	1	16.5	1.5	15		
t _{PHL}	D	Q	1.5	9.5	13.0	1	16	1.5	14.5	ns	
t _{PLH}		0	1.5	10	13.5	1	16.5	1.5	15		
t _{PHL}	LE	Q	1.5	9.5	12.5	1	15	1.5	14	ns	
t _{PZH}		0	1.5	9	11.5	1	14	1	13		
t _{PZL}	ŌĒ	Q	1.5	8.5	11.5	1	13.5	1	13	ns	
t _{PHZ}	OE	Q	1.5	10	12.5	1	16	1	14.5	-	
t _{PLZ}	UE	Ŷ	1.5	8	11.5	1	13	1	12.5	ns	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

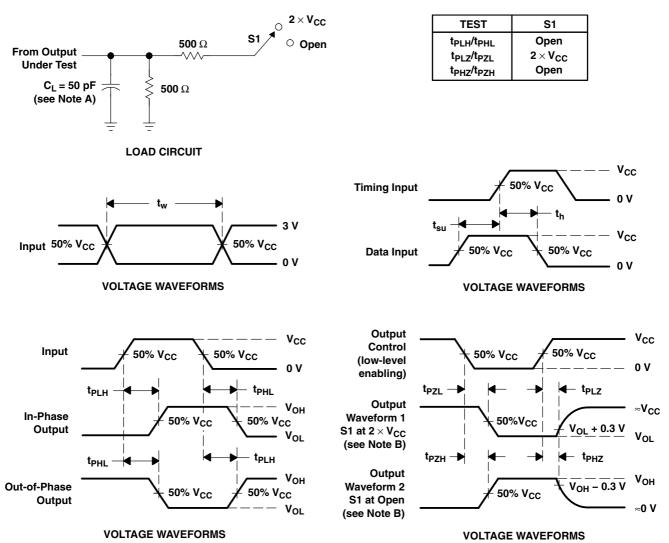
DADAMETER	то	то	٦	Γ _A = 25°	C	SN54	AC373	SN74	AC373		
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
t _{PLH}	C	0	1.5	7	9.5	1	11.5	1.5	10.5		
t _{PHL}	D	Q	1.5	7	9.5	1	11.5	1.5	10.5	ns	
t _{PLH}		0	1.5	7.5	9.5	1	12	1.5	10.5		
t _{PHL}	LE	Q	1.5	7	9.5	1	11	1.5	10.5	ns	
t _{PZH}	OE	0	1.5	7	8.5	1	10.5	1	9.5	20	
t _{PZL}	OE	Q	1.5	6.5	8.5	1	10	1	9.5	ns	
t _{PHZ}	OE	Q	1.5	8	11	1	13.5	1	12.5	-	
t _{PLZ}	UE	Ŷ	1.5	6.5	8.5	1	10.5	1	10	ns	

operating characteristics, $V_{CC} = 5 V$, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	$C_L = 50 \text{ pF}, f = 1 \text{ MHz}$	40	pF



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PARAMETER MEASUREMENT INFORMATION

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_Q = 50 Ω , t_r \leq 2.5 ns, t_f \leq 2.5 ns.
- C. All input puises are supplied by generators naving the rollowing characteristics: PHR \leq 1 MHz, $Z_0 = 50 \Omega$, t_r
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-87555012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8755501RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
5962-8755501SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
5962-8755501VRA	ACTIVE	CDIP	J	20	20	TBD	A42	N / A for Pkg Type	
5962-8755501VSA	ACTIVE	CFP	W	20	25	TBD	Call TI	N / A for Pkg Type	
SN74AC373DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	
SN74AC373DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC373DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC373DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC373DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC373DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC373DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC373DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC373DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC373DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC373N	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AC373NE4	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AC373NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC373NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC373NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



23-Mar-2012

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74AC373PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC373PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC373PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC373PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	
SN74AC373PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC373PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC373PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54AC373FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54AC373J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SNJ54AC373W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



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23-Mar-2012

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OTHER QUALIFIED VERSIONS OF SN54AC373, SN54AC373-SP, SN74AC373 :

• Catalog: SN74AC373, SN54AC373

• Enhanced Product: SN74AC373-EP, SN74AC373-EP

• Military: SN54AC373

• Space: SN54AC373-SP

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application

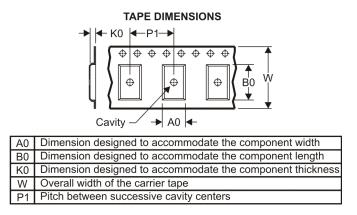
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC373DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AC373DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74AC373NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74AC373PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

5-May-2011



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC373DBR	SSOP	DB	20	2000	346.0	346.0	33.0
SN74AC373DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74AC373NSR	SO	NS	20	2000	346.0	346.0	41.0
SN74AC373PWR	TSSOP	PW	20	2000	346.0	346.0	33.0

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20



LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N**) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a metal lid.

D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AC.



PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. β . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0-10 Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



MECHANICAL DATA

MSSO002E - JANUARY 1995 - REVISED DECEMBER 2001

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150



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