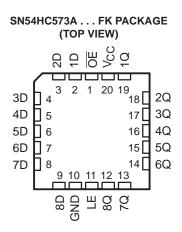
SCLS147E – DECEMBER 1982 – REVISED SEPTEMBER 2003

- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Drive Bus Lines Directly or Up To 15 LSTTL Loads
- Low Power Consumption, 80-µA Max I_{CC}

SN54HC573A . . . J OR W PACKAGE SN74HC573A . . . DB, DW, N, OR PW PACKAGE (TOP VIEW)

OE [1	\cup_{20}	Vcc
1D [2	19	[] 1Q
2D [3	18] 2Q
3D [4	17] 3Q
4D [5	16] 4Q
5D [6	15] 5Q
6D [7	14] 6Q
7D [8	13] 7Q
8D [9	12] 8Q
GND [10	11	LE

- Typical t_{pd} = 21 ns
- ±6-mA Output Drive at 5 V
- Low Input Current of 1 µA Max
- Bus-Structured Pinout



description/ordering information

These octal transparent D-type latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs respond to the data (D) inputs. When LE is low, the outputs are latched to retain the data that was set up.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

TA	PACK	AGET	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube of 25	SN74HC573AN	SN74HC573AN
		Tube of 40	SN74HC573ADW	1105704
4000 10 0500	SOIC – DW	Reel of 2500	SN74HC573ADWR	HC573A
–40°C to 85°C	SSOP – DB	Reel of 2000	SN74HC573ADBR	HC573A
		Reel of 2000	SN74HC573APWR	1105704
	TSSOP – PW	Reel of 250	SN74HC573APWT	HC573A
	CDIP – J	Tube of 25	SNJ54HC573AJ	SNJ54HC573AJ
–55°C to 125°C	CFP – W	Tube of 150	SNJ54HC573AW	SNJ54HC573AW
	LCCC – FK	Tube of 55	SNJ54HC573AFK	SNJ54HC573AFK

ORDERING INFORMATION

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



Copyright © 2003, Texas Instruments Incorporated On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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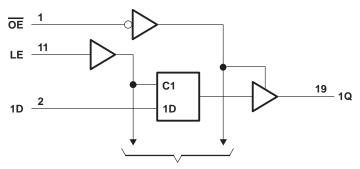
description/ordering information (continued)

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

	FUNCTION TABLE (each latch)												
	INPUTS		OUTPUT										
OE	LE	D	Q										
L	Н	Н	Н										
L	Н	L	L										
L	L	Х	Q ₀ Z										
Н	Х	Х	Z										

logic diagram (positive logic)



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	
Input clamp current, I_{IK} (V _I < 0 or V _I > V _{CC}) (see	Note 1) ±20 mA
	(see Note 1) ±20 mA
	±35 mA
	±70 mA
	DB package
-	DW package 58°C/W
1	V package
	PW package 83°C/W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



SCLS147E - DECEMBER 1982 - REVISED SEPTEMBER 2003

recommended operating conditions (see Note 3)

			SN	54HC57	3A	SN	74HC573	3A	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		2	5	6	2	5	6	V
		$V_{CC} = 2 V$	1.5			1.5			
VIH	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			V
		$V_{CC} = 6 V$	4.2			4.2			
		$V_{CC} = 2 V$			0.5			0.5	
VIL	Low-level input voltage	V _{CC} = 4.5 V			1.35			1.35	V
		V _{CC} = 6 V			1.8			1.8	
VI	Input voltage		0		VCC	0		VCC	V
VO	Output voltage		0		VCC	0		VCC	V
		$V_{CC} = 2 V$			1000			1000	
tt	Input transition (rise and fall) time	V _{CC} = 4.5 V			500			500	ns
		V _{CC} = 6 V			400			400	
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	7507.00			Т	A = 25°C	;	SN54H	C573A	SN74H	C573A	UNIT
PARAMETER	TEST CO	ONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V	1.9	1.998		1.9		1.9		
		I _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		4.4		
VOH	$V_I = V_{IH} \text{ or } V_{IL}$		6 V	5.9	5.999		5.9		5.9		V
		$I_{OH} = -6 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
		I _{OH} = -7.8 mA	6 V	5.48	5.8		5.2		5.34		
			2 V		0.002	0.1		0.1		0.1	
		I _{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	
V _{OL}	$V_{I} = V_{IH} \text{ or } V_{IL}$		6 V		0.001	0.1		0.1		0.1	V
		IOL = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I _{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
lį	$V_I = V_{CC} \text{ or } 0$		6 V		±0.1	±100		±1000		±1000	nA
IOZ	VO = ACC or 0		6 V		±0.01	±0.5		±10		±5	μΑ
ICC	$V_I = V_{CC} \text{ or } 0,$	IO = 0	6 V			8		160		80	μΑ
Ci			2 V to 6 V		3	10		10		10	pF



SCLS147E - DECEMBER 1982 - REVISED SEPTEMBER 2003

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			T _A = 2	25°C	SN54H	C573A	SN74H	C573A	
		vcc	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
		2 V	80		120		100		
tw	Pulse duration, LE high	4.5 V	16		24		20		ns
		6 V	14		20		17		
		2 V	50		75		63		
t _{su}	Setup time, data before LE \downarrow	4.5 V	10		15		13		ns
		6 V	9		13		11		
		2 V	20		24		24		
th	Hold time, data after LE \downarrow	4.5 V	5		5		5		ns
		6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

	FROM	то		Т	₄ = 25° Ω	;	SN54H	C573A	SN74H0	C573A	
PARAMETER	(INPUT)	(OUTPUT)	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V		77	175		265		220	
	D	Q	4.5 V		26	35		53		44	
			6 V		23	30		45		38	
^t pd			2 V		87	175		265		220	ns
	LE	Any Q	4.5 V		27	35		53		44	
			6 V		23	30		45		38	
			2 V		68	150		225		190	
ten	OE	Any Q	4.5 V		24	30		45		38	ns
			6 V		21	26		38		32	
			2 V		47	150		225		190	
^t dis	OE	Any Q	4.5 V		23	30		45		38	ns
			6 V		21	26		38		32	
			2 V		28	60		90		75	
tt		Any Q	4.5 V		8	12		18		15	ns
			6 V		6	10		15		13	



SN54HC573A, SN74HC573A **OCTAL TRANSPARENT D-TYPE LATCHES** WITH 3-STATE OUTPUTS SCLS147E – DECEMBER 1982 – REVISED SEPTEMBER 2003

switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$ (unless otherwise noted) (see Figure 1)

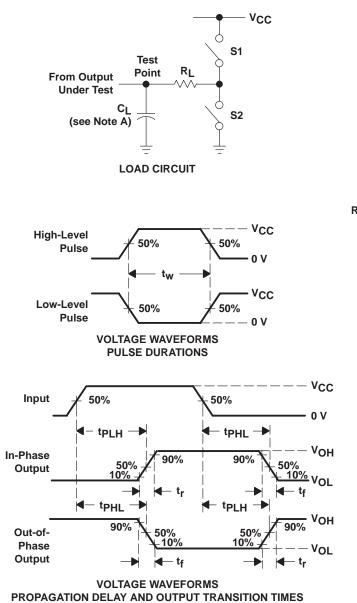
	FROM	то		Τį	₄ = 25°C	;	SN54H0	C573A	SN74H	C573A	
PARAMETER	(INPUT)	(OUTPUT)	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V		95	200		300		250	
	D	Q	4.5 V		33	40		60		50	
			6 V		21	34		51		43	
^t pd			2 V		103	225		335		285	ns
	LE	Any Q	4.5 V		33	45		67		57	
			6 V		29	38		57		48	
			2 V		85	200		300		250	
^t en	OE	Any Q	4.5 V		29	40		60		50	ns
			6 V		26	34		51		43	
			2 V		60	210		315		265	
tt		Any Q	4.5 V		17	42		63		53	ns
			6 V		14	36		53		45	

operating characteristics, $T_A = 25^{\circ}C$

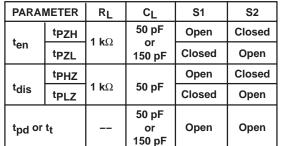
	PARAMETER	TEST CONDITIONS	TYP	UNIT
Cpd	Power dissipation capacitance per latch	No load	50	pF

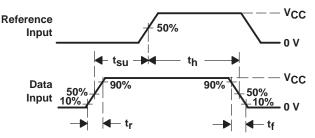


SCLS147E - DECEMBER 1982 - REVISED SEPTEMBER 2003

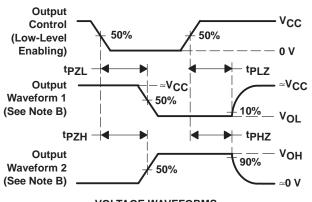


PARAMETER MEASUREMENT INFORMATION



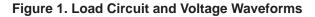


VOLTAGE WAVEFORMS SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

- NOTES: A. CL includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_f = 6 ns, t_f = 6 ns.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. tPLH and tPHL are the same as tpd.







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23-Mar-2012

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-8512801VRA	ACTIVE	CDIP	J	20	20	TBD	A42	N / A for Pkg Type	
5962-8512801VSA	ACTIVE	CFP	W	20	25	TBD	Call TI	N / A for Pkg Type	
85128012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
8512801RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
8512801SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
JM38510/65406BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
M38510/65406BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SN54HC573AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SN74HC573ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC573ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC573ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC573ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC573ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC573ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC573ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC573ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC573ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC573AN	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74HC573AN3	OBSOLETE	PDIP	Ν	20		TBD	Call TI	Call TI	
SN74HC573ANE4	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74HC573APWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	
SN74HC573APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74HC573APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC573APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC573APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC573APWTE4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC573APWTG4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54HC573AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54HC573AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SNJ54HC573AW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE OPTION ADDENDUM



23-Mar-2012

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC573A, SN54HC573A-SP, SN74HC573A :

• Catalog: SN74HC573A, SN54HC573A

Automotive: SN74HC573A-Q1, SN74HC573A-Q1

• Military: SN54HC573A

• Space: SN54HC573A-SP

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application

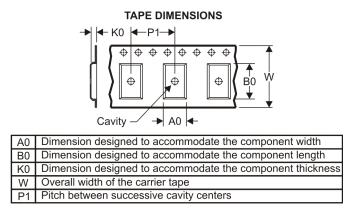
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC573ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HC573ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74HC573APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74HC573APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TEXAS INSTRUMENTS

www.ti.com

PACKAGE MATERIALS INFORMATION

5-May-2011



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC573ADBR	SSOP	DB	20	2000	346.0	346.0	33.0
SN74HC573ADWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74HC573APWR	TSSOP	PW	20	2000	346.0	346.0	33.0
SN74HC573APWT	TSSOP	PW	20	250	346.0	346.0	33.0

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20



LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N**) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AC.



LAND PATTERN DATA



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. β . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



MECHANICAL DATA

MSSO002E - JANUARY 1995 - REVISED DECEMBER 2001

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150



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