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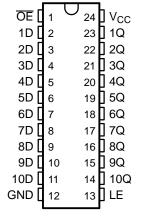
SN74LVC841A 10-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS307J-MARCH 1993-REVISED FEBRUARY 2005

FEATURES

- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 6.7 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 >2 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} Supports Partial-Power-Down Mode Operation
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DB, DGV, DW, OR PW PACKAGE (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This 10-bit bus-interface D-type latch is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC841A is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	SOIC - DW	Tube of 25	SN74LVC841ADW	LVC841A	
	SOIC - DW	Reel of 2000	SN74LVC841ADWR	LVC04TA	
	SSOP - DB	Reel of 2000	SN74LVC841ADBR	LC841A	
–40°C to 85°C		Tube of 60	SN74LVC841APW		
	TSSOP - PW	Reel of 2000	SN74LVC841APWR	LC841A	
		Reel of 250	SN74LVC841APWT		
	TVSOP - DGV	Reel of 2000	SN74LVC841ADGVR	LC841A	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

OE does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

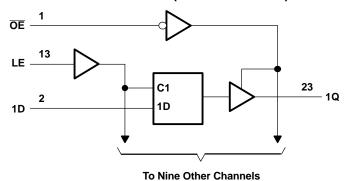
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FUNCTION TABLE

	INPUTS	OUTPUT	
ŌĒ	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	X	Q_0
Н	X	Χ	Z

LOGIC DIAGRAM (POSITIVE LOGIC)





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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_{I}	Input voltage range (2)		-0.5	6.5	V
Vo	Voltage range applied to any output in the high-in	-0.5	6.5	V	
Vo	Voltage range applied to any output in the high of	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
		DB package		63	
0	Dooks as the small impedence (4)	DGV package		86	°C/W
θ_{JA}	Package thermal impedance (4)	DW package		46	-C/VV
		PW package		88	
T _{stg}	Storage temperature range	-65	150	°C	

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT	
\/	Supply voltage	Operating	1.65	3.6	V	
V _{CC}	Supply voltage	Data retention only	1.5		V	
		V _{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
VI	Input voltage		0	5.5	V	
\/	Output voltage	High or low state	0	V _{CC}	V	
Vo	Output voltage	3-state	0	0 5.5		
		V _{CC} = 1.65 V		-4		
	High lovel output ourrent	$V_{CC} = 2.3 \text{ V}$		-8	mA	
I _{OH}	High-level output current	$V_{CC} = 2.7 \text{ V}$		-12	ША	
		$V_{CC} = 3 V$		-24		
		$V_{CC} = 1.65 \text{ V}$		4		
	Low level output ourrent	$V_{CC} = 2.3 \text{ V}$		8	mA	
I _{OL}	Low-level output current	$V_{CC} = 2.7 \text{ V}$		12	ША	
		V _{CC} = 3 V		24		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
T _A	Operating free-air temperature		-40	85	°C	

All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The value of V_{CC} is provided in the recommended operating conditions table.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	ONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾ MAX	UNIT	
	$I_{OH} = -100 \mu A$		1.65 V to 3.6 V	V _{CC} - 0.2			
	$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
V	$I_{OH} = -8 \text{ mA}$		2.3 V	1.7		V	
V _{OH}	I _{OH} = -12 mA		2.7 V	2.2		V	
	1 _{OH} = -12 IIIA		3 V	2.4			
	$I_{OH} = -24 \text{ mA}$		3 V	2.2			
	I _{OL} = 100 μA	1.65 V to 3.6 V		0.2			
	I _{OL} = 4 mA		1.65 V		0.45		
V _{OL}	I _{OL} = 8 mA	2.3 V		0.7	V		
	I _{OL} = 12 mA	2.7 V		0.4			
	I _{OL} = 24 mA	3 V		0.55			
I _I	V _I = 0 to 5.5 V		3.6 V		±5	μΑ	
I _{off}	V_I or $V_O = 5.5 \text{ V}$		0		±10	μΑ	
l _{OZ}	V _O = 0 to 5.5 V		3.6 V		±10	μΑ	
	$V_I = V_{CC}$ or GND	1 0	261/		10	^	
I _{CC}	$3.6 \text{ V} \le \text{V}_{\text{I}} \le 5.5 \text{ V}^{(2)}$	$I_{O} = 0$	3.6 V		10	μΑ	
ΔI_{CC}	One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μΑ	
C _i	$V_I = V_{CC}$ or GND	3.3 V		5	pF		
Co	$V_O = V_{CC}$ or GND		3.3 V		7	pF	

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. (2) This applies in the disabled state only.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC} = ± 0.1	1.8 V 5 V	V _{CC} = 1 ± 0.2		V _{CC} =	2.7 V	V _{CC} = ± 0.3	3.3 V 3 V	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	(1)		(1)		3.3		3.3		ns
t _{su}	Setup time, data before LE↓	(1)		(1)		2.1		2.1		ns
t _h	Hold time, data after LE↓	(1)		(1)		1		1		ns

⁽¹⁾ This information was not available at the time of publication.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.2	V _{CC} = 1.8 V ± 0.2 V		V_{CC} = 2.5 V \pm 0.2 V		V _{CC} = 2.7 V		V_{CC} = 3.3 V \pm 0.3 V	
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	D	Q	(1)	(1)	(1)	(1)		7.5	2.4	6.7	20
l _{pd}	t _{pd} LE		(1)	(1)	(1)	(1)		8.6	2.7	7.6	ns
t _{en}	ŌĒ	Q	(1)	(1)	(1)	(1)		8.5	1.3	7.2	ns
t _{dis}	ŌĒ	Q	(1)	(1)	(1)	(1)		6.6	1.9	5.9	ns
t _{sk(o)}										1	ns

⁽¹⁾ This information was not available at the time of publication.





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Operating Characteristics

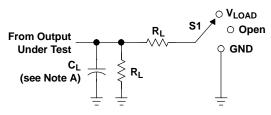
 $T_A = 25^{\circ}C$

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT	
Power dissipation capacitance		Outputs enabled	f = 10 MHz	(1)	(1)	25	nE.	
C _{pd}	per latch	Outputs disabled	1 = 10 MHZ	(1)	(1)	6	pF	

⁽¹⁾ This information was not available at the time of publication.



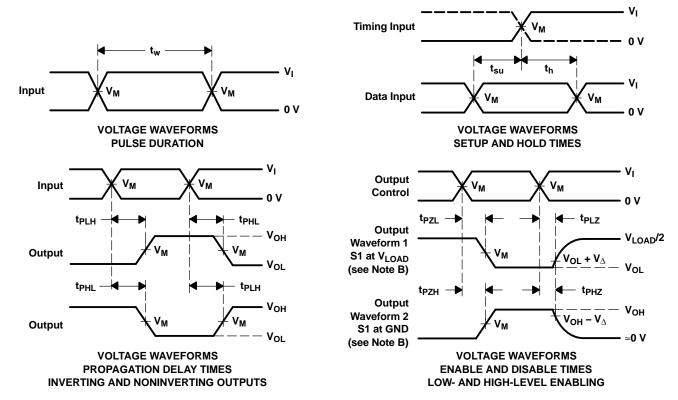
PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

1	0	Δ	n	CI	R	CI	П	ıT

.,	INPUTS		.,	.,		_	.,	
V _{CC}	VI	t _r /t _f	V _M V _{LOAD}		CL	R _L	V_{Δ}	
1.8 V \pm 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V	
2.5 V \pm 0.2 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V	
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V	
3.3 V \pm 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V	



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2009

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVC841ADBLE	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI
SN74LVC841ADBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC841ADBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC841ADBRG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC841ADGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC841ADGVRE4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC841ADGVRG4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC841ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC841ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC841ADWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC841APW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC841APWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC841APWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC841APWLE	OBSOLETE	TSSOP	PW	24		TBD	Call TI	Call TI
SN74LVC841APWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC841APWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC841APWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC841APWT	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC841APWTE4	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC841APWTG4	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



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for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

All difficults are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC841ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVC841ADGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC841APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVC841APWT	TSSOP	PW	24	250	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC841ADBR	SSOP	DB	24	2000	346.0	346.0	33.0
SN74LVC841ADGVR	TVSOP	DGV	24	2000	346.0	346.0	29.0
SN74LVC841APWR	TSSOP	PW	24	2000	346.0	346.0	33.0
SN74LVC841APWT	TSSOP	PW	24	250	346.0	346.0	33.0

DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194 DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



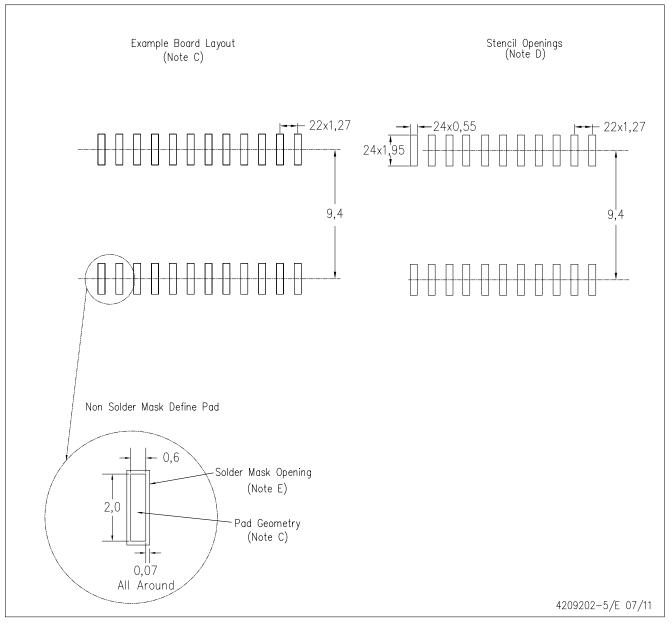
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



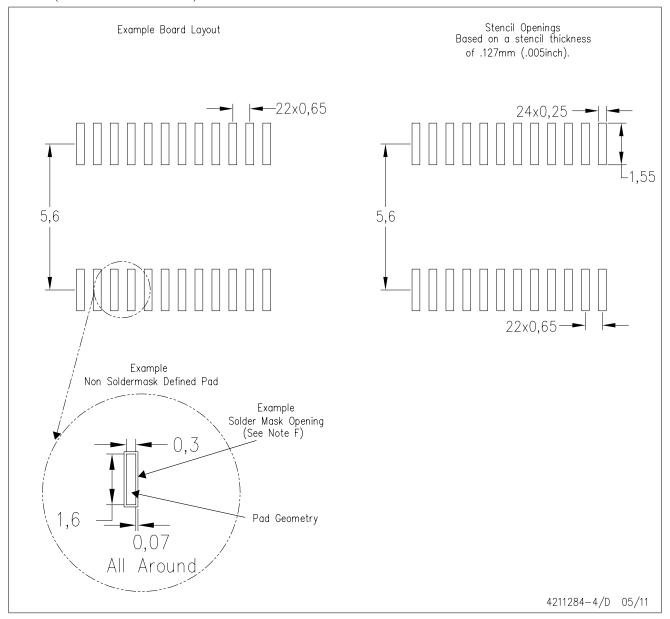
NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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