## 40MHz, 32-Channel Serial to Parallel Converter with Push-Pull Outputs

## Features

- HVCMOS ${ }^{\circledR}$ technology
- 5.0 V logic and 12 V supply rail
- Output voltage up to +200 V
- Low power level shifting
- Source/sink current minimum 50mA
- 40 MHz equivalent data rate
- Latched data outputs
- Forward and reverse shifting options (DIR pin)
- Chip select
- Polarity function


## General Description

The HV7620 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. This device has been designed for use as a driver for color AC plasma displays.

The device has 4 parallel 8-bit shift registers permitting data rates four times the speed of one. The data is clocked in simultaneously on all four data inputs with a single clock. Data is shifted in on a low to high transition of the clock. The latches and control logic perform the output enable function.

The DIR pin causes clockwise (CW) shifting of the data when connected to VDD1, and counterclockwise (CCW) shifting when connected to LVGND. Operation of the shift register is not affected by the $\overline{\mathrm{LE}}$ (latch enable) input. Transfer of data from the shift registers to the latches occurs when the $\overline{\mathrm{LE}}$ input is high. Data is stored in the latches when $\overline{\text { EE }}$ is low. The current source on the logic inputs provides active pull up when the input pins are open.

## Functional Block Diagram



## Ordering Information

|  | 64-Lead PQFP (3-sided) |
| :---: | :---: |
| Device | 20.00x14.00mm body |
|  | 3.40 mm height (max) |
| 0.80 mm pitch |  |
|  | 3.90mm footprint |
| HV7620 | HV7620PG-G |

-G indicates package is RoHS compliant ('Green')


## Absolute Maximum Ratings

| Parameter | Value |
| :--- | ---: |
| Supply voltage, $\mathrm{V}_{\mathrm{DD} 1}$ | -0.5 V to +15 V |
| Supply voltage, $\mathrm{V}_{\mathrm{DD} 2}$ | -0.5 V to +15 V |
| Supply voltage, $\mathrm{V}_{\mathrm{PP}}$ | -0.5 V to +225 V |
| Logic input levels | -2.0 V to $\mathrm{V}_{\mathrm{DD} 1}+2.0 \mathrm{~V}$ |
| Continuous total power dissipation ${ }^{1}$ | 1200 mW |
| Operating temperature range | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| Storage temperature range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

## Notes:

1. For operation above $25^{\circ} \mathrm{C}$ ambient derate linearly to maximum operating temperature at $20 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$.

## Recommended Operating Conditions

| Sym | Parameter |  | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{DD} 1}$ | Logic supply voltage |  | 4.5 | $\mathrm{V}_{\mathrm{DD} 2}$ | V |
| $\mathrm{V}_{\mathrm{DD} 2}$ | 12 V supply voltage |  | 10.8 | 13.2 | V |
| $V_{\text {PP }}$ | High voltage supply voltage |  | 50 | 200 | V |
| $\mathrm{V}_{\text {IH }}$ | High-level input voltage |  | $\mathrm{V}_{\mathrm{DD} 1}-0.5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{DD} 1}$ | V |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  | 0 | 0.5 | V |
| $\mathrm{f}_{\text {CLK }}$ | Clock frequency | $\mathrm{V}_{\mathrm{DD} 1}=5.0 \mathrm{~V}$ | - | 10 | MHz |
|  |  | $\mathrm{V}_{\mathrm{DD} 1}=12 \mathrm{~V}$ | - | 5 | MHz |
| $\mathrm{T}_{\text {A }}$ | Operating temperature range |  | -40 | +85 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{I}_{\mathrm{OD}}$ | Allowable pulsed current through output diodes ${ }^{1}$ |  | - | 500 | mA |
| $\mathrm{I}_{\text {GND(VPP) }}$ | Allowable pulsed $\mathrm{V}_{\text {PP }}$ or HVGND current ${ }^{1}$ |  | - | 16 | A |
| $\mathrm{V}_{\text {PP(SLEW }}$ | Slew rate of $\mathrm{V}_{\mathrm{PP}}$ |  | - | 340 | $\mathrm{V} / \mu \mathrm{s}$ |

Notes:

1. The current pulse width $=500 \mathrm{~ns}$, duty cycle $=5 \%$.

DC Electrical Characteristics
(Over operating supply voltages and temperature, unless otherwise noted, $V_{D D 1}=5.0 \mathrm{~V}, V_{D D 2}=12 \mathrm{~V}, V_{P P}=200 \mathrm{~V}$ and $T_{A}=25^{\circ} \mathrm{C}$ )

| Sym | Parameter |  | Min | Max | Units | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{DD} 1}$ | $\mathrm{V}_{\mathrm{DD} 1}$ supply current |  | - | 5.0 | mA | $\mathrm{f}_{\text {CLK }}=10 \mathrm{MHz}$ |
| $\mathrm{I}_{\mathrm{DD} 2}$ | $\mathrm{V}_{\mathrm{DD} 2}$ supply current |  | - | 20 | mA | $\mathrm{V}_{\mathrm{DD} 2}=13.2 \mathrm{~V}, \mathrm{f}_{\mathrm{CLK}}=10 \mathrm{MHz}$ |
| $\mathrm{I}_{\text {PP }}$ | High voltage supply current |  | - | 2.0 | mA | All outputs high or low |
| $\mathrm{I}_{\mathrm{DD1Q}}$ | Quiescent $\mathrm{V}_{\mathrm{DD} 1}$ supply current |  | - | 100 | $\mu \mathrm{A}$ | All input $=\mathrm{V}_{\mathrm{DD} 1}$ |
| $\mathrm{I}_{\mathrm{DD2Q}}$ | Quiescent $\mathrm{V}_{\mathrm{DD} 2}$ supply current |  | - | 100 | $\mu \mathrm{A}$ | All input $=V_{\text {DD1 }}$ |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output | $\mathrm{HV}_{\text {OUT }}$ | 185 | - | V | $\mathrm{I}_{0}=-50 \mathrm{~mA}$ |
|  |  | Data OUT | $\mathrm{V}_{\mathrm{DD}}-1$ | - |  | $\mathrm{I}_{0}=-100 \mu \mathrm{~A}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output | $\mathrm{HV}_{\text {OUT }}$ | - | 20 | V | $\mathrm{I}_{0}=+50 \mathrm{~mA}$ |
|  |  | Data OUT | - | 1.0 |  | $\mathrm{I}_{\mathrm{O}}=+100 \mu \mathrm{~A}$ |
| $\mathrm{I}_{\mathrm{H}}$ | High-level logic input current |  | - | 1.0 | $\mu \mathrm{A}$ | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{DD} 1}$ |
| $\mathrm{I}_{\text {LL }}$ | Low-level logic input current |  | - | -10 | $\mu \mathrm{A}$ | $\mathrm{V}_{\text {IN }}=0 \mathrm{~V}$ |
| $V_{G G}$ | HVGND to LVGND voltage difference |  | -1.0 | 1.0 | V | --- |

## AC Electrical Characteristics

(Logic signal inputs and data inputs have $t_{r} t_{f} \leq 5 n s . V_{D D 1}=5.0 \mathrm{~V}$ or $12 \mathrm{~V}, V_{D D 2}=12 \mathrm{~V}, V_{P P}=200 \mathrm{~V}$ )

| Sym | Parameter |  | Min | Max | Units | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{f}_{\text {CLK }}$ | Clock frequency | $\mathrm{V}_{\mathrm{DD1} 1}=5.0 \mathrm{~V}$ | - | 10 | MHz | Per register, $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |
|  |  | $\mathrm{V}_{\mathrm{DD} 1}=12 \mathrm{~V}$ | - | 5.0 |  |  |
| $t_{\text {wL }}, t_{\text {wH }}$ | Clock width high or low |  | 40 | - | ns | --- |
| $\mathrm{t}_{\mathrm{su}}$ | Data set-up time before clock rises |  | 20 | - | ns | --- |
| $\mathrm{t}_{\mathrm{H}}$ | Data hold time after clock rises |  | 20 | - | ns | --- |
| $\mathrm{t}_{\text {ON }}, \mathrm{t}_{\text {OFF }}$ | Time from latch enable to $\mathrm{HV}_{\text {OUt }}$ |  | - | 275 | ns | $C_{L}=15 \mathrm{pF}$ |
| $t_{\text {wLE }}$ | $\overline{\mathrm{LE}}$ pulse width |  | 25 | - | ns | --- |
| $\mathrm{t}_{\text {DLE }}$ | Delay time clock to $\overline{\mathrm{LE}}$ low to high |  | 50 | - | ns | --- |
| $\mathrm{t}_{\text {SLE }}$ | $\overline{\mathrm{LE}}$ set-up time before clock rises |  | 20 | - | ns | --- |
| $t_{\text {DLF }} \mathrm{t}_{\text {DLN }}$ | $\overline{\mathrm{BL}}$ or CS low to high to $\mathrm{HV}_{\text {out }}$ |  | - | 250 | ns | --- |
| $\mathrm{t}_{\text {COF }}, \mathrm{t}_{\text {CON }}$ | Clock to $\mathrm{HV}_{\text {Out }}$ |  | - | 275 | ns | --- |
| $\mathrm{t}_{\text {DLH }}$ | Delay time clock to data low to high |  | - | 100 | ns | $C_{L}=15 \mathrm{pF}$ |
| $\mathrm{t}_{\text {DHL }}$ | Delay time clock to data high to low |  | - | 100 | ns | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |

## Input and Output Equivalent Circuits



Logic Data Output

High Voltage Outputs

## Switching Waveforms



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Function Table

|  | Inputs |  |  |  |  |  |  |  |  |  |  |  |  | HV ${ }_{\text {OUT }}$ |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Function | $\mathrm{D}_{1 \times} \mathrm{A}$ | $\mathrm{D}_{\text {IN }} \mathrm{B}$ | $\mathrm{D}_{\text {IN }} \mathrm{C}$ | $\mathrm{D}_{\text {IN }} \mathrm{D}$ | CLK | LE | DIR | $\overline{\text { BLA }}$ | $\overline{\text { BLB }}$ | $\overline{\text { BLC }}$ | $\overline{\text { BLD }}$ | CS | $\overline{\text { POL }}$ | A | B | C | D |
| All O/P High | X | X | X | X | X | X | X | X | X | X | X | L | L | H | H | H | H |
| All O/P Low | X | X | X | X | X | X | X | X | X | X | X | L | H | L | L | L | L |
| "A" ${ }^{+}$ <br> Outputs Low | X | X | X | X | X | X | X | L | X | X | X | X | H | L | * | * | * |
| Normal Polarity | X | X | X | X | X | X | X | H | H | H | H | H | H |  | No Inv | ersion |  |
| Outputs Inverted | X | X | X | X | X | X | X | H | H | H | H | H | L |  | Inve | sion |  |
| Transparent Mode | H | L | L | L | $\uparrow$ | H | X | H | H | H | H | H | H | H | L | L | L |
| Data Stored | X | X | X | X | X | L | X | H | H | H | H | H | H |  | Store | data |  |
| Shift CW ${ }^{\text {A }}$ | X | X | X | X | $\uparrow$ | H | H | H | H | H | H | H | X | $\xrightarrow[\mathrm{A}_{\mathrm{N+1}}]{\mathrm{A}_{\mathrm{N}}}$ | $\xrightarrow[B_{N+1}]{\mathrm{B}_{\mathrm{N}}}$ | $\xrightarrow[C_{N+1}]{\mathrm{C}_{\mathrm{N}}}$ | $\xrightarrow[D_{N+1}]{D_{N}}$ |
| Shift CCW ${ }^{\text {B }}$ | X | X | X | X | $\uparrow$ | H | L | H | H | H | H | H | X | $\xrightarrow[\mathrm{A}_{\mathrm{N}-1}]{\mathrm{A}_{\mathrm{N}}}$ | $\xrightarrow[\mathrm{B}_{\mathrm{N}-1}]{\mathrm{B}_{\mathrm{N}}}$ | $\xrightarrow[\mathrm{C}_{\mathrm{N}-1}]{\mathrm{C}_{\mathrm{N}}}$ | $\xrightarrow[D_{N-1}]{D_{N}}$ |

## Notes:

$H=$ High level, $L=$ Low level, $X=$ Irrelevant, $\uparrow=$ Low to high transition.

* = Dependent on previous stage's state before the last $C L K \uparrow$ for last $\overline{L E}$ high.
$t=\overline{B L B}, \overline{B L C}$ and $\overline{B L D}$ will have similar effect on their respective output.
$A=$ When Shift CW is selected, $D_{\text {IN }}$ is input and $D_{\text {out }}$ is output.
$B=$ When Shift CCW is selected, $D_{\text {IN }}$ is output and $D_{\text {out }}$ is input.


## Power-up sequence:

1. GND (HV, LV)
2. $V_{D D 1}$
3. $V_{D D 2}$
4. Logic Input Signals

To power down reverse the sequence above.

Pin Function

| Pin \# | Function |
| :---: | :---: |
| 1 | HVGND |
| 2 | VPP |
| 3 | HV ${ }_{\text {OUT }}$ D8 |
| 4 | $\mathrm{HV}_{\text {OUT }} \mathrm{C} 8$ |
| 5 | $\mathrm{HV}_{\text {OUT }} \mathrm{B} 8$ |
| 6 | $\mathrm{HV}_{\text {OUT }} \mathrm{A} 8$ |
| 7 | HV ${ }_{\text {OUT }}$ D7 |
| 8 | $\mathrm{HV}_{\text {OUT }} \mathrm{C} 7$ |
| 9 | $\mathrm{HV}_{\text {OUT }} \mathrm{B7}$ |
| 10 | $\mathrm{HV}_{\text {OUT }} \mathrm{A} 7$ |
| 11 | $\mathrm{HV}_{\text {Out }} \mathrm{D} 6$ |
| 12 | $\mathrm{HV}_{\text {OUT }} \mathrm{C} 6$ |
| 13 | $\mathrm{HV}_{\text {OUT }} \mathrm{B6}$ |
| 14 | $\mathrm{HV}_{\text {out }} \mathrm{A} 6$ |
| 15 | $\mathrm{HV}_{\text {OUT }} \mathrm{D} 5$ |
| 16 | $\mathrm{HV}_{\text {OUT }} \mathrm{C} 5$ |


| Pin \# | Function |
| :---: | :---: |
| 17 | HV $_{\text {ouT }}$ B5 |
| 18 | HV $_{\text {ouT }}$ A5 |
| 19 | VPP |
| 20 | HVGND |
| 21 | HVGND |
| 22 | VDD2 |
| 23 | $\overline{\text { BLC }}$ |
| 24 | $\overline{\text { BLD }}$ |
| 25 | $\overline{\text { LE }}$ |
| 26 | $\mathrm{D}_{\text {ouT }} \mathrm{D}$ |
| 27 | $\mathrm{D}_{\text {IN }} \mathrm{D}$ |
| 28 | $\mathrm{D}_{\text {IN }} \mathrm{C}$ |
| 29 | $\mathrm{D}_{\text {ouT }} \mathrm{C}$ |
| 30 | $\overline{\text { POL }}$ |
| 31 | LVGND |
| 32 | DIR |


| Pin \# | Function |
| :---: | :---: |
| 33 | CS |
| 34 | $\mathrm{D}_{\text {out }} \mathrm{B}$ |
| 35 | $\mathrm{D}_{\text {IN }} \mathrm{B}$ |
| 36 | $\mathrm{D}_{\text {IN }} \mathrm{A}$ |
| 37 | $\mathrm{D}_{\text {out }} \mathrm{A}$ |
| 38 | CLK |
| 39 | $\overline{\text { BLA }}$ |
| 40 | $\overline{\text { BLB }}$ |
| 41 | VDD1 |
| 42 | LVGND |
| 43 | N/C |
| 44 | HVGND |
| 45 | HVGND |
| 46 | VPP |
| 47 | HV ${ }_{\text {out }}$ D4 |
| 48 | HV ${ }_{\text {ouT }} C 4$ |


| Pin \# | Function |
| :---: | :---: |
| 49 | HV ${ }_{\text {OUT }}$ B4 |
| 50 | HV ${ }_{\text {out }}$ A4 |
| 51 | $\mathrm{HV}_{\text {OUT }} \mathrm{D} 3$ |
| 52 | $\mathrm{HV}_{\text {OUT }} \mathrm{C} 3$ |
| 53 | $\mathrm{HV}_{\text {out }} \mathrm{B} 3$ |
| 54 | $\mathrm{HV}_{\text {out }} \mathrm{A} 3$ |
| 55 | $\mathrm{HV}_{\text {OUT }} \mathrm{D} 2$ |
| 56 | $\mathrm{HV}_{\text {OUT }} \mathrm{C} 2$ |
| 57 | $\mathrm{HV}_{\text {Out }} \mathrm{B}^{\text {a }}$ |
| 58 | $\mathrm{HV}_{\text {OUT }} \mathrm{A}^{\text {2 }}$ |
| 59 | $\mathrm{HV}_{\text {OUT }} \mathrm{D} 1$ |
| 60 | $\mathrm{HV}_{\text {Out }} \mathrm{C} 1$ |
| 61 | $\mathrm{HV}_{\text {OUT }} \mathrm{B} 1$ |
| 62 | $\mathrm{HV}_{\text {out }} \mathrm{A} 1$ |
| 63 | VPP |
| 64 | HVGND |

## 64-Lead PQFP (3-Sided) Package Outline (PG)

## $20.00 \times 14.00 \mathrm{~mm}$ body, 3.40 mm height (max), 0.80 mm pitch, 3.90 mm footprint



## Top View



View B

Note:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. The leads on this side are trimmed.

| Symbol |  | A | A1 | A2 | b | D | D1 | E | E1 | e | L | L1 | L2 | L3 | $\theta$ | 01 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Dimen- <br> sion <br> (mm) | MIN | 2.80 | 0.25 | 2.55 | 0.30 | 22.25 | 19.80 | 17.65 | 13.80 | $\begin{aligned} & 0.80 \\ & \text { BSC } \end{aligned}$ | 0.73 | $\begin{aligned} & 1.95 \\ & \text { REF } \end{aligned}$ | $\begin{aligned} & 0.25 \\ & \text { BSC } \end{aligned}$ | $\begin{aligned} & 0.55 \\ & \text { REF } \end{aligned}$ | $0^{\circ}$ | $5^{\circ}$ |
|  | NOM | - | - | 2.80 | - | 22.50 | 20.00 | 17.90 | 14.00 |  | 0.88 |  |  |  | 3.50 | - |
|  | MAX | 3.40 | 0.50 | 3.05 | 0.45 | 22.75 | 20.20 | 18.15 | 14.20 |  | 1.03 |  |  |  | $7^{\circ}$ | $16^{\circ}$ |

## Drawings not to scale.

Supertex Doc. \#: DSPD-64PQFPPG, Version NR090608.
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

[^0]
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