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- 2-V to 6-V V_{CC} Operation
- Inputs Accept Voltages to 6 V
- Max t_{pd} of 10.5 ns at 5 V
- 3-State Inverting Outputs Drive Bus Lines Directly
- Full Parallel Access for Loading

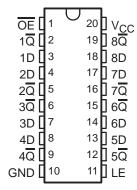
description/ordering information

The 'AC533 devices are octal transparent D-type latches with 3-state outputs. When the latch-enable (LE) input is high, the $\overline{\mathbb{Q}}$ outputs follow the complements of the data (D) inputs. When LE is taken low, the $\overline{\mathbb{Q}}$ outputs are latched at the inverse logic levels set up at the D inputs.

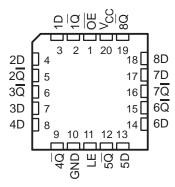
A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

SN54AC533 . . . J OR W PACKAGE SN74AC533 . . . DB, DW, N, NS, OR PW PACKAGE (TOP VIEW)



SN54AC533 . . . FK PACKAGE (TOP VIEW)



To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

TA	PACKAGI	Ε†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	PDIP – N	Tube	SN74AC533N	SN74AC533N	
	COIC DW	Tube	SN74AC533DW	10500	
	SOIC - DW	Tape and reel	SN74AC533DWR	AC533	
-40°C to 85°C	SOP - NS	Tape and reel	SN74AC533NSR	AC533	
	SSOP – DB	Tape and reel	SN74AC533DBR	AC533	
	TOOOD DW	Tube	SN74AC533PW	10500	
	TSSOP – PW	Tape and reel	SN74AC533PWR	AC533	
	CDIP – J	Tube	SNJ54AC533J	SNJ54AC533J	
–55°C to 125°C	CFP – W	Tube	SNJ54AC533W	SNJ54AC533W	
	LCCC – FK	Tube	SNJ54AC533FK	SNJ54AC533FK	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

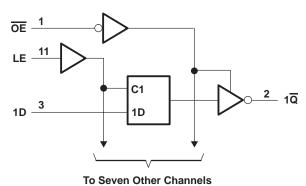


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FUNCTION TABLE (each latch)

	INPUTS	OUTPUT	
OE	LE	D	Q
L	Н	Н	L
L	Н	L	Н
L	L	Χ	\overline{Q}_0
Н	X	Χ	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V to 7 V
Input voltage range, V _I (see Note 1)		. -0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Note 1)		$0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)		±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CO}	c)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	-	±50 mA
Continuous current through V _{CC} or GND		±200 mA
Package thermal impedance, θ _{JA} (see Note 2):	: DB package	70°C/W
	DW package	58°C/W
	N package	69°C/W
	NS package	60°C/W
	PW package	83°C/W
Storage temperature range, T _{stq}		-65° C to 150° C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Note 3)

			SN54A	C533	SN74A	C533	
			MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage		2	6	2	6	V
		V _{CC} = 3 V	2.1		2.1		
V_{IH}	High-level input voltage	$V_{CC} = 4.5 \text{ V}$	3.15		3.15		V
		$V_{CC} = 5.5 \text{ V}$	3.85		3.85		
		V _{CC} = 3 V		0.9		0.9	
VIL	Low-level input voltage	$V_{CC} = 4.5 V$		1.35		1.35	V
		V _{CC} = 5.5 V		1.65		1.65	
VI	Input voltage		0	Vcc	0	Vcc	V
VO	Output voltage		0	Vcc	0	Vcc	V
		V _{CC} = 3 V	200	-12		-12	
loh	High-level output current	V _{CC} = 4.5 V	Q.	-24		-24	mA
		V _{CC} = 5.5 V		-24		-24	
		V _{CC} = 3 V		12		12	
lOL	Low-level output current	V _{CC} = 4.5 V		24		24	mA
		V _{CC} = 5.5 V		24		24	
Δt/Δν	Input transition rise or fall rate			8		8	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST SOMBITIONS	,,	T,	Δ = 25°C	SN54A	C533	SN74A	C533	
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP MA	K MIN	MAX	MIN	MAX	UNIT
		3 V	2.9		2.9		2.9		
	I _{OH} = -50 μA	4.5 V	4.4		4.4		4.4		
.,		5.5 V	5.4		5.4		5.4		.,
VOH	I _{OH} = -12 mA	3 V	2.56		2.4	N.	2.46		V
	24 == 4	4.5 V	3.86		3.7	Z.	3.76		
	$I_{OH} = -24 \text{ mA}$	5.5 V	4.86		4.7	70	4.76		
		3 V		0.	1 4	0.1		0.1	.,
	I _{OL} = 50 μA	4.5 V		0.	1 2	0.1		0.1	
		5.5 V		0.	1 0	0.1		0.1	
VOL	I _{OL} = 12 mA	3 V		0.3	6	0.5		0.44	V
		4.5 V		0.3	6	0.5		0.44	
	I _{OL} = 24 mA	5.5 V		0.3	6	0.5		0.44	
loz	V _O = V _{CC} or GND	5.5 V		±0.2	5	±5		±2.5	μΑ
l _l	V _I = V _{CC} or GND	5.5 V		±0.	1	±1		±1	μΑ
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4	80		40	μΑ
C _i	$V_I = V_{CC}$ or GND	5 V		4.5		·		·	pF

SN54AC533, SN74AC533 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

	-		T _A = 25°C		SN54AC533		SN74AC533	
			MAX	MIN	MAX	MIN	MAX	UNIT
t _W	Pulse duration, LE high	6		85	EN	6.5		ns
t _{su}	Setup time, data before LE↓	5.5		7.5	EV.	6		ns
th	Hold time, data after LE↓	1.5		2.5	1	1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

		$T_A = 25$	5°C	SN54AC533	SN74A	C533	
			MAX	MIN MAX	MIN	MAX	UNIT
t _W	Pulse duration, LE high	4.5		6.55	5		ns
t _{su}	Setup time, data before LE↓	4		6	4.5		ns
th	Hold time, data after LE↓	1.5		2.5	1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

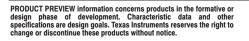
BABAMETER	FROM	то	T _A = 1	25°C	SN54AC533		SN74AC533		LINUT
PARAMETER	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
^t PLH	6	Ια	2	14	1	17.5	1.5	16	
^t PHL	D	α	2	13	1	16	1.5	14.5	ns
t _{PLH}	LE	ĪQ		14.5	1	18	1.5	16.5	20
^t PHL	LE	α	2	13	1,	16	1.5	14.5	ns
^t PZH	ŌĒ	Ια	2	12.5	37	15.5	1.5	14	
^t PZL	OE	α	2	12.5	90	15.5	1.5	14	ns
t _{PHZ}	ŌĒ	Ια	2	13	2 1	16	1.5	14.5	ns
t _{PLZ}	OE	y	2	13	1	16	1.5	14.5	115

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

BABAMETER	FROM	то	T _A = 1	25°C	SN54A	C533	SN74A	C533	
PARAMETER	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
^t PLH	6	ρl	2	10	1	12.5	1.5	11	
^t PHL	D	α	2	9.5	1	12	1.5	10.5	ns
^t PLH		· Q		10.5	1	13	1.5	11.5	
^t PHL	LE	α	2	10	1,4	13	1.5	11	ns
^t PZH	ŌĒ	ρl	2	9.5	(b)	12	1.5	10.5	
^t PZL	OE	α	2	9.5	70	12	1.5	10.5	ns
^t PHZ	<u>OE</u>	ρl	2	10	<u>ا</u> ر	12.5	1.5	11	ns
^t PLZ	OE	ά	2	10	1	12.5	1.5	11	115

operating characteristics, V_{CC} = 5 V, T_A = 25°C

		PARAMETER	TEST CO	TYP	UNIT	
ı	C _{pd}	Power dissipation capacitance	$C_L = 50 \text{ pF},$	f = 1 MHz	40	pF

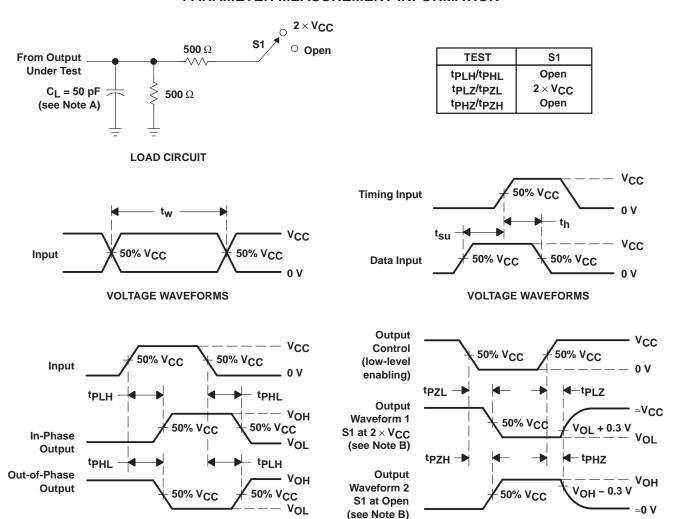




VOLTAGE WAVEFORMS

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50~\Omega$, $t_f \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

20-Aug-2011

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74AC533DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	
SN74AC533DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC533DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC533DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC533DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC533DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC533DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC533DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC533DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC533N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AC533NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AC533NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC533NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC533NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC533PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC533PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC533PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC533PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	

⁽¹⁾ The marketing status values are defined as follows:



PACKAGE OPTION ADDENDUM

20-Aug-2011

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

All difficultions are norminal	ı				1	1		1		1		
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC533DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AC533DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74AC533NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC533DBR	SSOP	DB	20	2000	346.0	346.0	33.0
SN74AC533DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74AC533NSR	SO	NS	20	2000	346.0	346.0	41.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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