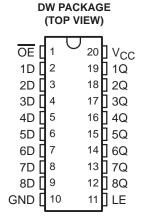
- Qualified for Automotive Applications
- ESD Protection Exceeds 1500 V Per MIL-STD-883, Method 3015; Exceeds 150 V Using Machine Model (C = 200 pF, R = 0)
- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17



### description/ordering information

The SN74AHCT573 is an octal transparent D-type latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable  $(\overline{OE})$  input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

 $\overline{\text{OE}}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

#### ORDERING INFORMATION<sup>†</sup>

TA	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC - DW	Tape and reel	SN74AHCT573QDWRQ1	AHCT573QQ1

<sup>†</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

### FUNCTION TABLE (each latch)

	OUTPUT		
OE	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	$Q_0$
Н	Χ	Χ	Z

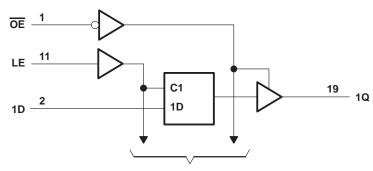


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<sup>‡</sup> Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

### logic diagram (positive logic)



To Seven Other Channels

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, $V_{CC}$ Input voltage range, $V_{I}$ (see Note 1) Output voltage range, $V_{O}$ (see Note 1) Input clamp current, $I_{IK}$ ( $V_{I}$ < 0) Output clamp current, $I_{OK}$ ( $V_{O}$ < 0 or $V_{O}$ > $V_{CC}$ ) Continuous output current, $I_{O}$ ( $V_{O}$ = 0 to $V_{CC}$ ) Continuous current through $V_{CC}$ or GND Package thermal impedance, $\theta_{JA}$ (see Note 2)	$\begin{array}{llllllllllllllllllllllllllllllllllll$
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level input voltage	2		V
V <sub>IL</sub>	Low-level input voltage		0.8	V
VI	Input voltage	0	5.5	V
Vo	Output voltage	0	VCC	V
loh	High-level output current		-8	mA
loL	Low-level output current		8	mA
Δt/Δν	Input transition rise or fall rate		20	ns/V
TA	Operating free-air temperature	-40	125	°C

NOTE 3: All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST SOMBITIONS	.,	T <sub>A</sub> = 25°C				MAY	
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	UNIT
\/a	$I_{OH} = -50 \mu A$	451/	4.4	4.5		4.4		.,
Voн	$I_{OH} = -8 \text{ mA}$	4.5 V	3.94			3.8		V
\/a.	$I_{OL} = 50 \mu A$	4.5 V			0.1		0.1	V
VoL	$I_{OL} = 8 \text{ mA}$	4.5 V			0.36		0.44	V
lį	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	μΑ
loz	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5	μΑ
Icc	$V_{I} = 5.5 \text{ V or GND},  I_{O} = 0$	5.5 V			4		40	μΑ
∆l <sub>CC</sub> †	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	mA
C <sub>i</sub>	$V_I = V_{CC}$ or GND	5 V		2.5	10			pF
Co	$V_O = V_{CC}$ or GND	5 V		3				pF

<sup>†</sup>This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or VCC.

# timing requirements over recommended operating free-air temperature range, $\rm V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

		T <sub>A</sub> = 25°C		MINI	BAAV	LINUT
		MIN	MAX	MIN	MAX	UNIT
t <sub>W</sub>	Pulse duration, LE high	5		5		ns
t <sub>su</sub>	Setup time, data before LE↓	3.5		3.5		ns
th	Hold time, data after LE↓	1.5		1.5		ns

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

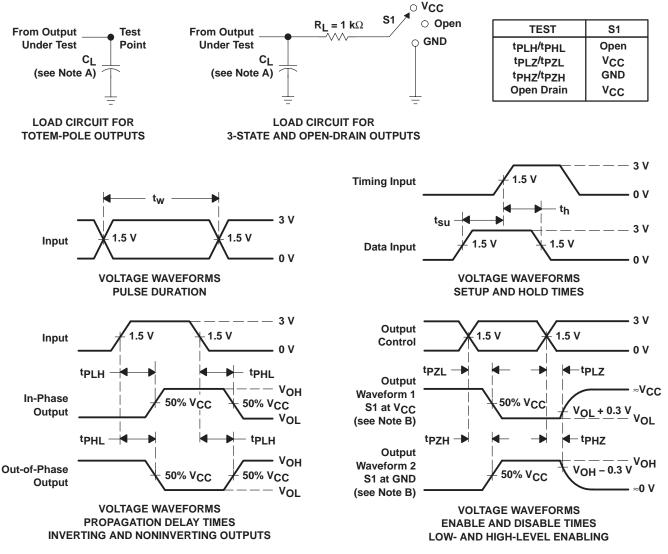
DADAMETED	FROM	ТО	LOAD	T	λ = 25°C	;	NAIN.	MAY	LINIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	UNIT
tPLH	D	0	0. 45 = 5		4.2	6	1	6.5	
<sup>t</sup> PHL	U	Q	C <sub>L</sub> = 15 pF		5.1	7	1	9	ns
t <sub>PLH</sub>	- [	0	0. 45		4.7	6.5	1	7.5	
t <sub>PHL</sub>	LE	Q	C <sub>L</sub> = 15 pF		5.6	7.5	1	9	ns
<sup>t</sup> PZH	ŌĒ	0	0 45 -5		4.1	6.5	1	7	
tPZL	OE	Q	C <sub>L</sub> = 15 pF		5.5	7.5	1	10	ns
t <sub>PHZ</sub>	ŌĒ	_	0 45 -5		5.5	8	1	11	
tPLZ	OE	Q	C <sub>L</sub> = 15 pF		5.4	8	1	9.5	ns
t <sub>PLH</sub>	6		0. 50.5		5.2	7	1	7.5	
t <sub>PHL</sub>	D	Q	C <sub>L</sub> = 50 pF		6.1	8	1	10	ns
t <sub>PLH</sub>	- [		0. 50.5		5.7	7.5	1	8.5	
<sup>t</sup> PHL	LE	Q C <sub>L</sub> = 50			6.6	8.5	1	10	ns
<sup>t</sup> PZH	ŌĒ	0	0 50 - 5		5.1	7.5	1	8	
tPZL	OE	Q	$C_L = 50 pF$		6.5	8.5	1	11	ns
t <sub>PHZ</sub>	ŌĒ	0	0. 50.5		6.7	9	1	12	
tPLZ	UE	Q	C <sub>L</sub> = 50 pF		6.4	9	1	10.5	ns
tsk(o)			C <sub>L</sub> = 50 pF			1.5			ns



### operating characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER		ONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load,	f = 1 MHz	16	pF

### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq 3$  ns,  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



### PACKAGE OPTION ADDENDUM

www.ti.com 11-Jun-2009

### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins Pa	ackage Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74AHCT573QDWRQ1	ACTIVE	SOIC	DW	20 2	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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### OTHER QUALIFIED VERSIONS OF SN74AHCT573-Q1:

Catalog: SN74AHCT573Military: SN54AHCT573

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

DW (R-PDSO-G20)

### PLASTIC SMALL OUTLINE



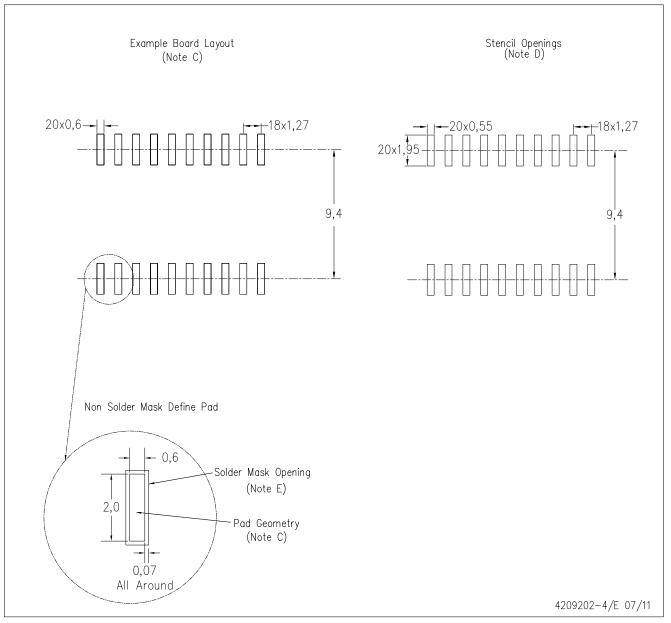
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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