SCLS411I – APRIL 1998 – REVISED APRIL 2005

- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 8 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V , T_A = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54LV573A . . . J OR W PACKAGE SN74LV573A ... RGY PACKAGE SN54LV573A ... FK PACKAGE SN74LV573A ... DB, DGV, DW, NS, (TOP VIEW) (TOP VIEW) **OR PW PACKAGE** ₽₩°°°ã 202 (TOP VIEW) Ш 20 🛛 V_{CC} OE [1 20 3 2 1 20 19 3D 18 2Q 4 1D 2 19 1Q 1D 2 19 1Q 4D 17 3Q 5 2D Πз 18 🛛 2Q 2D 3 18 2Q 5D 16 4Q 3D 6 3D 17 🛛 3Q 4 17 3Q 4 6D Π7 15 5Q 4D 4D 5 16 4Q 5 16 🛛 4Q 7D 14 6Q 8 | 5D 6 15 5Q 5D 6 15 🛛 5Q 9 10 11 12 13 6Q 6D 7 14 6D Π7 14 🛛 6Q 7D 8 13 7Q DND DNE Щãã 7D П 8 13 7Q 12 8Q 8D 9 12 8Q 8D 9 GND 10 11 🛛 LE 10 11 Щ GND

description/ordering information

T _A	РАСКА	GE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	QFN – RGY	Reel of 1000	SN74LV573ARGYR	LV573A
		Tube of 25	SN74LV573ADW	11/5704
10°C to 95°C	SOIC – DW	Reel of 2000	SN74LV573ADWR	LV573A
	SOP – NS	Reel of 2000	SN74LV573ANSR	74LV573A
	SSOP – DB Reel of 2000		SN74LV573ADBR	LV573A
–40°C to 85°C		Tube of 70	SN74LV573APW	
	TSSOP – PW	Reel of 2000	SN74LV573APWR	LV573A
		Reel of 250	SN74LV573APWT	
	TVSOP – DGV	Reel of 2000	SN74LV573ADGVR	LV573A
	VFBGA – GQN	Reel of 1000	SN74LV573AGQNR	LV573A
	CDIP – J	Tube of 20	SNJ54LV573AJ	SNJ54LV573AJ
–55°C to 125°C	CFP – W	Tube of 85	SNJ54LV573AW	SNJ54LV573AW
	LCCC – FK	Tube of 55	SNJ54LV573AFK	SNJ54LV573AFK

ORDERING INFORMATION

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN54LV573A, SN74LV573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS SCLS4111 – APRIL 1998 – REVISED APRIL 2005

description/ordering information (continued)

The 'LV573A devices are octal transparent D-type latches designed for 2-V to 5.5-V V_{CC} operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

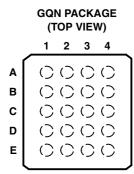
While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



terminal assignments

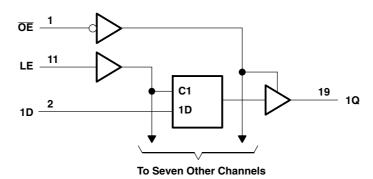
	1	2	3	4
Α	1D	OE	V _{CC}	1Q
в	3D	3Q	2D	2Q
С	5D	4D	5Q	4Q
D	7D	7Q	6D	6Q
Е	GND	8D	LE	8Q

FUNCTION TABLE

	(cuo		
	INPUTS	OUTPUT	
OE	LE	Q	
L	Н	Н	Н
L	н	L	L
L	L	Х	Q ₀
Н	Х	Х	Z



logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, FK, J, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}
or power-off state, V _O (see Note 1) –0.5 V to 7 V
Output voltage range applied in the high or low state, V_O (see Notes 1 and 2)0.5 V to V_{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)
Output clamp current, I _{OK} (V _O < 0)
Continuous output current, I_O (V _O = 0 to V _{CC}) ±35 mA
Continuous current through V _{CC} or GND ±70 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package
(see Note 3): DGV package
(see Note 3): DW package
(see Note 3): GQN package
(see Note 3): NS package
(see Note 3): PW package
(see Note 4): RGY package
Storage temperature range, T _{stg}

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

2. This value is limited to 5.5 V maximum.

3. The package thermal impedance is calculated in accordance with JESD 51-7.

4. The package thermal impedance is calculated in accordance with JESD 51-5.



SCLS4111 - APRIL 1998 - REVISED APRIL 2005

recommended operating conditions (see Note 5)

			SN54L	V573A	SN74L	/573A	
			MIN	MAX	MIN	MAX	UNIT
V _{CC}	Supply voltage		2	5.5	2	5.5	V
		$V_{CC} = 2 V$	1.5		1.5		
.,		V_{CC} = 2.3 V to 2.7 V	$V_{CC} imes 0.7$		$V_{CC} imes 0.7$.,
VIH	High-level input voltage	V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} imes 0.7$		v
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} imes 0.7$		
		$V_{CC} = 2 V$		0.5		0.5	
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} imes 0.3$		$V_{CC} imes 0.3$.,
V _{IL}	Low-level input voltage	V_{CC} = 3 V to 3.6 V		$V_{CC}\!\times\!0.3$		$V_{CC} imes 0.3$	v
		V_{CC} = 4.5 V to 5.5 V		$V_{CC}\!\times\!0.3$		$V_{CC} imes 0.3$	
VI	Input voltage		0	5.5	0	5.5	V
.,		High or low state	0	Vcc	0	V _{CC}	.,
Vo	Output voltage	3-state	0	5.5	0	5.5	V
		$V_{CC} = 2 V$		-50		-50	μA
		V_{CC} = 2.3 V to 2.7 V		5 -2		-2	
I _{OH}	High-level output current	V_{CC} = 3 V to 3.6 V	0	-8		-8	mA
		V_{CC} = 4.5 V to 5.5 V	Q	-16		-16	
		$V_{CC} = 2 V$		50		50	μA
		V_{CC} = 2.3 V to 2.7 V		2		2	
I _{OL}	Low-level output current	V_{CC} = 3 V to 3.6 V		8		8	mA
		V_{CC} = 4.5 V to 5.5 V		16		16	
		V_{CC} = 2.3 V to 2.7 V		200		200	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 3 V to 3.6 V		100		100	ns/V
		V_{CC} = 4.5 V to 5.5 V		20		20	
Τ _Α	Operating free-air temperature		-55	125	-40	85	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			SN54LV5734		SN74	ILV573A		
PARAMETER	TEST CONDITIONS	V _{cc}	MIN TYP	MAX	MIN	ΤΥΡ Ν	IAX	UNIT
	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} -0.1		V _{CC} -0.1			
N/	I _{OH} = -2 mA	2.3 V	2		2			v
V _{OH}	I _{OH} = -8 mA	3 V	2.48		2.48			v
	I _{OH} = -16 mA	4.5 V	3.8	b	3.8			
	I _{OL} = 50 μA	2 V to 5.5 V	In.	0.1			0.1	
V	$I_{OL} = 2 \text{ mA}$	2.3 V	Ho	0.4			0.4	v
V _{OL}	I _{OL} = 8 mA	3 V	10	0.44		(0.44	v
	I _{OL} = 16 mA	4.5 V	ng	0.55		(0.55	
l	$V_{I} = 5.5 V \text{ or GND}$	0 to 5.5 V	06	±1			±1	μA
I _{OZ}	$V_O = V_{CC}$ or GND	5.5 V	4	±5			±5	μA
I _{CC}	$V_{I} = V_{CC} \text{ or } GND, \qquad I_{O} = 0$	5.5 V		20			20	μA
I _{off}	V_{I} or V_{O} = 0 to 5.5 V	0		5			5	μA
Ci	$V_{I} = V_{CC}$ or GND	3.3 V	1.8			1.8		pF

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SCLS411I - APRIL 1998 - REVISED APRIL 2005

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V \pm 0.2 V (unless otherwise noted) (see Figure 1)

					SN54LV573A		SN74LV573A		
	PARAMETER			MAX	MIN	МАХ	MIN	MAX	UNIT
tw	Pulse duration	LE high	6.5		6.5	12.0	6.5		ns
t _{su}	Setup time	Data before LE \downarrow	5		5	JIP.	5		ns
t _h	Hold time	Data after LE \downarrow	2		2		2		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

	PARAMETER				SN54LV573A		SN74LV573A		LINUT
	PARAMETER			MAX	MIN	МАХ	MIN	MAX	UNIT
tw	Pulse duration	LE high	5		5	5.0	5		ns
t _{su}	Setup time	Data before LE \downarrow	3.5		3.5	JIL	3.5		ns
t _h	Hold time	Data after LE \downarrow	1.5		1,5		1.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54LV573A		SN74LV573A			
	PARAMETER				MIN	MAX	MIN	MAX	UNIT
tw	Pulse duration	LE high	5		5	12.0	5		ns
t _{su}	Setup time	Data before LE \downarrow	3.5		3.5	JIP .	3.5		ns
t _h	Hold time	Data after LE \downarrow	1.5		1,5		1.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V \pm 0.2 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	LOAD	T,	₄ = 25°C	;	SN54L	/573A	SN74L	/573A	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
•	D	Q			8.9*	15.8*	1*	18*	1	18	
t _{pd}	LE	Q	0 15 55		9.6*	16.2*	1*	19*	1	19	ns
t _{en}	ŌE	Q	C _L = 15 pF		9.3*	16.2*	1*	19*	1	19	115
t _{dis}	ŌĒ	Q			6.7*	12.6*	1*	15*	1	15	
	D	Q			10.9	18.7	T.	21	1	21	
t _{pd}	LE	Q			11.6	19.1	200	23	1	23	
t _{en}	ŌE	Q	C _L = 50 pF		11.4	19	0 لار	22	1	22	ns
t _{dis}	ŌĒ	Q			8.6	17.3	1	19	1	19	
t _{sk(o)}						2				2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.



SCLS411I - APRIL 1998 - REVISED APRIL 2005

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

	FROM	то	LOAD	Т	₄ = 25°C	;	SN54L	V573A	SN74L	/573A	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	ТҮР	MAX	MIN	MAX	MIN	MAX	UNIT
	D	Q			6.2*	11*	1*	13*	1	13	
t _{pd}	LE	Q	0 15 -5		6.8*	11.9*	1*	14*	1	14	ns
t _{en}	ŌĒ	Q	C _L = 15 pF		6.6*	11.5*	1*	13.5*	1	13.5	115
t _{dis}	ŌĒ	Q			4.9*	11*	1*	13*	1	13	
	D	Q			7.7	14.5	T.	16.5	1	16.5	
t _{pd}	LE	Q			8.2	15.4	50	17.5	1	17.5	
t _{en}	ŌE	Q	C _L = 50 pF		8	15	0 K	17	1	17	ns
t _{dis}	ŌĒ	Q	[6.2	14.5	1	16.5	1	16.5	
t _{sk(o)}						1.5				1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

	FROM	то	LOAD	Т	₄ = 25°C	;	SN54L	V573A	SN74L	/573A	
PARAMETER	(INPUT)	(OUTPUT) CAPA	CAPACITANCE	MIN	ТҮР	MAX	MIN	MAX	MIN	MAX	UNIT
	D	Q			4.3*	6.8*	1*	8*	1	8	
t _{pd}	LE	Q	0 – 15 pF		4.7*	7.7*	1*	9*	1	9	ns
t _{en}	ŌĒ	Q	C _L = 15 pF		4.7*	7.7*	1*	9*	1	9	115
t _{dis}	ŌĒ	Q			3.5*	7.7*	1*	9*	1	9	
	D	Q			5.3	8.8	T.	10	1	10	
t _{pd}	LE	Q			5.7	9.7	10	11	1	11	
t _{en}	ŌE	Q	C _L = 50 pF		5.7	9.7	Q 1	11	1	11	ns
t _{dis}	ŌĒ	Q			4.2	9.7	1	11	1	11	
t _{sk(o)}						1				1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 6)

		SN			
	PARAMETER	MIN	UNIT		
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.6	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.5	-0.8	V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		2.9		V
V _{IH(D)}	High-level dynamic input voltage	2.31			V
V _{IL(D)}	Low-level dynamic input voltage			0.99	V

NOTE 6: Characteristics are for surface-mount packages only.



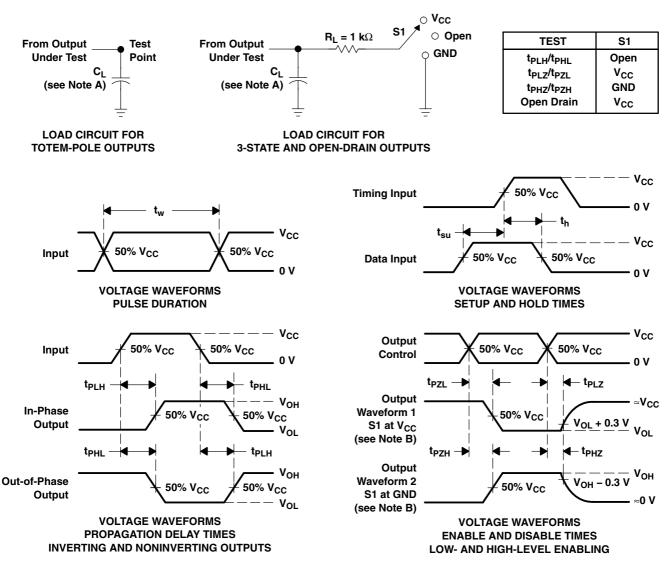
SN54LV573A, SN74LV573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS SCLS4111 – APRIL 1998 – REVISED APRIL 2005

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC}	TYP	UNIT		
C _{pd} Pov		Outputs enabled			3.3 V	16	
	Power dissipation conseitance		D to Q	C _I = 50 pF, f = 10 MH	5 V	18	pF
	Power dissipation capacitance		1540	C _L = 50 pF, f = 10 M⊦	2 3.3 V	18.2	рг
			LE to Q		5 V	21.3	



SCLS4111 - APRIL 1998 - REVISED APRIL 2005



PARAMETER MEASUREMENT INFORMATION

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_r \leq 3 ns, t_f \leq 3 ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LV573ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ADGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ADGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ADGVRG4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



20-Aug-2011

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LV573APWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573APWTE4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573APWTG4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV573ARGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN74LV573ARGYRG4	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN74LV573AZQNR	ACTIVE	BGA MICROSTAR JUNIOR	ZQN	20	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)



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20-Aug-2011

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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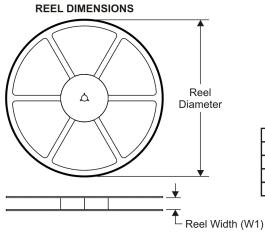
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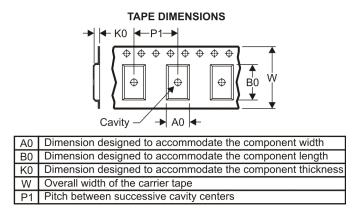
PACKAGE MATERIALS INFORMATION

www.ti.com

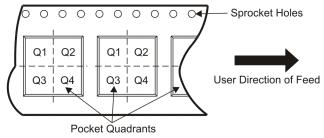
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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



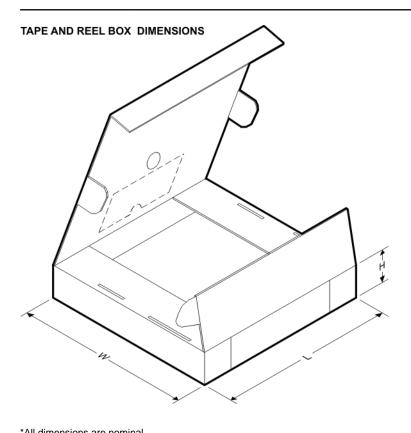
*All dimensions are nomina												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV573ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV573ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV573ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LV573ANSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74LV573APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LV573APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LV573ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
SN74LV573AZQNR	BGA MI CROSTA R JUNI OR	ZQN	20	1000	330.0	12.4	3.3	4.3	1.6	8.0	12.0	Q1

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PACKAGE MATERIALS INFORMATION

29-Jul-2011



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV573ADBR	SSOP	DB	20	2000	346.0	346.0	33.0
SN74LV573ADGVR	TVSOP	DGV	20	2000	346.0	346.0	29.0
SN74LV573ADWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74LV573ANSR	SO	NS	20	2000	346.0	346.0	41.0
SN74LV573APWR	TSSOP	PW	20	2000	346.0	346.0	33.0
SN74LV573APWT	TSSOP	PW	20	250	346.0	346.0	33.0
SN74LV573ARGYR	VQFN	RGY	20	3000	346.0	346.0	29.0
SN74LV573AZQNR	BGA MICROSTAR JUNIOR	ZQN	20	1000	340.5	338.1	20.6

ZQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BC-2.
- D. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).



MECHANICAL DATA

PLASTIC SMALL-OUTLINE

MPDS006C - FEBRUARY 1996 - REVISED AUGUST 2000

DGV (R-PDSO-G**)

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins MO-153

14/16/20/56 Pins – MO-194



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

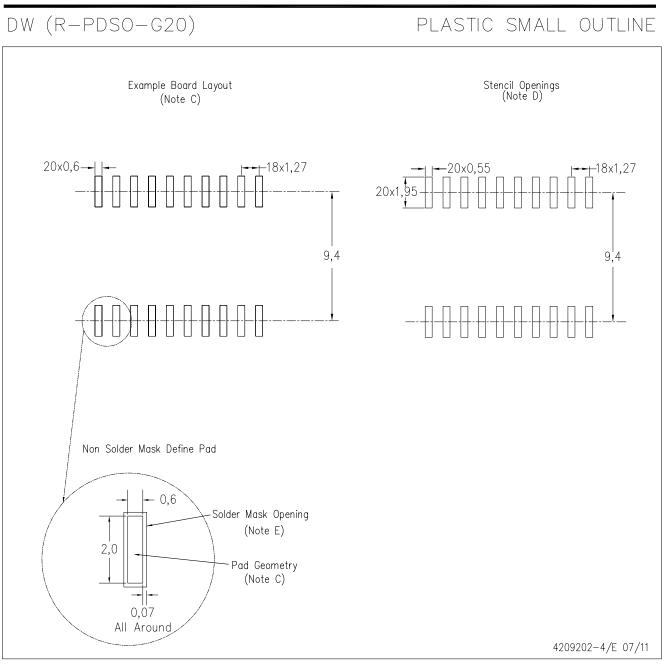
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AC.



LAND PATTERN DATA



NOTES:

A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. β . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



MECHANICAL DATA



- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.



RGY (R-PVQFN-N20)

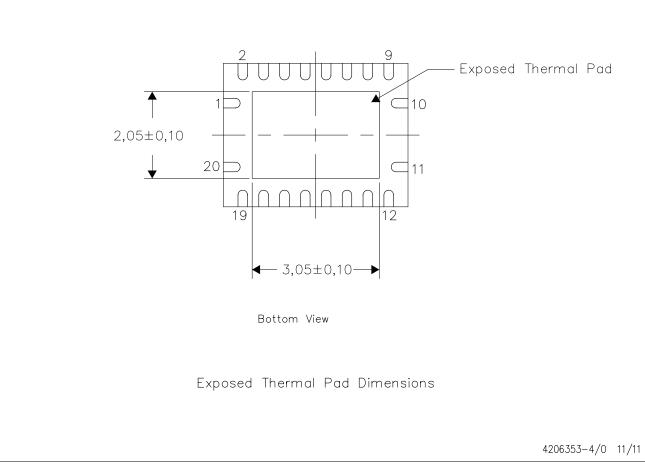
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

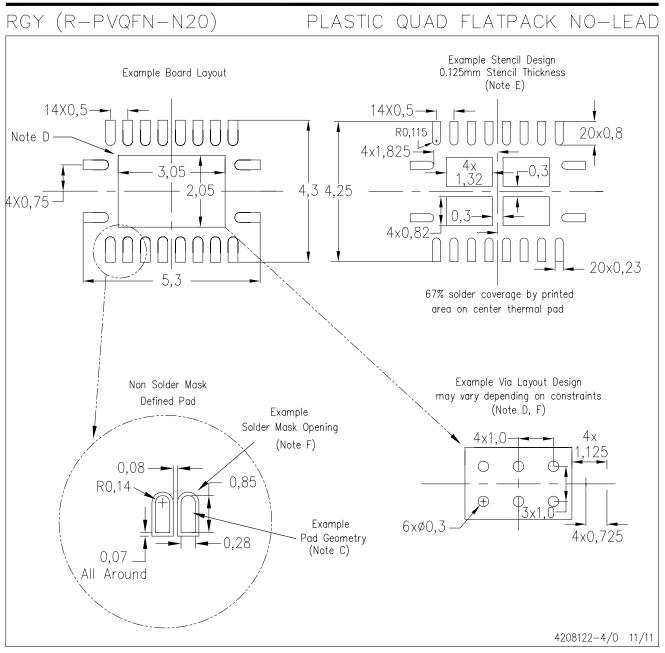
For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com.

- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



MECHANICAL DATA

MSSO002E - JANUARY 1995 - REVISED DECEMBER 2001

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150



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