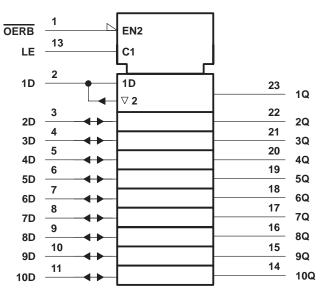
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 3-State I/O-Type Read-Back Inputs Bus-Structured Pinout 	DW OR NT PACKAGE (TOP VIEW)			
True Logic Outputs		7 ₂₄] V _{CC}		
Package Options Include Plastic	1D [] 2	23] 1Q		
Small-Outline (DW) Packages and Standard	2D 🛛 3	22 2 2Q		
Plastic (NT) 300-mil DIPs	3D 🛛 4	21 🛛 3Q		
	4D 🛛 5	20 🛛 4Q		
description	5D 🛛 6	19 🛛 5Q		
This 10-bit latch is designed specifically for storing	6D 🛛 7	18 🛛 6Q		
the contents of the input data bus and providing	7D 🛛 8	17 🛛 7Q		
the capability of reading back the stored data onto	8D 🛛 9	16 🛛 8Q		
the input data bus.	9D 🛛 10	15 9Q		
	10D 🛛 11	14 0Q		
The ten latches are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs.	GND [12	13 LE		

Read back is provided through the output-enable (OERB) input. When OERB is taken low, the data present at the output of the data latches passes back onto the input data bus. When OERB is taken high, the output of the data latches is isolated from the D inputs. OERB does not affect the internal operation of the latches; however, precautions should be taken to avoid a bus conflict.

The SN74ALS994 is characterized for operation from 0°C to 70°C.

logic symbol[†]



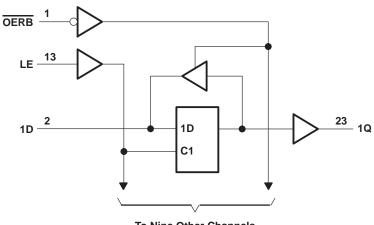
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



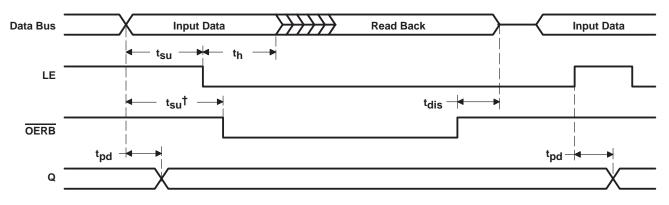
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logic diagram (positive logic)



To Nine Other Channels

timing diagram



[†] This setup time ensures that the read-back circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, V _{CC}	
Input voltage, VI (OERB and LE)	
Voltage applied to D inputs	5.5 V
Operating free-air temperature range, T _A	0°C to 70°C
Storage temperature range	65°C to 150°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



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recommended operating conditions

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage				5.5	V
VIH	High-level input voltage		2			V
VIL	Low-level input voltage				0.8	V
		Q			-2.6	
ЮН	High-level output current	D			-0.4	mA
		Q			24	
IOL	Low-level output current	D			8	mA
tw	Pulse duration, LE high					ns
	Outrue time	Data before LE \downarrow	10			
t _{su}	Setup time	Data before OERB↓†	10			ns
t _h	Hold time, data after LE \downarrow		5			ns
Тд	Operating free-air temperature		0		70	°C

[†] This setup time ensures that the read-back circuit will not create a conflict on the input data bus.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CON	MIN	TYP‡	MAX	UNIT	
VIK		$V_{CC} = 4.5 V,$	lj = – 18 mA			-1.2	V
	All outputs	$V_{CC} = 4.5 V$ to 5.5 V,	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2			
VOH	Q	$V_{CC} = 4.5 V,$	I _{OH} = – 2.6 mA	2.4	3.2		V
		D V _{CC} = 4.5 V	I _{OL} = 4 mA		0.25	0.4	V
	D		IOL = 8 mA		0.35	0.5	
VOL		N 45.V	I _{OL} = 12 mA		0.25	0.4	
	Q	V _{CC} = 4.5 V	I _{OL} = 24 mA		0.35	0.5	
	OERB, LE		V _I = 7 V			0.1	
II.	D inputs	V _{CC} = 5.5 V	V _I = 5.5 V			0.1	mA
	OERB, LE	N 55N				20	μΑ
ΙΗ	D inputs§	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20	
	OERB, LE	N 55N				-0.1	
۱L	D inputs§	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.1	mA
۱ ₀ ¶		V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	mA
Icc		V _{CC} = 5.5 V,	Q outputs high		30	50	
		OERB high	Q outputs low		52	82	mA

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C. § For I/O ports (Q_A thru Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



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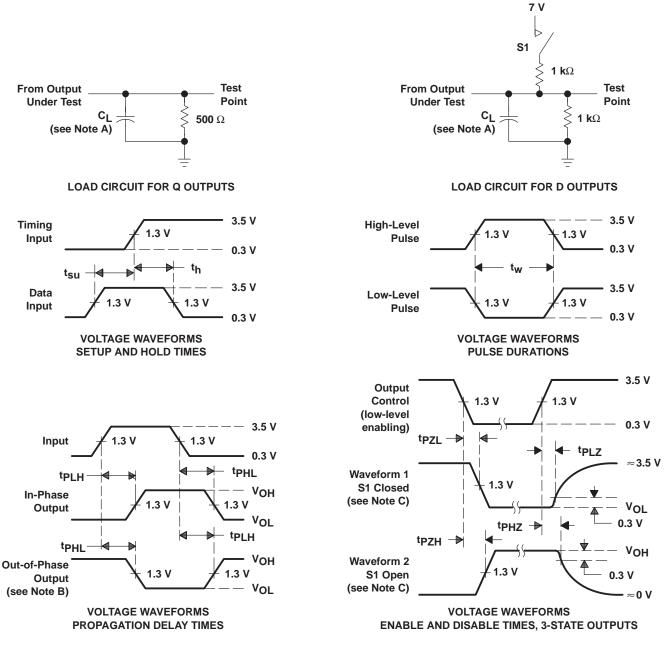
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 C _L = 50 pF T _A = MIN t	UNIT	
		, , ,	MIN	MAX	
^t PLH	5		3	14	
^t PHL	D	Q	4	18	ns
^t PLH			6	21	
^t PHL	LE	Q	8	27	ns
ten‡	OERB	D	4	21	
t _{dis} §	OERB	0	2	16	ns

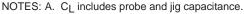
[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. [‡] t_{en} = t_{PZH} or t_{PZL} § t_{dis} = t_{PHZ} or t_{PLZ}



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PARAMETER MEASUREMENT INFORMATION



- B. When measuring propagation delay times of 3-state outputs, switch S1 is open.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. All input pulses have the following characteristics: PRR \leq 1 MHz, t_f = t_f = 2 ns, duty cycle = 50%.

Figure 1. Load Circuits and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74ALS994DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS994DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS994DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS994NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS994NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. **TBD**: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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NT (R-PDIP-T**) 24 pins shown

PLASTIC DUAL-IN-LINE PACKAGE



All integrations are in minimeters. Dimensioning and toil
 B. This drawing is subject to change without notice.

The 28 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AD.



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