

#### **General Description**

The MAX9650/MAX9651 are single- and dual-channel VCOM amplifiers with rail-to-rail inputs and outputs. The MAX9650/MAX9651 can drive up to 1300mA of peak current per channel and operate up to 20V.

The MAX9650/MAX9651 are designed to source and sink a high current quickly to hold the VCOM voltage stable in large TFT-LCD panels.

The MAX9650/MAX9651 feature 40V/µs slew rate and 35MHz bandwidth to guickly settle outputs for 120Hz frame rate and full HD television.

The MAX9650/MAX9651 feature output short-circuit protection and thermal shutdown. These devices are available in exposed pad packages for excellent heat dissipation.

**Applications** 

**TFT-LCD Panels** Instrument Control Voltage Sources

### **Features**

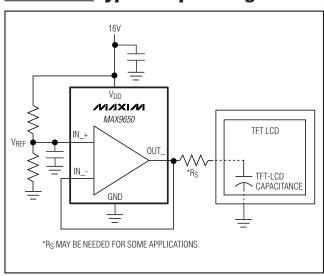
- ♦ 1300mA Peak Output Current
- ♦ Rail-to-Rail Inputs and Outputs
- ♦ Operates Up to 20V
- ♦ 40V/µs Slew Rate
- ♦ 35MHz Bandwidth
- **♦** 5mA Quiescent Current per Channel
- **♦** Excellent Heat Dissipation (Exposed Pad)

#### **Ordering Information**

PART	AMPS PER PACKAGE	PIN- PACKAGE	TOP MARK
MAX9650AZK+	1	5 SOT23	ADSI
MAX9650AZK/V+	1	5 SOT23	ADSK
MAX9650AUA+	1	8 μMAX-EP*	AABI
MAX9650ATA+	1	8 TDFN-EP*	BKX
MAX9651AUA+	2	8 μMAX-EP*	AABH
MAX9651ATA+	2	8 TDFN-EP*	BKY

Note: All devices are specified over the -40°C to +125°C operating range.

### **Typical Operating Circuit**



<sup>+</sup>Denotes a lead(Pb)-free/RoHS-compliant package.

<sup>/</sup>V denotes an automotive qualified part.

<sup>\*</sup>EP = Exposed pad.

#### **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage (VDD to GND)       -0.3V to +22V         Any Other Pin to GND       -0.3V to (VDD + 0.3V)         IN_+/IN (current)       ±20mA	O <sub>l</sub> Ju St
OUT_ (current)	Le
Continuous Power Dissipation ( $T_A = +70^{\circ}C$ )	Sc
5-Pin SOT23 (derate 3.7mW/°C above +70°C)297.4mW	
8-Pin µMAX-EP (derate 12.9mW/°C	
above +70°C)1030.9mW	
8-Pin TDFN-EP (derate 23.8mW/°C	
above +70°C)1951.2mW	

	Operating Temperature Range	40°C to +125°C
,	Junction Temperature	+150°C
	Storage Temperature Range	65°C to +150°C
	Lead Temperature (soldering, 10s).	+300°C
	Soldering Temperature (reflow)	+260°C
	• ' '	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS**

(VDD = 19V, VGND = 0V, VCM = VOUT = VDD/2, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIO	NS	MIN	TYP	MAX	UNITS
Supply Voltage Range	$V_{DD}$	Guaranteed by PSRR	Guaranteed by PSRR			20	V
Quiescent Current	I <sub>DD</sub>	Per channel			3.7	8	mA
High Output Voltage	Voн	$I_H = +5mA$ , $V_{IN} = V_{DD}$		V <sub>DD</sub> - 0.30	V <sub>DD</sub> - 0.05		V
Low Output Voltage	V <sub>OL</sub>	$I_L = -5mA$ , $V_{IN} = 0V$			0.05	0.30	V
la and Offers Veltage	1/	T <sub>A</sub> = +25°C		-14	3.5	+14	\/
Input Offset Voltage	Vos	$T_A = -40^{\circ}\text{C to } + 125^{\circ}\text{C}$		-17		+17	mV
Load Deculation	I D	I <sub>OUT</sub> = 0mA to -80mA			+0.2		να\ / /να Λ
Load Regulation	LR	I <sub>OUT</sub> = 0mA to +80mA			-0.2		mV/mA
Input Bias Current	I <sub>FB</sub>	At $V_{IN} = 9.5V$			0.01	1	μΑ
Voltage Gain	Ay	$R_L = 10k\Omega$ , $C_L = 50pF$		0.99		1.01	V/V
Power-Supply Rejection Ratio	PSRR	$V_{DD} = 6V$ to 20V, $V_{CM} = V_{OUT} = 3V$		70	95		dB
Common-Mode Input Voltage Range	CMVR	Inferred from CMRR test		0.5		V <sub>DD</sub> - 0.5	V
Common-Mode Rejection Ratio	CMRR	$0.5V \le V_{CM} \le V_{DD} - 0.5V$		60	80		dB
		V <sub>OUT</sub> = 9.5V	MAX9650AZK+	20			
Continuous Output Current	Io	(Note 2)	MAX9650AUA+	80			mA
		V <sub>DD</sub> = 15V, V <sub>OUT</sub> = 7.5V	MAX9650ATA+		±350		
Transient Peak Output Current	IPK	(Note 3)			±1.3		А
Bandwidth	BW	-3dB			35		MHz
Slew Rate	SR	4V step, $C_L = 50pF$ , $R_L = 10k\Omega$ , $A_V = +1V/V$			40		V/µs
Settling Time	ts	Settling to 0.1% of V <sub>OUT</sub> , I <sub>L</sub> R <sub>S</sub> = $2.2\Omega$ , C <sub>S</sub> = $0.1\mu$ F (Fig			2.0		μs

#### **ELECTRICAL CHARACTERISTICS (continued)**

(V<sub>DD</sub> = 19V, V<sub>GND</sub> = 0V, V<sub>CM</sub> = V<sub>OUT</sub> = V<sub>DD</sub>/2, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Load Capacitance	CLOAD	(Note 4)		150		nF
Noninverting Input Resistance	R <sub>IN+</sub>	(Note 5)		100		МΩ
Inverting Input Resistance	R <sub>IN</sub> -	(Note 5)		100		МΩ
Input Capacitance	CIN			3		рF
Thermal Shutdown				+170		°C
Thermal Shutdown Hysteresis				15		°C

Note 1: All devices are 100% production tested at  $T_A = +25$ °C. All temperature limits are guaranteed by design.

Note 2: Continuous output current is tested with one output at a time.

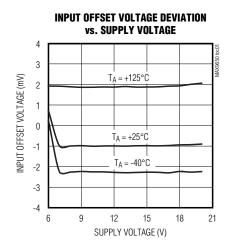
Note 3: See the Thermal Shutdown with Temperature Hysteresis section.

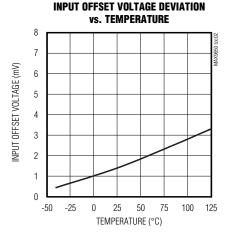
**Note 4:** A series resistor can extend load capacitance range. The settling time can be optimized by a small series resistance. See the *Applications Information* section for more information.

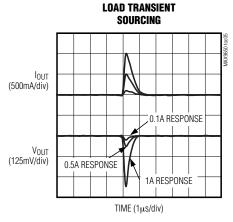
Note 5: Inputs are protected by back-to-back diodes.

#### \_Typical Operating Characteristics

 $(V_{DD} = 19V, GND = 0, V_{CM} = V_{OUT} = V_{DD}/2, T_A = +25^{\circ}C, unless otherwise specified.)$ 

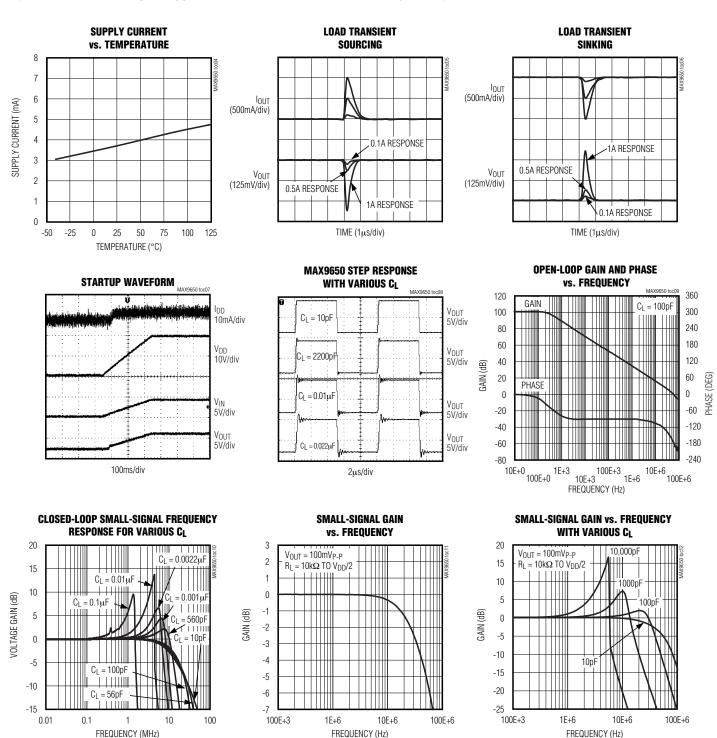






### Typical Operating Characteristics (continued)

 $(V_{DD} = 19V, GND = 0, V_{CM} = V_{OUT} = V_{DD}/2, T_A = +25^{\circ}C, unless otherwise specified.)$ 



#### **Pin Description**

	PIN				
MA	X9650	MAX9651	NAME	FUNCTION	
SOT23	μΜΑΧ-ΕΡ, TDFN-ΕΡ	(µMAX-EP, TDFN-EP)	IVANL	TONOTION	
1	6	1	OUTA	VCOM Output A	
2	4	4	GND	Ground	
3	3	3	INA+	Positive Input A	
4	2	2	INA-	Negative Input A	
5	7	8	V <sub>DD</sub>	Positive-Supply Input. Bypass V <sub>DD</sub> to GND with a 0.1µF capacitor as close as possible to the device.	
_	_	5	INB+	Positive Input B	
_	_	6	INB-	Negative Input B	
_	_	7	OUTB	VCOM Output B	
_	1, 5, 8	_	N.C.	No Connection. Not internally connected.	
_	_	_	EP	Exposed Pad ( $\mu$ MAX and TDFN Only). EP is internally connected to GND. Connect EP to GND.	

#### **Detailed Description**

The MAX9650/MAX9651 operational rail-to-rail input/output amplifiers hold the VCOM voltage stable while providing the ability to source and sink a high current quickly (1.3A) into a capacitive load such as the backplane of a TFT-LCD panel.

### Thermal Shutdown with Temperature Hysteresis

The MAX9650/MAX9651 are capable of high output currents and feature thermal-shutdown protection with temperature hysteresis. When the die temperature reaches +170°C, the device shuts down. When the die cools down by 15°C, the device turns on again. In a TFT-LCD application, the duty cycle is very low. Even with high values of voltage and current, the power dissipation is low and the chip does not shut down.

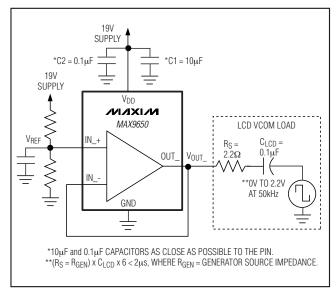


Figure 1. Settling Time Test Circuit

#### **Applications Information**

#### **Output Load**

The MAX9650/MAX9651 are designed to drive capacitive loads. A small value of series resistance improves the performance of the device to ensure stability and fast settling with very large or very small capacitive loads. In many cases, this resistance is already present due to connection resistance in the wiring and no additional physical resistor is necessary. For minimum series resistance required for stability with capacitive loading, see Figure 2.

#### **Power Supplies and Bypass Capacitors**

The MAX9650/MAX9651 operate from a 6V to 20V single supply or from ±4.5V to ±10V dual supplies. Proper supply bypassing ensures stability while driving high

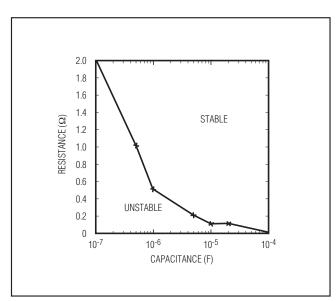


Figure 2. Minimum Combined ESR/Series/Trace Resistance Required for Stability of the MAX9650 in Response to Capacitive Loads

transient loads. The MAX9650/MAX9651 require a minimum  $10\mu\text{F}$  (C1) and  $0.1\mu\text{F}$  (C2) power-supply bypass capacitors placed as close as possible to the power-supply pin (V<sub>DD</sub>). See Figure 3. For dual-supply operation, use  $10\mu\text{F}$  and  $0.1\mu\text{F}$  bypass capacitors on both supplies (V<sub>DD</sub> and GND) with each capacitor placed as close as possible to V<sub>DD</sub> and GND.

#### **Layout and Grounding**

The exposed pad on the  $\mu$ MAX® and TDFN packages provide a low thermal resistance for heat dissipation. Solder the exposed pad to a ground plane for best thermal performance. Do not route traces under these packages. For dual-supply operation, the exposed pad (EP) can be electrically connected to the negative supply or it can be left unconnected.

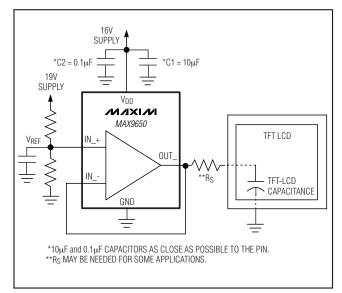


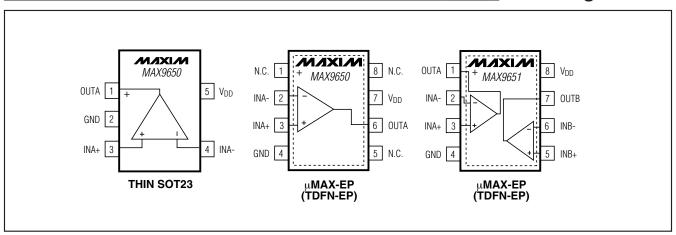
Figure 3. Typical TFT-LCD Backplane Drive Circuit

Chip Information

PROCESS: BICMOS

μΜΑΧ is a registered trademark of Maxim Integrated Products, Inc.

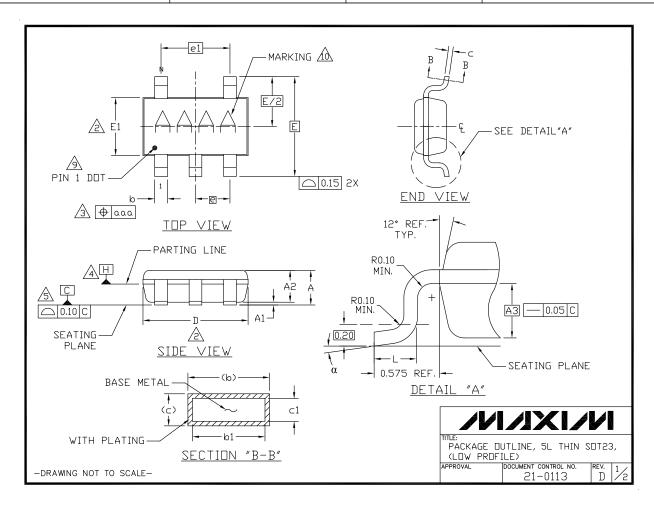
### Pin Configurations



#### **Package Information**

For the latest package outline information and land patterns, go to <a href="www.maxim-ic.com/packages">www.maxim-ic.com/packages</a>. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
5 SOT23	Z5+2	<u>21-0113</u>	<u>90-0241</u>
8 μMAX	U8E+2	<u>21-0107</u>	<u>90-0145</u>
8 TDFN-EP	T833+2	21-0137	<u>90-0058</u>



#### Package Information (continued)

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#### NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.

'D' AND 'E1' ARE REFERENCE DATUM AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE BOTTOM PARTING LINE. MOLD FLASH OPPOTRUSION SHALL NOT EXCEED 0.15mm ON 'D' AND 0.25mm ON 'E' PER SIDE.

3. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.07mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.

DATUM PLANE EH LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT THE BOTTOM OF PARTING LINE.

THE LEAD TIPS MUST LINE WITHIN A SPECIFIED TOLERANCE ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL LINES. DNE PLANE IS THE SEATING PLANE, DATUM EC-J AND THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM EC-J IN THE DIRECTION INDICATED. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO DNE ANOTHER WITH 0.10mm AT SEATING PLANE.

- 6. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-193 EXCEPT FOR THE 'e' DIMENSION WHICH IS 0.95mm INSTEAD OF 1.00mm. THIS PART IS IN FULL COMPLIANCE TO EIAJ SPECIFICATION SC-74.
- 7. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
- 8. WARPAGE SHALL NOT EXCEED 0.10mm.

THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 PP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE

10. MARKING IS FOR PACKAGE DRIENTATION REFERENCE ONLY.

- 11. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
- 12. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

	DIMENSIONS					
	MIN	NDM	MAX			
Α	ı	-	1.10			
A1	0.00	0.075	0.10			
A2	0.85	0.88	0.90			
A3		0.50 BSC				
b	0.30	-	0.45			
b1	0.25	0.35	0.40			
C	0.15	-	0.20			
⊂1	0.12	0.127	0.15			
D	2.80	2.90	3.00			
Ε		2.75 BSC				
E1	1.55	1.60	1.65			
L	0.30	0.40	0.50			
e1		1.90 BSC				
е	0.95 BSC					
α	0*	4°	8*			
aaa	0.20					
PKG CDDE	Z5-1, Z5-2, Z5-3					

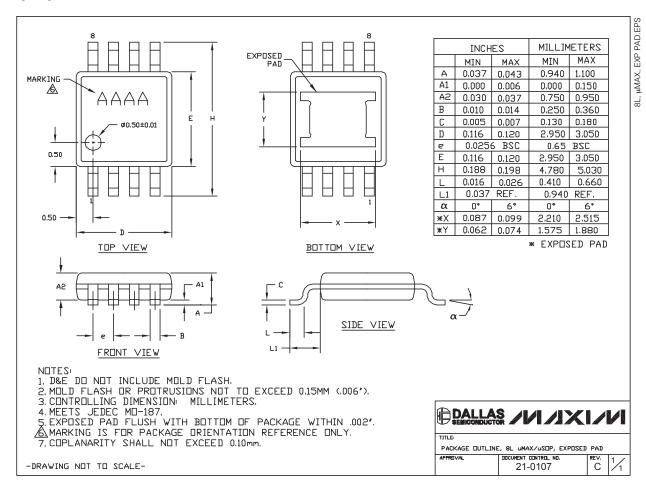
TITLE:
PACKAGE DUTLINE, 5L THIN SDT23,
(LDW PROFILE)

pocument control no. Rev. 21–0113 D 2

-DRAWING NOT TO SCALE-

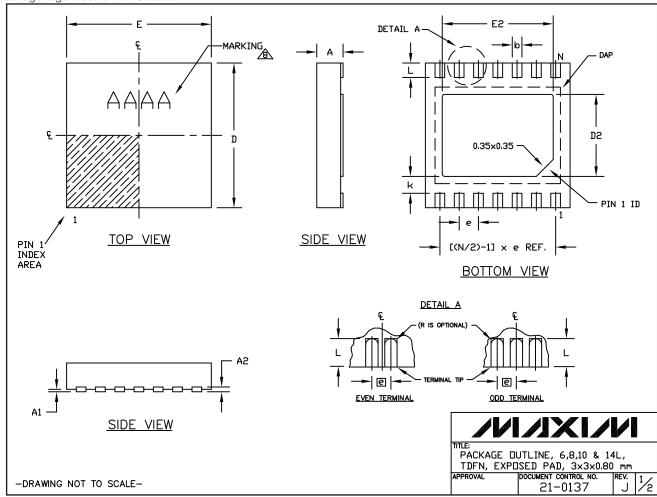
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COMMON DIMENSIONS						
SYMBOL	MIN.	MAX.				
Α	0.70	0.80				
D	2.90	3.10				
E	2.90	3.10				
A1	0.00	0.05				
١	0.20	0.40				
k 0.25 MIN.						
A2 0.20 REF.						

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	е	JEDEC SPEC	b	[(N/2)-1] x e
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033MK-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC		0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC		0.20±0.05	2.40 REF
T1433-3F	14	1.70±0.10	2.30±0.10	0.40 BSC		0.20±0.05	2.40 REF

-DRAWING NOT TO SCALE-

- 1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
- 2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
- 3. WARPAGE SHALL NOT EXCEED 0.10 mm.
- 4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
- 5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
- "N" IS THE TOTAL NUMBER OF LEADS.
- 7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
- MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
- 9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PHFREE (+) PKG. CODES.

PACKAGE DUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

PROVAL | DOCUMENT CONTROL NO. | REV.

21-0137

MIXIM

### \_Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/08	Initial release	_
1	10/08	Updated slew rate and added TDFN-EP package	1, 2, 6, 10, 11
2	5/09	Updated continuous output current specification	2
3	2/10	Added automotive part to <i>Ordering Information</i> , corrected units for input offset voltage, and added figure for minimum series resistance	1, 2, 5, 6
4	7/10	Removed extraneous information in the <i>Electrical Characteristics</i> table and corrected typo in TOC 5	2, 4

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