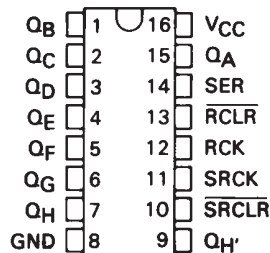


# SN54LS594, SN54LS599, SN74LS594, SN74LS599 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

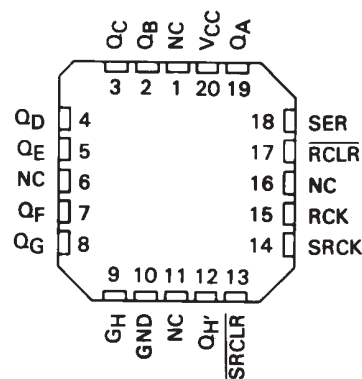
SDLS005 – D2747, JUNE 1983 – REVISED MARCH 1988

- **8-Bit Serial-In, Parallel-Out Shift Registers with Storage**
- **Choice of Output Configurations:**  
'LS594 ... Buffered  
'LS599 ... Open-Collector
- **Guaranteed Shift Frequency:**  
DC to 20 MHz
- **Independent Direct-Overriding Clears on Shift and Storage Registers**
- **Independent Clocks for Both Shift and Storage Registers**

SN54LS594, SN54LS599 . . . J OR W PACKAGE  
SN74LS594, SN74LS599 . . . N PACKAGE  
(TOP VIEW)



SN54LS594, SN54LS599 . . . FK PACKAGE  
(TOP VIEW)



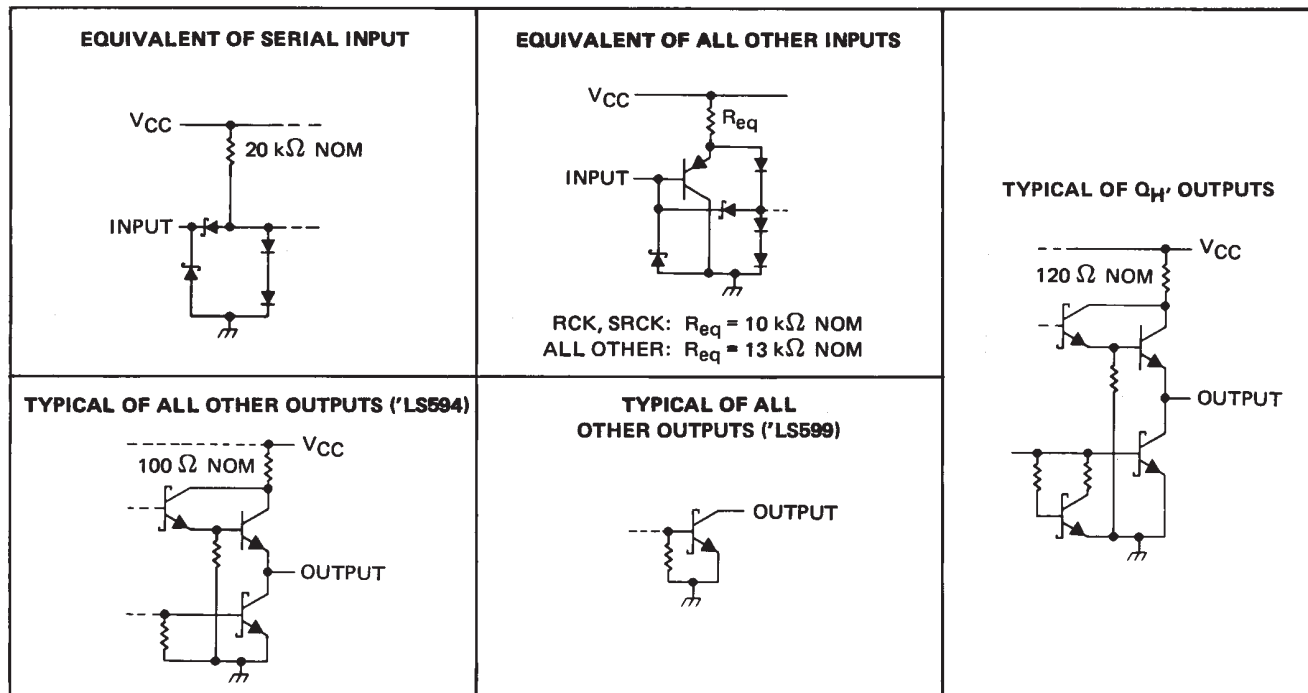
## description

These devices each contain an 8-bit D-type storage register. The storage register has buffered ('LS594) or open-collector ('LS599) outputs. Separate clocks and direct-overriding clears are provided on both the shift and storage registers. A shift output (Q<sub>H</sub>') is provided for cascading purposes.

Both the shift register and the storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register will always be one clock pulse ahead of the storage register.

NC — No internal connection

## schematics of inputs and outputs



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# SN54LS594, SN54LS599, SN74LS594, SN74LS599 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS'		SN74LS'		UNIT			
		MIN	TYP‡	MAX	MIN		TYP‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5		V			
V <sub>OH</sub>	'LS594 Q Q <sub>H</sub> '	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX	I <sub>OH</sub> = -1 mA		2.4 3.2		V		
			I <sub>OH</sub> = -2.6 mA		2.4 3.1				
			I <sub>OH</sub> = -1 mA		2.4 3.2				
I <sub>OH</sub>	'LS599 Q	V <sub>CC</sub> = MIN, V <sub>OH</sub> = 5.5 V	V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX,	0.1		0.1	mA		
V <sub>OL</sub>	Q Q <sub>H</sub> '	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX	V <sub>IH</sub> = 2 V,	I <sub>OL</sub> = 12 mA		0.25 0.4		V	
				I <sub>OL</sub> = 24 mA		0.35 0.5			
				I <sub>OL</sub> = 8 mA		0.25 0.4			
				I <sub>OL</sub> = 16 mA		0.35 0.5			
I <sub>I</sub>		V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V			0.1		0.1	mA	
I <sub>IH</sub>		V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20		20	μA	
I <sub>IL</sub>	SER	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.4		-0.4		mA
	All others				-0.2		-0.2		
I <sub>OS</sub> §	'LS594 Q	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0			-30 -130		-30 -130		mA
	Q <sub>H</sub> '				-20 -100		-20 -100		
I <sub>CCH</sub>	'LS594	V <sub>CC</sub> = MAX, All possible inputs grounded,			34 50		34 50		mA
	'LS599				30 45		30 45		
I <sub>CCL</sub>	'LS594	All outputs open			42 65		42 65		mA
	'LS599				38 55		38 55		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C, (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS594			'LS599			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PLH</sub>	SRCK↑	Q <sub>H</sub> '	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 30 pF	12 18			12 18			ns
t <sub>PHL</sub>				15 23			17 25			
t <sub>PLH</sub>	RCK↑	Q <sub>A</sub> thru Q <sub>H</sub>	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 45 pF	12 18			28 42			ns
t <sub>PHL</sub>				20 30			24 35			
t <sub>PHL</sub>	SRCLR↓	Q <sub>H</sub> '	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 30 pF	22 33			24 35			ns
t <sub>PHL</sub>	RCLR↓	Q <sub>A</sub> thru Q <sub>H</sub>	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 45 pF	38 57			40 60			ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

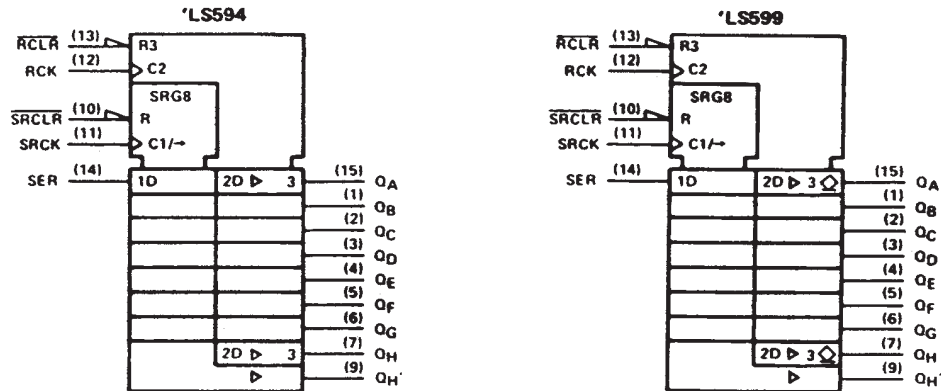


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# SN54LS594, SN54LS599, SN74LS594, SN74LS599 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

SDLS005 – D2747, JUNE 1983 – REVISED MARCH 1988

## logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for J, N, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage .....	7 V
Off-state output voltage .....	5.5 V
Operating free-air temperature range: SN54LS594, SN54LS599 .....	$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$
SN74LS594, SN74LS599 .....	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$
Storage temperature range .....	$-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$

NOTE 1: Voltage values are with respect to the network ground terminal.

## recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$V_{OH}$	High-level output voltage			5.5			5.5	V
$I_{OH}$	High-level output current	$Q_A$ thru $Q_H$ , 'LS599 only						mA
		$Q_H'$			-1		-1	
$I_{OL}$	Low-level output current	$Q_A$ thru $Q_H$ , 'LS594 only						mA
		$Q_H'$			-1		-2.6	
$I_{OL}$	Low-level output current	$Q$			8		16	mA
					12		24	
$f_{SRCK}$	Shift clock frequency	0		20	0		20	MHz
$f_{RCK}$	Register clock frequency	0		25	0		25	MHz
$t_w(SRCK)$	Duration of shift clock pulse	25			25			ns
$t_w(RCK)$	Duration of register clock pulse	20			20			ns
$t_w(SRCLR)$	Duration of shift clear pulse, low level	20			20			ns
$t_w(RCLR)$	Duration of register clear pulse, low level	35			35			ns
$t_{su}$	Setup time	SRCLR inactive before SRCK↑		20		20		ns
		SER before SRCK↑		20		20		
		SRCK↑ before RCK↑ (see Note 2)		40		40		
		SRCLR low before RCK↑		40		40		
		RCLR high before RCK↑		20		20		
$t_h$	Hold time	SER after SRCK↑		0		0		ns
$T_A$	Operating free-air temperature	-55		125	0		70	$^{\circ}\text{C}$

NOTE 2: This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together, in which case the storage register state will be one clock pulse behind the shift register.

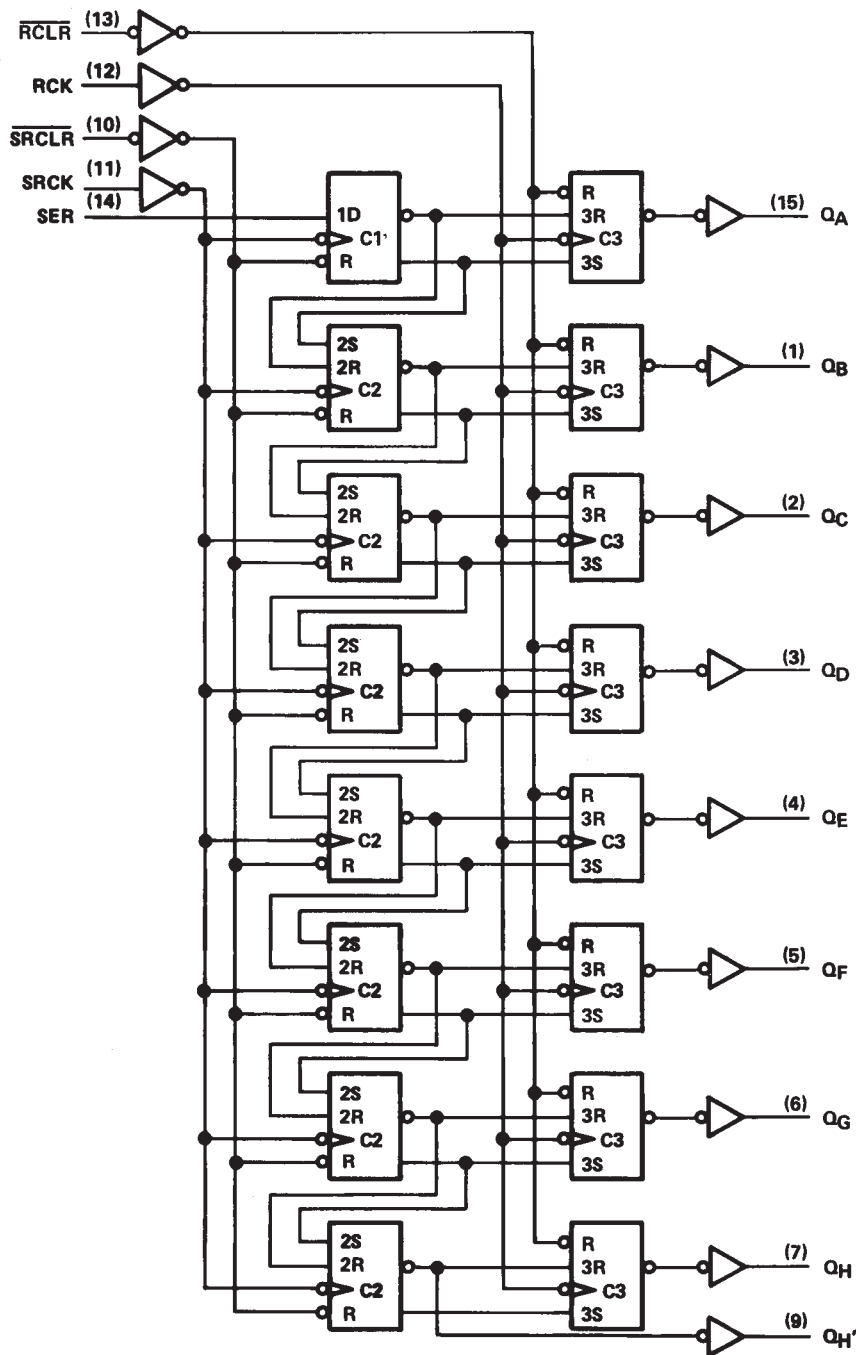


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# SN54LS594, SN54LS599, SN74LS594, SN74LS599 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

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## logic diagram (positive logic)



Pin numbers shown are for J, N, and W packages.



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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS594NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS594NSR	SO	NS	16	2000	346.0	346.0	33.0

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