SN54ACT563 ... J OR W PACKAGE SN74ACT563 ... DB, DW, N, NS, OR PW PACKAGE

(TOP VIEW)

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- 4.5-V to 5.5-V V<sub>CC</sub> Operation
- Inputs Accept Voltages to 5.5 V
- Max t<sub>pd</sub> of 8.5 ns at 5 V
- Inputs Are TTL-Voltage Compatible
- 3-State Inverted Outputs Drive Bus Lines Directly
- Flow-Through Architecture to Optimize PCB Layout

## description/ordering information

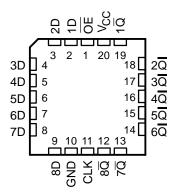
The 'ACT563 devices are octal D-type transparent latches with 3-state outputs. When the latch-enable (LE) input is high, the  $\overline{Q}$  outputs are set to the complements of the data (D) inputs. When LE is taken low, the  $\overline{Q}$  outputs are latched at the inverse logic levels set up at the D inputs.

A buffered output-enable  $(\overline{OE})$  input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high logic level provide the capability to drive bus lines without interface or pullup components.

OE does not affect internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

	•		
OE		$\cup_{20}$	v <sub>cc</sub>
1D	2	19	] 1Q
2D	[] З	18	] 2Q
3D	4	17	] 3Q
4D	5	16	4Q
5D	6	15	] 5Q
6D	7	14	] 6 <mark>Q</mark>
7D	8 ]	13	] 7Q
8D	9	12	8Q
GND	[ 10	11	LE
	-		•

SN54ACT563 . . . FK PACKAGE (TOP VIEW)



To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ТА	PACKAGE	Et.	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube	SN74ACT563N	SN74ACT563N
	SOIC - DW	Tube	SN74ACT563DW	ACT563
–40°C to 85°C	50IC - DW	Tape and reel	SN74ACT563DWR	AC1503
-40°C to 85°C	SOP – NS	Tape and reel	SN74ACT563NSR	ACT563
	SSOP – DB	Tape and reel	SN74ACT563DBR	AD563
	TSSOP – PW	Tape and reel	SN74ACT563PWR	AD563
	CDIP – J	Tube	SNJ54ACT5634J	SNJ54ACT563J
–55°C to 125°C	CFP – W	Tube	SNJ54ACT563W	SNJ54ACT563W
	LCCC – FK	Tube	SNJ54ACT563FK	SNJ54ACT563FK

#### ORDERING INFORMATION

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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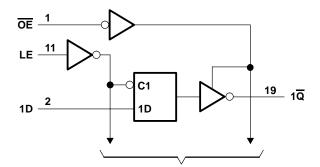


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	FUNCTION TABLE (each latch)										
	INPUTS	OUTPUT									
OE	LE	D	Q								
L	Н	Н	L								
L	н	L	н								
L	L	Х	$\overline{Q}_0$								
Н	Х	Х	Z								

## logic diagram (positive logic)



**To Seven Other Channels** 

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Input voltage range, $V_I$ (see Note 1) Output voltage range, $V_O$ (see Note 1) Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) Continuous current through $V_{CC}$ or GND	-0 -0.5 V to V -0.5 V to V -0.5 V to V DB package DW package N package NS package PW package	CC + 0.5 V CC + 0.5 V ±20 mA ±20 mA ±50 mA ±200 mA 70°C/W 58°C/W 69°C/W 60°C/W
Storage temperature range, T <sub>stg</sub>	PW package65°0	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



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#### recommended operating conditions (see Note 3)

		SN54A	CT563	SN74A	CT563	
		4.5 5.5 4.5   2 2 2   0.8 0 VCC 0   0 VCC 0 V	MAX	UNIT		
VCC	Supply voltage	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2	2	2		V
VIL	Low-level input voltage		0.8		0.8	V
VI	Input voltage	0	Vcc	0	VCC	V
Vo	Output voltage	0,	Vcc	0	VCC	V
ЮН	High-level output current	D D	-24		-24	mA
IOL	Low-level output current	20	24		24	mA
$\Delta t / \Delta v$	Input transition rise or fall rate	2	8		8	ns/V
TA	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		T	A = 25°C	;	SN54A	CT563	SN74A	CT563	UNIT
PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
	1 50 HA	4.5 V	4.4	4.49		4.4		4.4		
	I <sub>OH</sub> = -50 μA	5.5 V	5.4	5.49		5.4		5.4		
Vou	1011 - 24 mA	4.5 V	3.86			3.7		3.76		V
Vон	I <sub>OH</sub> = -24 mA	5.5 V	4.86			4.7		4.76		v
	I <sub>OH</sub> = -50 mA <sup>†</sup>	5.5 V				3.85	2			
	$I_{OH} = -75 \text{ mA}^{\dagger}$	5.5 V					VIE	3.85		
	le 50 uA	4.5 V		0.001	0.1		0.1		0.1	V
	I <sub>OL</sub> = 50 μA	5.5 V		0.001	0.1	~	0.1		0.1	
Ve	a  = 24  mA	4.5 V			0.36	UC D	0.5		0.44	
VOL	I <sub>OL</sub> = 24 mA	5.5 V			0.36	70	0.5		0.44	v
	I <sub>OL</sub> = 50 mA <sup>†</sup>	5.5 V				54	1.65			
	I <sub>OL</sub> = 75 mA <sup>†</sup>	5.5 V							1.65	
I <sub>OZ</sub>	$V_{O} = V_{CC}$ or GND	5.5 V			±0.25		±5		±2.5	μA
lj	$V_{I} = V_{CC} \text{ or } GND$	5.5 V			±0.1		±1		±1	μA
ICC	$V_{I} = V_{CC} \text{ or GND}, \qquad I_{O} = 0$	5.5 V			4		80		40	μA
$\Delta I_{CC}^{\ddagger}$	One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V		0.6			1.6		1.5	mA
Ci	$V_{I} = V_{CC} \text{ or } GND$	5 V		4.5						pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

<sup>‡</sup>This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

# timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

		T <sub>A</sub> = 25°C		SN54ACT563	SN74ACT563		UNIT	
		MIN	MAX		MIN MAX MIN MAX			
tw	Pulse duration, LE high	3		5	3		ns	
t <sub>su</sub>	Setup time, data before LE $\downarrow$	4		4.5	4.5		ns	
t <sub>h</sub>	Hold time, data after LE $\downarrow$	0		1.5	0		ns	

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# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	T <sub>A</sub> = 25°C			SN54ACT563		SN74ACT563		UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<sup>t</sup> PLH	D		3	7	11.5	1	14.5	2.5	12.5	ns
<sup>t</sup> PHL	D	<u>a</u>	3	6	10	1	12	2.5	11	115
<sup>t</sup> PLH	LE	Q	3	6.5	10.5	1	12.5	2.5	11.5	20
<sup>t</sup> PHL	LL	ġ	2.5	5.5	9.5	1	<b>Q</b> 11.5	2	10.5	ns
<sup>t</sup> PZH	OE	-	2.5	5.5	9	Q.	11.5	2	10	
<sup>t</sup> PZL	ÛE	Q	2	5.5	8.5	$\overline{\Delta}_{0}$	11	2	9.5	ns
<sup>t</sup> PHZ	ŌĒ	Q	3.5	6.5	10.5	<b>a</b> 1	12	2.5	11.5	200
<sup>t</sup> PLZ	UE	y y	2	4.5	8	1	9.5	1	8.5	ns

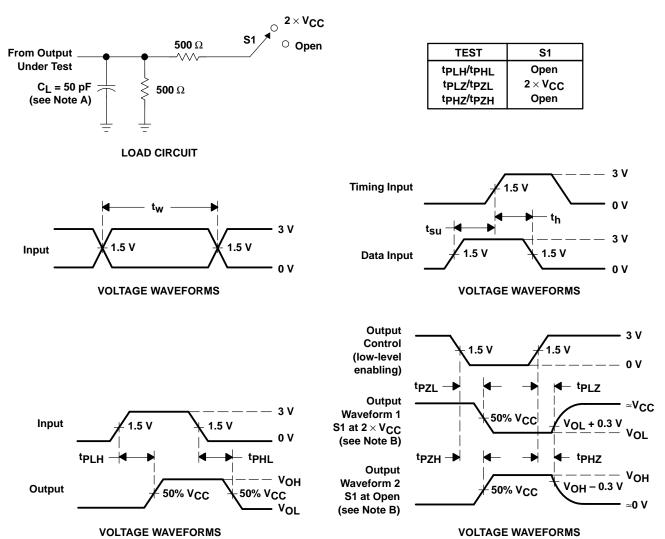
# operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	$C_L = 50 \text{ pF},  f = 1 \text{ MHz}$	50	pF

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#### PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

- Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one input transition per measurement.

#### Figure 1. Load Circuit and Voltage Waveforms





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#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74ACT563DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	
SN74ACT563DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ACT563DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ACT563DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ACT563DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU Level-1-260C-UNLIM		
SN74ACT563DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ACT563N	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ACT563NE4	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ACT563PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ACT563PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ACT563PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ACT563PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	
SN74ACT563PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ACT563PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ACT563PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

# PACKAGE OPTION ADDENDUM



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<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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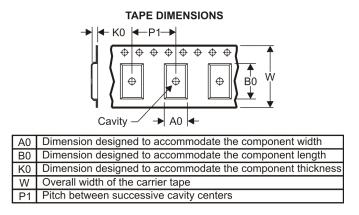
# PACKAGE MATERIALS INFORMATION

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## TAPE AND REEL INFORMATION





## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT563DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74ACT563PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

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# PACKAGE MATERIALS INFORMATION

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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT563DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74ACT563PWR	TSSOP	PW	20	2000	346.0	346.0	33.0

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