Data Sheet

CADEKA
Amplify the Human Experience

Comlinear® CLC2005

Dual, Low Cost, +2.7V to 5.5V, 260MHz Rail-to-Rail Amplifier

FEATURES

- 260MHz bandwidth
- Fully specified at +2.7V and +5V supplies
- Output voltage range: 0.036V to 4.953V; V_S = +5; R_L = 2kΩ
- Input voltage range: -0.3V to +3.8V; V_S = +5
- 145V/µs slew rate
- 4.2mA supply current per amplifier
- ±55mA linear output current
- ±85mA short circuit current
- Directly replaces AD8052 and AD8042 in single supply applications
- Pb-free SOIC-8 package

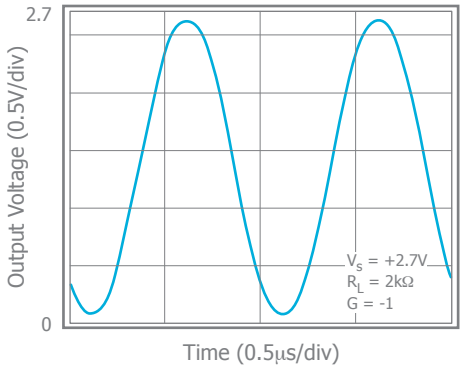
APPLICATIONS

- A/D driver
- Active filters
- CCD imaging systems
- CD/DVD ROM
- Coaxial cable drivers
- High capacitive load driver
- Portable/battery-powered applications
- Twisted pair driver
- Video driver

General Description

The *Comlinear* CLC2005 is a dual, low cost, voltage feedback amplifier. This amplifier is designed to operate on +2.7V,+5V, or ±2.5V supplies. The input voltage range extends 300mV below the negative rail and 1.2V below the positive rail. The CLC2005 offers superior dynamic performance with a 260MHz small signal bandwidth and 145V/µs slew rate. The combination of low power, high output current drive, and rail-to-rail performance make the *Comlinear* CLC2005 well suited for battery-powered communication/computing systems. The combination of low cost and high performance make the *Comlinear* CLC2005 suitable for high volume applications in both consumer and industrial applications such as wireless phones, scanners, and color copiers.

Output Swing



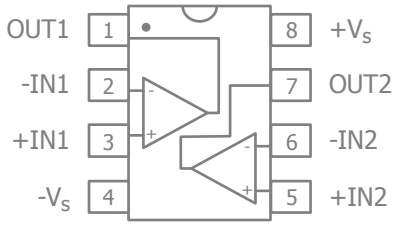
Ordering Information

Part Number	Package	Pb-Free	Operating Temperature Range	Packaging Method
CLC2005ISO8	SOIC-8	Yes	-40°C to +85°C	Rail
CLC2005ISO8X	SOIC-8	Yes	-40°C to +85°C	Reel

Moisture sensitivity level for all parts is MSL-1.

Pin Configuration

SOIC-8



Pin Assignments

SOIC-8

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$-V_S$	Negative supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	$+V_S$	Positive supply

Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage	0	+6	V
Input Voltage Range	$-V_S$ -0.5V	$+V_S$ +0.5V	V

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			175	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			260	°C
Package Thermal Resistance				
8-Lead SOIC		100		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

ESD Protection

Product	SOIC-8
Human Body Model (HBM)	2.5kV
Charged Device Model (CDM)	2kV

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C

Electrical Characteristics

V_S = +2.7V, G = 2, R_f = 2kΩ, R_L = 2kΩ to V_S/2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth(2)	G = +1, V_{OUT} = 0.05V_{pp}		215		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		85		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 2V_{pp}		36		MHz
GBWP	Gain Bandwidth Product			86		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time(2)	V_{OUT} = 0.2V step		3.7		ns
t_S	Settling Time to 0.1%	V_{OUT} = 1V step		40		ns
OS	Overshoot	V_{OUT} = 0.2V step		9		%
SR	Slew Rate	2.7V step, G = -1		130		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion(2)	1V_{pp}, 5MHz		79		dBc
HD3	3rd Harmonic Distortion(2)	1V_{pp}, 5MHz		82		dBc
		1V_{pp}, 5MHz		77		dB
e_n	Input Voltage Noise	> 1MHz		16		nV/√Hz
i_n	Input Current Noise	> 1MHz		1.3		pA/√Hz
X_{TALK}	Crosstalk(1)	10MHz		65		dB
DC Performance						
V_{IO}	Input Offset Voltage			-1.6		mV
dV_{IO}	Average Drift			10		µV/°C
I_b	Input Bias Current			3		µA
dI_b	Average Drift			7		nA/°C
I_{IO}	Input Offset Current			0.1		µA
PSRR	Power Supply Rejection Ratio(1)	DC	52	57		dB
A_{OL}	Open-Loop Gain			75		dB
I_S	Quiescent Current	Per Amplifier		3.9		mA
Input Characteristics						
R_{IN}	Input Resistance			4.3		MΩ
C_{IN}	Input Capacitance			1.8		pF
CMIR	Common Mode Input Range			-0.3 to 1.5		V
CMRR	Common Mode Rejection Ratio	DC, V_{cm} = 0V to V_s -1.5		87		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 10kΩ to V_s/2		0.023 to 2.66		V
		R_L = 2kΩ to V_s/2		0.025 to 2.653		V
		R_L = 150Ω to V_s/2		0.065 to 2.55		V
I_{OUT}	Output Current			±55		mA
		-40°C to +85°C		±50		mA
I_{SC}	Short-Circuit Output Current			±85		mA
V_s	Power Supply Operating Range		2.5	2.7	5.5	V

Notes:

1. 100% tested at 25°C.
2. R_f = 1kΩ was used for optimal performance. (For G = +1, R_f = 0).

Electrical Characteristics

V_S = 5V, G = 2, R_f = 2kΩ, R_L = 2kΩ to V_S/2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth(2)	G = +1, V_{OUT} = 0.05V_{pp}		260		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		90		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 2V_{pp}		40		MHz
GBWP	Gain Bandwidth Product			90		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time(2)	V_{OUT} = 0.2V step		3.6		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		40		ns
OS	Overshoot	V_{OUT} = 0.2V step		7		%
SR	Slew Rate	5V step, G = -1		145		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion(2)	2V_{pp}, 5MHz		71		dBc
HD3	3rd Harmonic Distortion(2)	2V_{pp}, 5MHz		78		dBc
		2V_{pp}, 5MHz		70		dB
DG	Differential Gain	NTSC (3.85MHz), AC-Coupled, R_L = 150Ω		0.06		%
		NTSC (3.85MHz), DC-Coupled, R_L = 150Ω		0.08		%
DP	Differential Phase	NTSC (3.85MHz), AC-Coupled, R_L = 150Ω		0.07		°
		NTSC (3.85MHz), DC-Coupled, R_L = 150Ω		0.06		°
e_n	Input Voltage Noise	>1MHz		16		nV/√Hz
i_n	Input Current Noise	>1MHz		1.3		pA/√Hz
X_{TALK}	Crosstalk(2)	10MHz		62		dB
DC Performance						
V_{IO}	Input Offset Voltage(1)		-8	1.4	+8	mV
dV_{IO}	Average Drift			10		µV/°C
I_b	Input Bias Current(1)		-8	3	+8	µA
dI_b	Average Drift			7		nA/°C
I_{IO}	Input Offset Current(1)		-0.8	0.1	+0.8	µA
PSRR	Power Supply Rejection Ratio(1)	DC	52	57		dB
A_{OL}	Open-Loop Gain(1)		68	78		dB
I_S	Quiescent Current(1)	Per Amplifier		4.2	5.2	mA
Input Characteristics						
R_{IN}	Input Resistance			4.3		MΩ
C_{IN}	Input Capacitance			1.8		pF
CMIR	Common Mode Input Range			-0.3 to 3.8		V
CMRR	Common Mode Rejection Ratio(1)	DC, V_{cm} = 0V to V_s -1.5	72	87		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 10kΩ to V_s/2		0.027 to 4.97		V
		R_L = 2kΩ to V_s/2		0.036 to 4.953		V
		R_L = 150Ω to V_s/2(1)	0.3	0.12 to 4.8	4.625	V
I_{OUT}	Output Current			±55		mA
		-40°C to +85°C		±50		mA
I_{SC}	Short-Circuit Output Current			±85		mA
V_s	Power Supply Operating Range		2.5	5	5.5	V

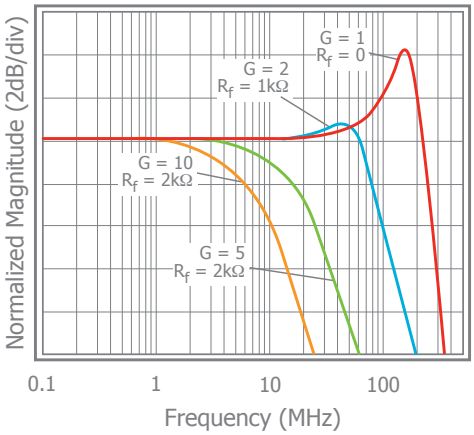
Notes:

1. 100% tested at 25°C.
2. R_f = 1kΩ was used for optimal performance. (For G = +1, R_f = 0).

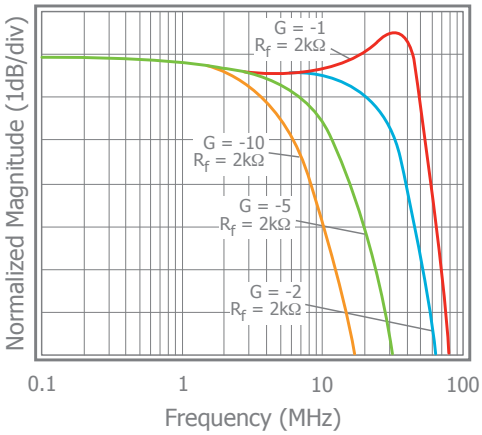
Typical Performance Characteristics

V_S = +5V, G = 2, R_f = 2kΩ, R_L = 2kΩ to V_S/2; unless otherwise noted.

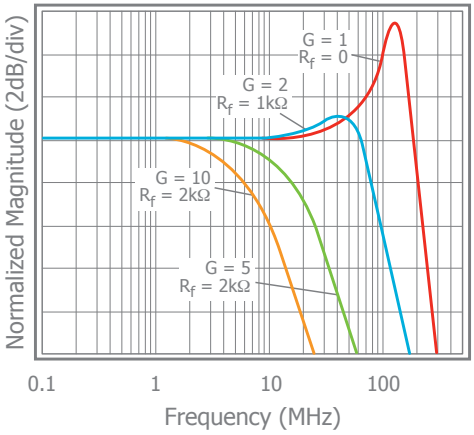
Non-Inverting Frequency Response V_S = +5V



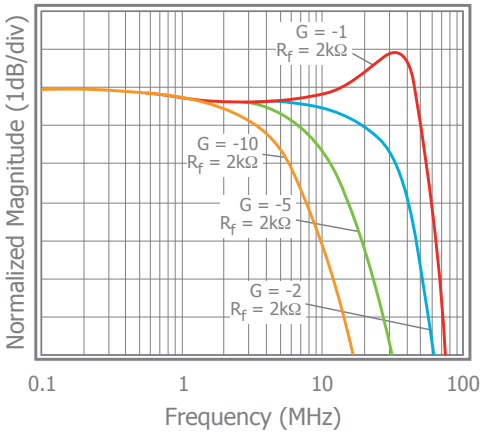
Inverting Frequency Response V_S = +5V



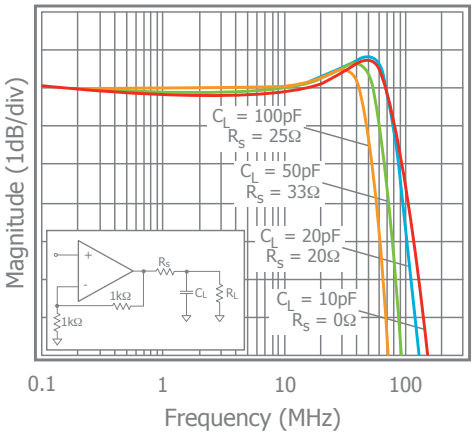
Non-Inverting Frequency Response V_S = +2.7V



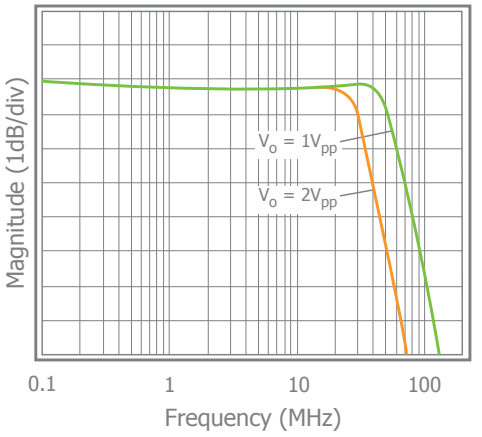
Inverting Frequency Response V_S = +2.7V



Frequency Response vs. C_L



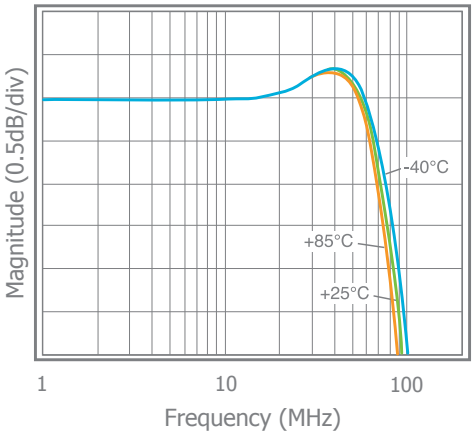
Large Signal Frequency Response



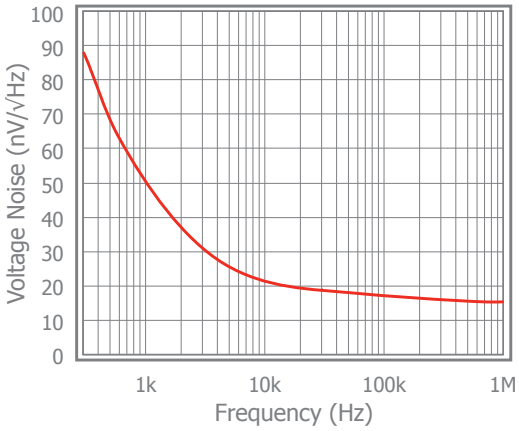
Typical Performance Characteristics

V_S = +5V, G = 2, R_f = 2kΩ, R_L = 2kΩ to V_S/2; unless otherwise noted.

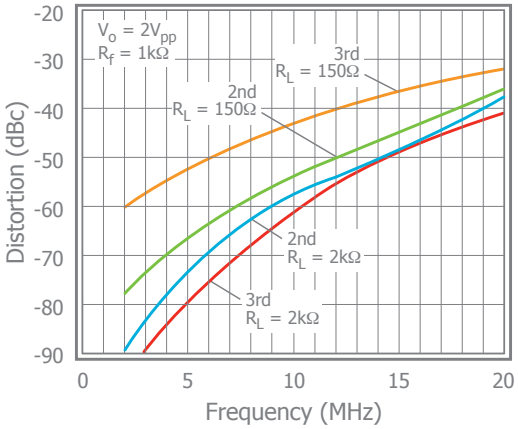
Frequency Response vs. Temperature



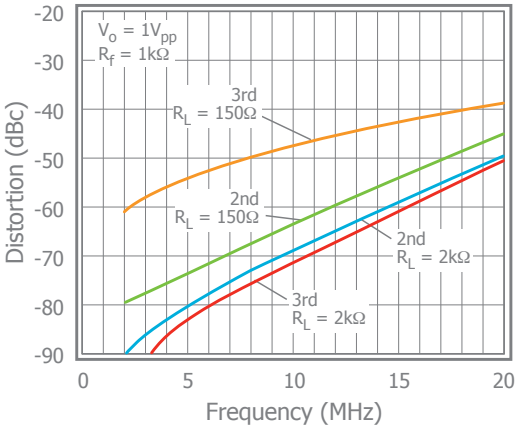
Input Voltage Noise



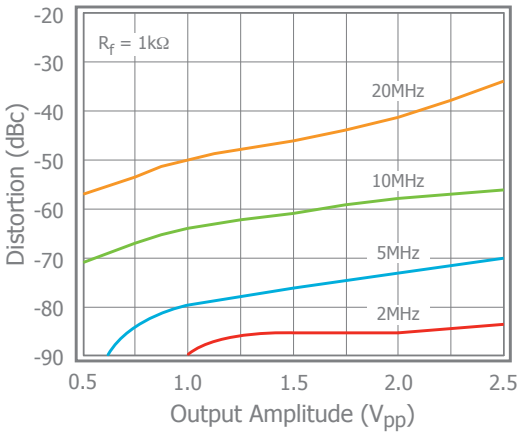
2nd & 3rd Harmonic Distortion; V_S = +5V



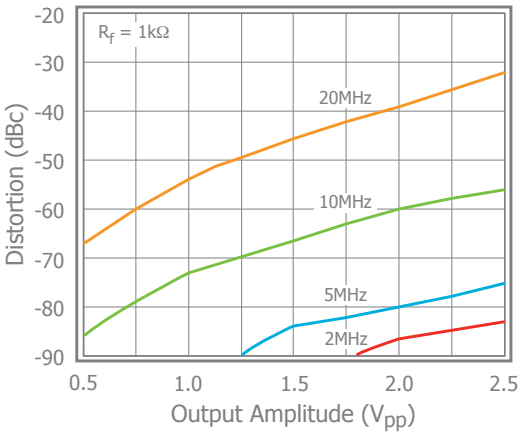
2nd & 3rd Harmonic Distortion; V_S = +2.7V



2nd Harmonic Distortion vs. V_o



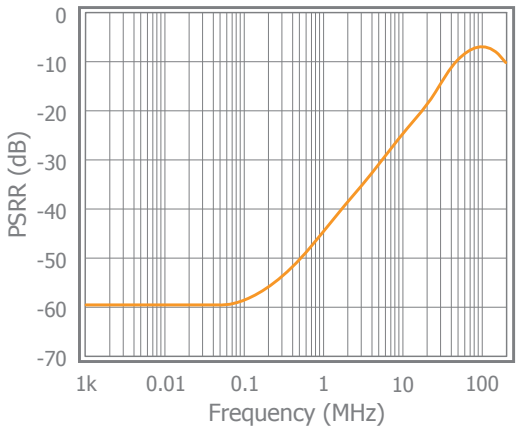
3rd Harmonic Distortion vs. V_o



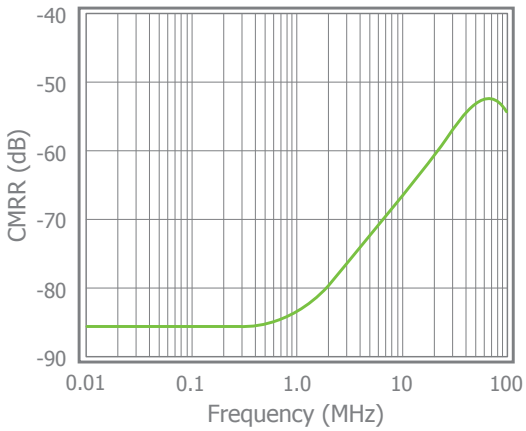
Typical Performance Characteristics

V_S = +5V, G = 2, R_f = 2kΩ, R_L = 2kΩ to V_S/2; unless otherwise noted.

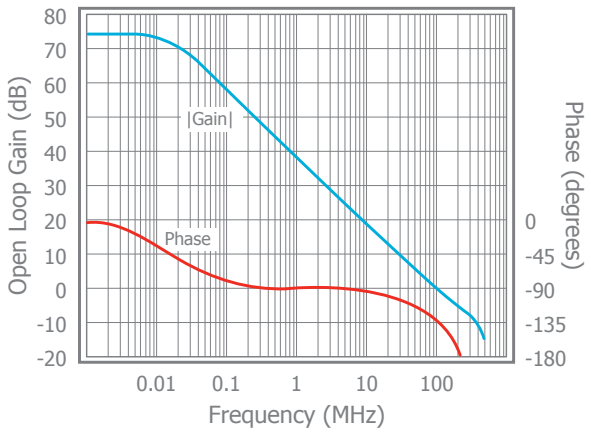
PSRR



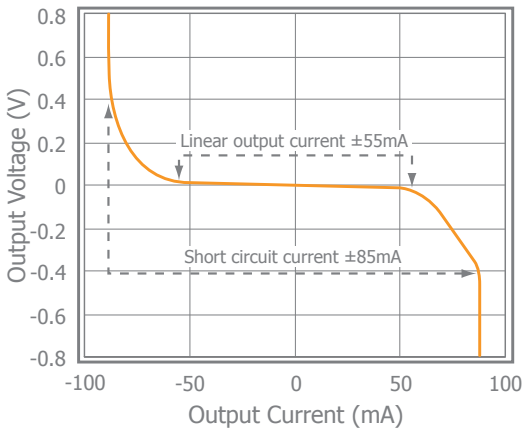
CMRR



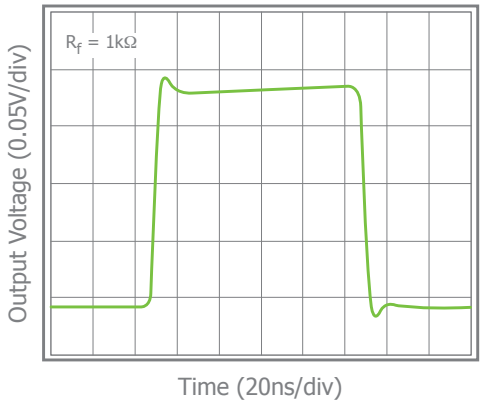
Open Loop Gain & Phase vs. Frequency



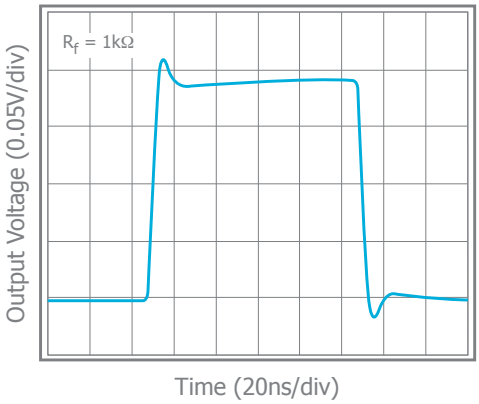
Output Current



Small Signal Pulse Response V_S = +5V



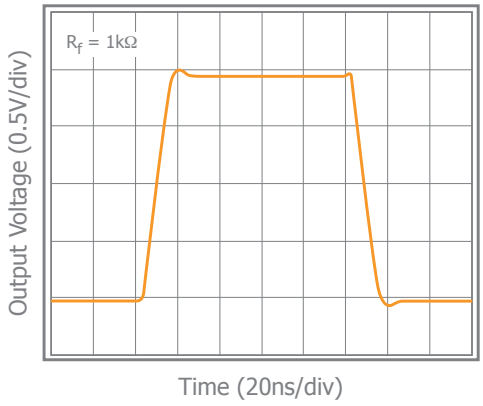
Small Signal Pulse Response V_S = +2.7V



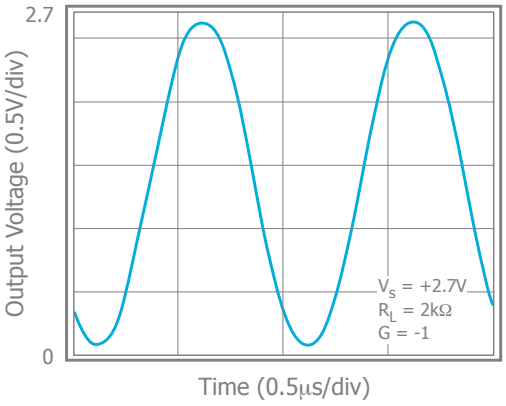
Typical Performance Characteristics

V_S = +5V, G = 2, R_f = 2kΩ, R_L = 2kΩ to V_S/2; unless otherwise noted.

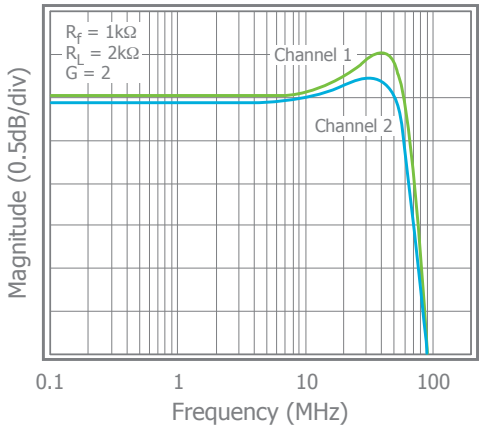
Large Signal Pulse Response V_S = +5V



Output Swing



Channel Matching V_S = +5V



General Description

The CLC2005 is a single supply, general purpose, voltage-feedback amplifier fabricated on a complementary bipolar process using a patent pending topography. It features a rail-to-rail output stage and is unity gain stable. Both gain bandwidth and slew rate are insensitive to temperature.

The common mode input range extends to 300mV below ground and to 1.2V below V_S. Exceeding these values will not cause phase reversal. However, if the input voltage exceeds the rails by more than 0.5V, the input ESD devices will begin to conduct. The output will stay at the rail during this overdrive condition.

The design uses a Darlington output stage. The output stage is short circuit protected and offers "soft" saturation protection that improves recovery time.

The typical circuit schematic is shown in Figure 1.

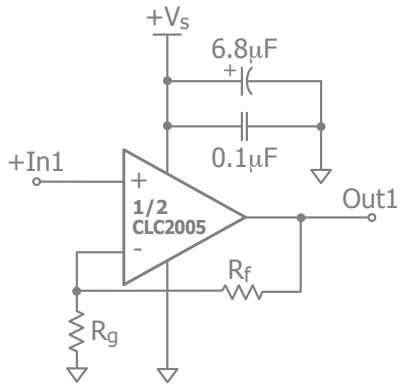


Figure 1: Typical Configuration

At non-inverting gains other than G = +1, keep R_g below 1kΩ to minimize peaking; thus, for optimum response at a gain of +2, a feedback resistor of 1kΩ is recommended. Figure 2 illustrates the CLC2005 frequency response with both 1kΩ and 2kΩ feedback resistors.

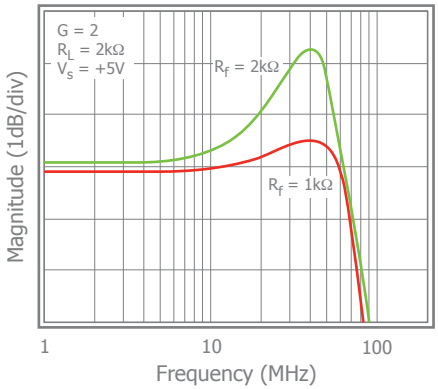


Figure 2: Frequency Response vs. R_f

Power Dissipation

The maximum internal power dissipation allowed is directly related to the maximum junction temperature. If the maximum junction temperature exceeds 150°C, some reliability degradation will occur. If the maximum junction temperature exceeds 175°C for an extended time, device failure may occur.

The CLC2005 is short circuit protected. However, this may not guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. Follow the maximum power derating curves shown in Figure 3 to ensure proper operation.

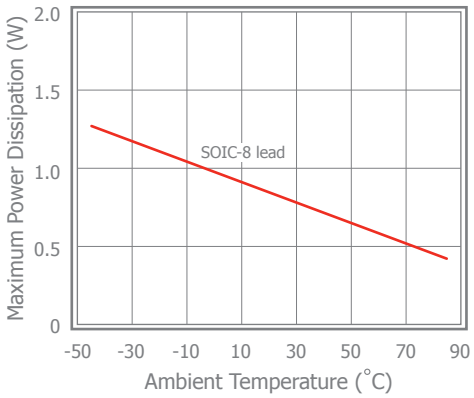


Figure 3: Power Derating Curves

Overdrive Recovery

For an amplifier, an overdrive condition occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the ranges are exceeded. The CLC2005 will typically recover in less than 20ns from an overdrive condition. Figure 4 shows the CLC2005 in an overdriven condition.

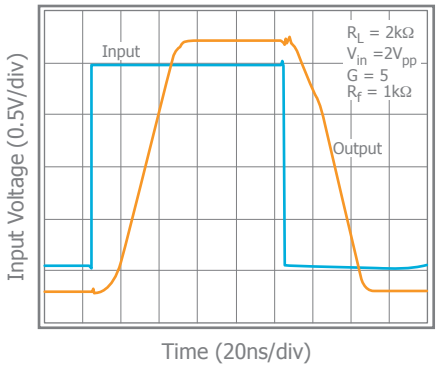


Figure 4: Overdrive Recovery

Driving Capacitive Loads

The *Frequency Response vs. C_L* plot on page 6, illustrates the response of the CLC2005. A small series resistance (R_S) at the output of the amplifier, illustrated in Figure 5, will improve stability and settling performance. R_S values in the *Frequency Response vs. C_L* plot were chosen to achieve maximum bandwidth with less than 1dB of peaking. For maximum flatness, use a larger R_S.

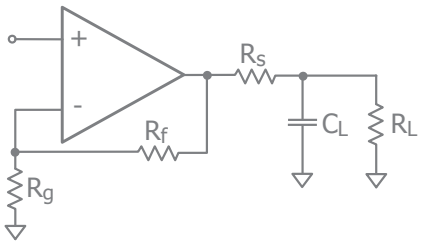


Figure 5: Typical Topology for driving a capacitive load

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Cadeka has evaluation boards to use as a guide for high frequency layout and to aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF and 0.1µF ceramic capacitors
- Place the 6.8µF capacitor within 0.75 inches of the power pin
- Place the 0.1µF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts shown in Figure 7 for more information.

When evaluating only one channel, complete the following on the unused channel:

1. Ground the non-inverting input.
2. Short the output to the inverting input.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of this device:

Eval Board	Description	Products
CEB006	Dual Channel, Dual Supply 8 lead SOIC	CLC2005SO8

Evaluation board schematics and layouts are shown in Figure 6 and Figure 7.

The CEB006 evaluation board is built for dual supply operation. Follow these steps to use the board in a single supply application:

1. Short -V_S to ground.
2. Use C3 and C4, if the -V_S pin of the CLC2005 is not directly connected to the ground plane.

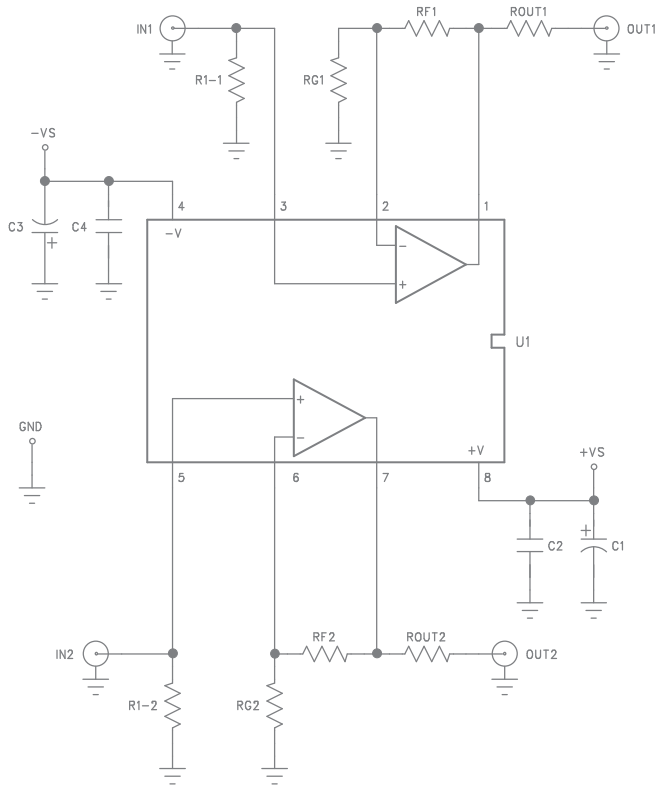


Figure 6: Evaluation Board Schematic

CLC2005 Evaluation Board Layout

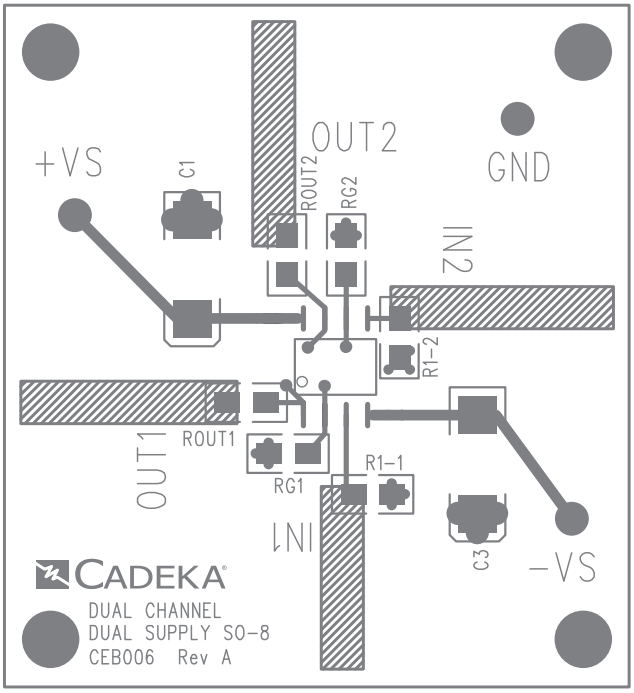


Figure 7a: CEB006 (Top)

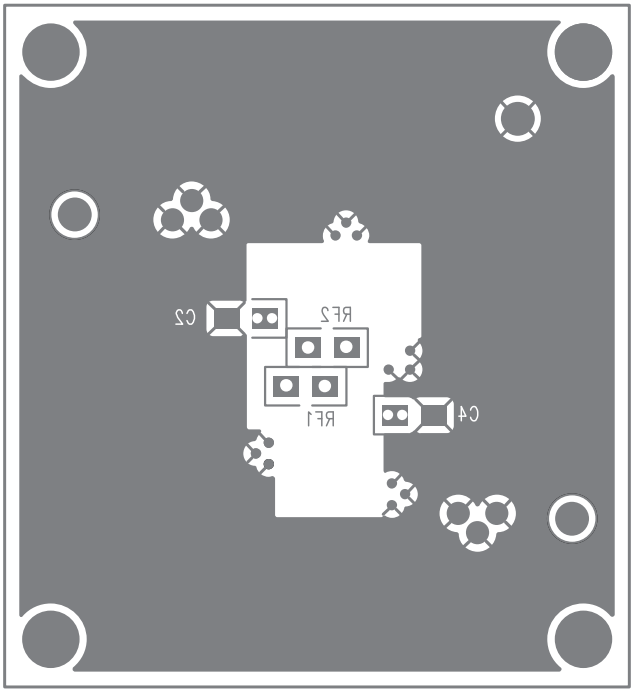
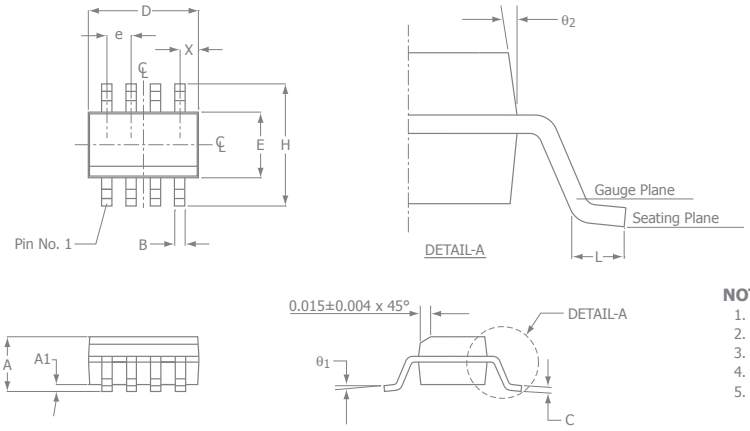


Figure 7b: CEB006 (Bottom)

Mechanical Dimensions

SOIC-8 Package



SOIC-8		
SYMBOL	**MIN**	**MAX**
A	0.054	0.068
A1	0.004	0.0098
B	0.014	0.019
D	0.189	0.196
E	0.150	0.157
H	0.229	0.244
e	0.050 BSC	
C	0.0075	0.0098
L	0.016	0.034
X	0.0215 Ref	
θ_1	0°	8°
θ_2	7° BSC	

NOTE:

1. All dimensions are in inches.
2. Lead coplanarity should be 0" to 0.004" max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.0075" from the lead tip.

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