

# 1.8 V to 5.5 V, 80 μA, 8 BIT, LOW POWER, SINGLE CHANNEL, DIGITAL-TO-ANALOG CONVERTER

#### **FEATURES**

Qualified for Automotive Applications

Relative Accuracy: 0.25 LSB INL

Micro-Power Operation: 80 μA at 1.8 V

Power-Down: 0.5 μA at 5 V, 0.1 μA at 1.8 V

Wide Power Supply: 1.8 V to 5.5 V

Power-On Reset to Zero Scale

· Straight Binary Data Format

 Low Power Serial Interface With Schmitt-Triggered Inputs: Up to 50 MHz

 On-Chip Output Buffer Amplifier, Rail-to-Rail Operation

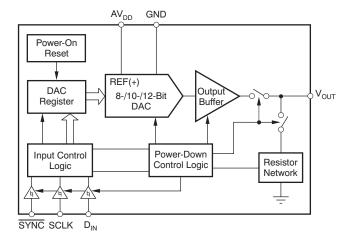
SYNC Interrupt Facility

Tiny 6-Pin SC70 Package

#### **APPLICATIONS**

- Portable, Battery-Powered instruments
- Process Control
- Digital Gain and Offset Adjustment
- Programmable Voltage and Current Sources

RELATED DEVICES	16-BIT	14-BIT	12-BIT	10-BIT	8-BIT
Pin and Function Compatible	DAC8411	DAC8311	DAC7311	DAC6311	DAC5311



#### DESCRIPTION

The DAC5311 is an 8-bit, low-power, single-channel, voltage output, digital-to-analog converters (DAC). It is monotonic by design and provides excellent linearity and minimizes undesired code-to-code transient voltages while offering an easy upgrade path within a pin-compatible family. The device uses a versatile, 3-wire serial interface that operates at clock rates of up to 50 MHz and is compatible with standard SPI™, QSPI™, MICROWIRE™, and digital signal processor (DSP) interfaces.

DAC5311 uses an external power supply as a reference voltage to set the output range. The devices incorporate a power-on reset (POR) circuit that ensures the DAC output powers up at 0 V and remains there until a valid write to the device occurs. It contains a power-down feature, accessed over the serial interface, that reduces current consumption of the device to 0.1  $\mu$ A at 1.8 V in power-down mode. The low power consumption of this part in normal operation makes it ideally suited for portable battery-operated equipment. The power consumption is 0.55 mW at 5 V, reducing to 2.5  $\mu$ W in power-down mode.

DAC5311 is pin-compatible with the DAC8311 and DAC8411, offering an easy upgrade path from 8-bit resolution to 14- and 16-bit resolution. The device is available in a small 6-pin SC70 package. This package offers a flexible solution over the automotive temperature range of –40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SPI, QSPI are trademarks of Motorola, Inc. MICROWIRE is a trademark of National Semiconductor Corporation. All other trademarks are the property of their respective owners.





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	PACKAGE MARKING
-40°C to 85°C	±0.25	±0.25	SC70-6 - DCK	Reel of 3000	DAC5311IDCKRQ1	OCZ

<sup>(1)</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

#### ABSOLUTE MAXIMUM RATINGS(1)

AV <sub>DD</sub> to GND	−0.3 V to 6 V
Digital input voltage to GND	-0.3 V to AV <sub>DD</sub> +0.3 V
AV <sub>OUT</sub> to GND	–0.3 V to AV <sub>DD</sub> +0.3 V
Operating temperature range	-40°C to 85°C
Storage temperature range	-65°C to 150°C
Junction temperature (T <sub>J</sub> max)	150°C
Power dissipation	$(T_J max - T_A)/\theta_{JA} W$
$\theta_{JA}$ thermal impedance	250°C/W

<sup>(1)</sup> Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

Submit Documentation Feedback

<sup>(2)</sup> Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

### **ELECTRICAL CHARACTERISTICS**

At AV  $_{DD}$  = 1.8 V to 5.5 V, R  $_{L}$  = 2 k $\Omega$  to GND, C  $_{L}$  = 200 pF to GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
STATIC PERFORMANCE <sup>(1)</sup>						
Resolution		8			Bits	
Relative accuracy	Measured by the line passing through codes 3 and 252		±0.01	±0.25	LSB	
Differential nonlinearity			±0.01	±0.25	LSB	
Offset error	Measured by the line passing through two codes (2)		±0.05	±4	mV	
Offset error drift			3		μV/°C	
Zero code error	All zeros loaded to the DAC register		0.2		mV	
Full-scale error	All ones loaded to DAC register		0.04	0.2	% of FSR	
Gain error			0.05	±0.15	% of FSR	
Cain tanananatura aaa#iaiaat	AV <sub>DD</sub> = 5 V		±0.5		ppm of	
Gain temperature coefficient	AV <sub>DD</sub> = 1.8 V		±1.5		FSR/°C	
OUTPUT CHARACTERISTICS	3)					
Output voltage range		0		$AV_{DD}$	V	
Output voltage settling time	$R_L$ = 2 k $\Omega$ , $C_L$ = 200 pF, $AV_{DD}$ = 5 V, 1/4 scale to 3/4 scale		6	10	μs	
	$R_L = 2 M\Omega$ , $C_L = 470 pF$		12		μs	
Slew rate			0.7		V/μs	
Connective load atability	R <sub>L</sub> = ∞		470		pF	
Capacitive load stability	$R_L = 2 k\Omega$		1000		pF	
Code change glitch impulse	1-LSB change around major carry		0.5		nV-s	
Digital feed through			0.5		nV-s	
Power-on glitch impulse	$R_L = 2 \text{ k}\Omega, C_L = 200 \text{ pF}, AV_{DD} = 5 \text{ V}$		17		mV	
DC output impedance			0.5		Ω	
Chart aircuit aurrant	AV <sub>DD</sub> = 5 V		50		mA	
Short-circuit current	$AV_{DD} = 3 V$		20		mA	
Power-up time	Coming out of power-down mode		50		μs	
AC PERFORMANCE						
SNR			81		dB	
THD	$T_A$ = 25°C, BW = 20 kHz, 12-bit level, AV <sub>DD</sub> = 5 V,		-65		dB	
SFDR	f <sub>OUT</sub> = 1 kHz, 1st 19 harmonics removed for SNR calculation		65		dB	
SINAD	65		dB			
DAC autout naine density (4)	T <sub>A</sub> = 25°C, at zero-scale input, f <sub>OUT</sub> = 1 kHz, AV <sub>DD</sub> = 5 V		17		nV/√ <del>Hz</del>	
DAC output noise density <sup>(4)</sup>	$T_A$ = 25°C, at mid-code input, $f_{OUT}$ = 1 kHz, $AV_{DD}$ = 5 V		110		nV/√ <del>Hz</del>	
DAC output noise <sup>(5)</sup>	$T_A$ = 25°C, at mid-code input, 0.1 Hz to 10 Hz, $AV_{DD}$ = 5 V		3		$\mu V_{PP}$	

<sup>(1)</sup> Linearity calculated using a reduced code range of 3 to 252, output unloaded.

 <sup>(2)</sup> Straight line passing through codes 3 and 252, output unloaded.
 (3) Specified by design and characterization, not production tested.
 (4) For more details, see Figure 16.

<sup>(5)</sup> For more details, see Figure 17.

## **ELECTRICAL CHARACTERISTICS (continued)**

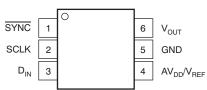
At AV  $_{DD}$  = 1.8 V to 5.5 V, R  $_{L}$  = 2 k $\Omega$  to GND, C  $_{L}$  = 200 pF to GND (unless otherwise noted)

P	ARAMETER	TEST CO	MIN	TYP	MAX	UNIT		
LOGIC INP	JTS <sup>(6)</sup>	1		•		,		
Input curren	t					±1	μΑ	
V. I. Camerill		AV <sub>DD</sub> = 5 V				0.8	V	
V <sub>IN</sub> L, input low voltage		AV <sub>DD</sub> = 1.8 V				0.5	V	
\/    :	-inh waltana	AV <sub>DD</sub> = 5 V		1.8			V	
V <sub>IN</sub> H, input I	nign voitage	AV <sub>DD</sub> = 1.8 V		1.1			V	
Pin capacita	nce				1.5	3	pF	
POWER RE	QUIREMENTS							
AV <sub>DD</sub>				1.8		5.5	V	
	Normal mode	$V_{IN}H = AV_{DD}$ and $V_{IN}L =$ GND, at midscale code (7)	$AV_{DD} = 3.6 \text{ V to } 5.5 \text{ V}$		110	160		
			$AV_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$		95	150	μΑ	
			$AV_{DD} = 1.8 \text{ V to } 2.7 \text{ V}$		80	140		
I <sub>DD</sub>	Power-down mode	$V_{IN}H = AV_{DD}$ and $V_{IN}L =$ GND, at midscale code	$AV_{DD} = 3.6 \text{ V to } 5.5 \text{ V}$		0.5	3.5	μΑ	
			$AV_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$		0.4	3.0		
			$AV_{DD} = 1.8 \text{ V to } 2.7 \text{ V}$		0.1	2.0		
			$AV_{DD} = 3.6 \text{ V to } 5.5 \text{ V}$		0.55	0.88		
	Normal mode	V <sub>IN</sub> H = AV <sub>DD</sub> and V <sub>IN</sub> L = GND, at midscale code	$AV_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$		0.25	0.54	mW	
Power		OND, at midscale code	$AV_{DD} = 1.8 \text{ V to } 2.7 \text{ V}$		0.14	0.38		
dissipation			AV <sub>DD</sub> = 3.6 V to 5.5 V		2.50	19.2		
	Power-down mode	$V_{IN}H = AV_{DD}$ and $V_{IN}L =$ GND, at midscale code	$AV_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$		1.08	10.8	μW	
		O. D., at midsoale code	$AV_{DD} = 1.8 \text{ V to } 2.7 \text{ V}$		0.72	8.1		
TEMPERAT	URE RANGE			"				
Specified pe	rformance range			-40		85	°C	

<sup>(6)</sup> Specified by design and characterization, not production tested.(7) For more details, see Figure 9, Figure 44, and Figure 69.

### **PIN CONFIGURATION**

### DCK PACKAGE SC70-6 (TOP VIEW)



#### **Table 1. PIN DESCRIPTION**

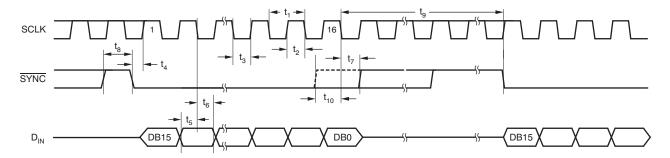
PIN	NAME	DESCRIPTION					
1 SYNC		Level-triggered control input (active low). This is the frame synchronization signal for the input data. When SYNC goes low, it enables the input shift register and data are transferred in on the falling edges of the following clocks. The DAC is updated following 16th clock cycle, unless SYNC is taken high befor this edge, in which case the rising edge of SYNC acts as an interrupt and the write sequence is ignored by the DAC5311. See the SYNC Interrupt section for more details.					
2	SCLK	Serial clock input. Data can be transferred at rates up to 50 MHz.					
3	D <sub>IN</sub>	Serial data input. Data is clocked into the 16-bit input shift register on the falling edge of the serial clock input.					
4	AV <sub>DD</sub> /V <sub>REF</sub>	Power supply input, 1.8 V to 5.5 V.					
5	GND	Ground reference point for all circuitry on the part.					
6	$V_{OUT}$	Analog output voltage from DAC. The output amplifier has rail-to-rail operation.					

SBAS470-JUNE 2009

www.ti.com

**DAC5311-Q1 INSTRUMENTS** 

### **SERIAL WRITE OPERATION**



## TIMING REQUIREMENTS(1)

All specifications at -40°C to 85°C,  $AV_{DD}$  = 1.8 V to 5.5 V (unless otherwise noted)

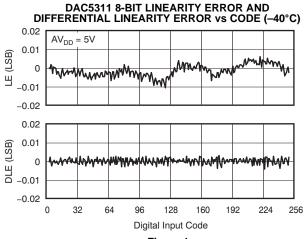
	PARAMETER	TEST CONDITIONS	MIN	TYP MAX	UNIT	
t <sub>1</sub> <sup>(2)</sup>	COLK avala tima	AV <sub>DD</sub> = 1.8 V to 3.6 V	50			
ι <sub>1</sub> ` ΄	SCLK cycle time	$AV_{DD} = 3.6 \text{ V to } 5.5 \text{ V}$	20		ns	
	SCLK high time	$AV_{DD} = 1.8 \text{ V to } 3.6 \text{ V}$	25		no	
t <sub>2</sub>	SCEN High time	$AV_{DD} = 3.6 \text{ V to } 5.5 \text{ V}$	10		ns	
	SCLK low time	AV <sub>DD</sub> = 1.8 V to 3.6 V	25			
t <sub>3</sub>	SCEN low time	AV <sub>DD</sub> = 3.6 V to 5.5 V	10		ns	
	CVNC to CCL K riging adds sotup time	AV <sub>DD</sub> = 1.8 V to 3.6 V	0		ne	
t <sub>4</sub>	SYNC to SCLK rising edge setup time	$AV_{DD} = 3.6 \text{ V to } 5.5 \text{ V}$	0		ns	
	Data satur time	$AV_{DD} = 1.8 \text{ V to } 3.6 \text{ V}$			ns	
t <sub>5</sub>	Data setup time	$AV_{DD} = 3.6 \text{ V to } 5.5 \text{ V}$				
	Data hold time	$AV_{DD} = 1.8 \text{ V to } 3.6 \text{ V}$				
t <sub>6</sub>	Data floid time	$AV_{DD} = 3.6 \text{ V to } 5.5 \text{ V}$	4.5		ns	
	SCLK falling edge to SYNC rising edge	$AV_{DD} = 1.8 \text{ V to } 3.6 \text{ V}$			ns	
t <sub>7</sub>	SCEN failing edge to STNC rising edge	AV <sub>DD</sub> = $3.6 \text{ V to } 5.5 \text{ V}$				
	Minimum SYNC high time	AV <sub>DD</sub> = 1.8 V to 3.6 V	50			
t <sub>8</sub>	Minimum SYNC night time	AV <sub>DD</sub> = 3.6 V to 5.5 V	20		ns	
	46th CCLIV follow adds to CVNC follow adds	$AV_{DD} = 1.8 \text{ V to } 3.6 \text{ V}$			ns	
t <sub>9</sub>	16th SCLK falling edge to SYNC falling edge	AV <sub>DD</sub> = 3.6 V to 5.5 V				
	SYNC rising edge to 16th SCLK falling edge	AV <sub>DD</sub> = 1.8 V to 3.6 V	15		ns	
t <sub>10</sub>	(for successful SYNC interrupt)					

All input signals are specified with  $t_R$  =  $t_F$  = 3 ns (10% to 90% of AV<sub>DD</sub>) and timed from a voltage level of (V<sub>IL</sub> + V<sub>IH</sub>)/2. Maximum SCLK frequency is 50 MHz at AV<sub>DD</sub> = 3.6 V to 5.5 V and 20 MHz at AV<sub>DD</sub> = 1.8 V to 3.6 V.



### TYPICAL CHARACTERISTICS: AVDD = 5 V

At T<sub>A</sub> = 25°C, AV<sub>DD</sub> = 5 V, and DAC loaded with midscale code (unless otherwise noted)





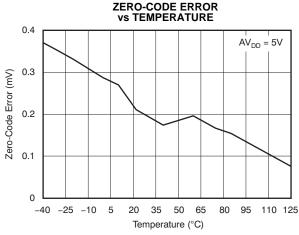


Figure 2.

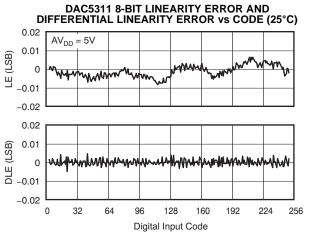


Figure 3.

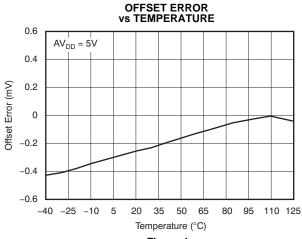
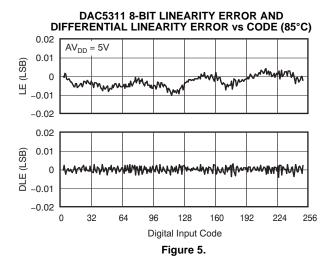


Figure 4.



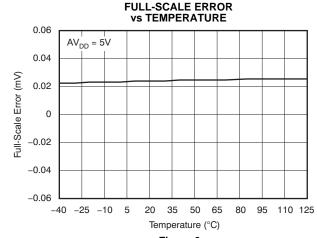
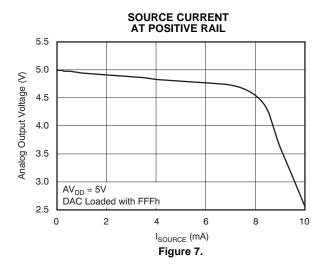
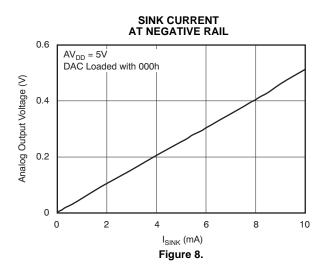


Figure 6.

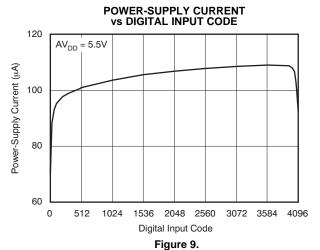
## TYPICAL CHARACTERISTICS: AV<sub>DD</sub> = 5 V (continued)

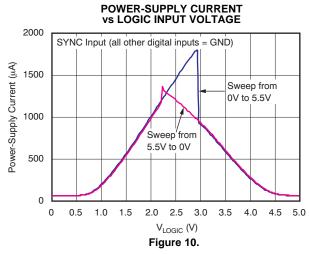
At  $T_A = 25$ °C,  $AV_{DD} = 5$  V, and DAC loaded with midscale code (unless otherwise noted)

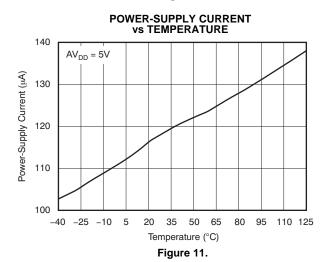


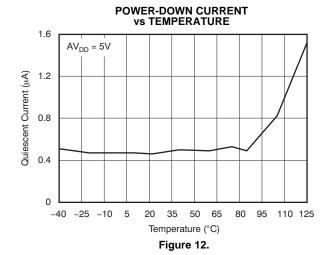


Instruments



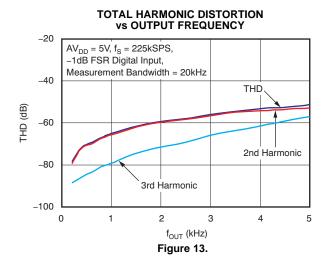


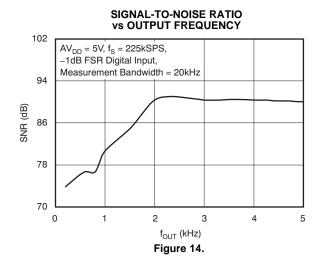


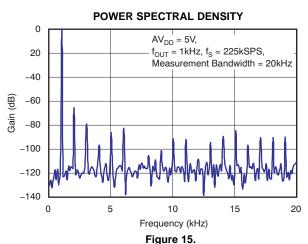


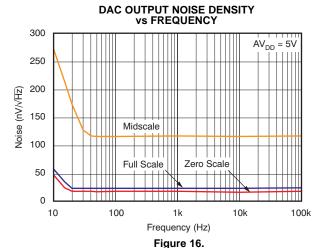
## TYPICAL CHARACTERISTICS: AV<sub>DD</sub> = 5 V (continued)

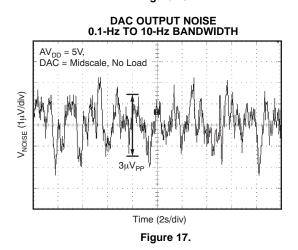
At  $T_A = 25$ °C,  $AV_{DD} = 5$  V, and DAC loaded with midscale code (unless otherwise noted)











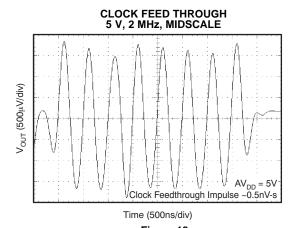
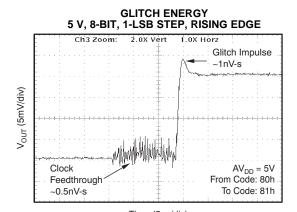


Figure 18.

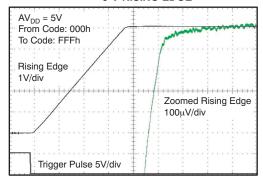
## TYPICAL CHARACTERISTICS: AV<sub>DD</sub> = 5 V (continued)

At  $T_A = 25$ °C,  $AV_{DD} = 5$  V, and DAC loaded with midscale code (unless otherwise noted)



Time (5μs/div) Figure 19.

#### FULL-SCALE SETTLING TIME 5-V RISING EDGE



Time (2µs/div)

HALF-SCALE SETTLING TIME 5-V RISING EDGE

Figure 21.

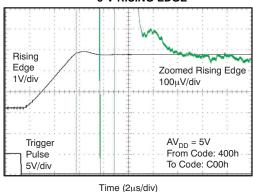
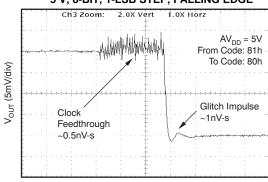


Figure 23.

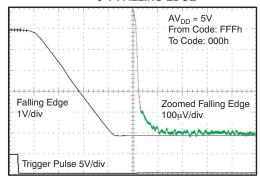
#### GLITCH ENERGY 5 V, 8-BIT, 1-LSB STEP, FALLING EDGE

**INSTRUMENTS** 



Time (5μs/div) Figure 20.

#### FULL-SCALE SETTLING TIME 5-V FALLING EDGE



Time (2µs/div)

Figure 22.

#### HALF-SCALE SETTLING TIME 5-V FALLING EDGE

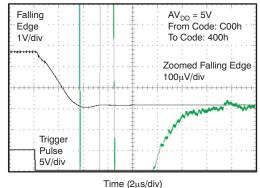


Figure 24.



## TYPICAL CHARACTERISTICS: AV<sub>DD</sub> = 5 V (continued)

At  $T_A = 25$ °C,  $AV_{DD} = 5$  V, and DAC loaded with midscale code (unless otherwise noted)

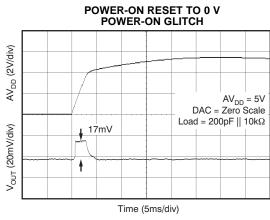


Figure 25.

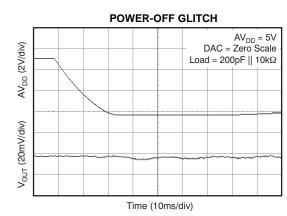


Figure 26.

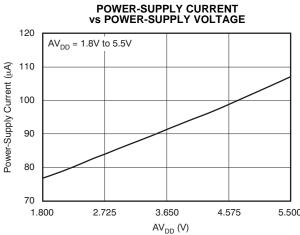


Figure 27.

5.500

POWER-DOWN CURRENT vs POWER-SUPPLY VOLTAGE

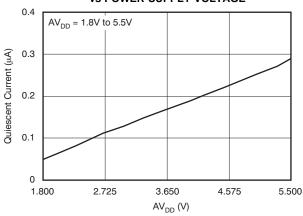


Figure 28.

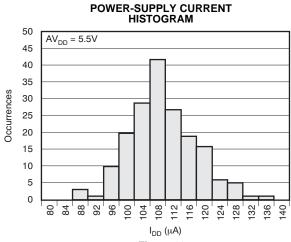
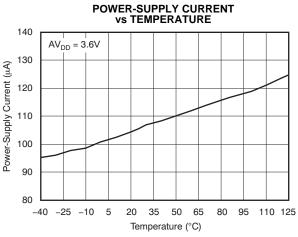


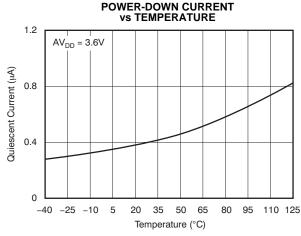
Figure 29.

## TYPICAL CHARACTERISTICS: AV<sub>DD</sub> = +3.6 V

At  $T_A = 25$ °C,  $AV_{DD} = +3.6$  V, and DAC loaded with midscale code (unless otherwise noted)







Instruments

Figure 31.

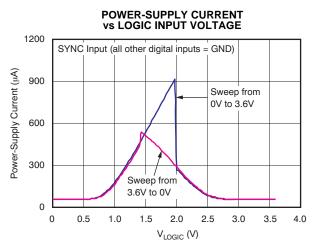
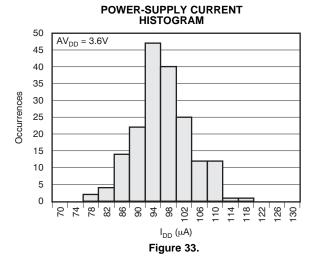
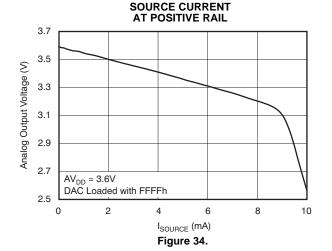


Figure 32.



SINK CURRENT AT NEGATIVE RAIL AV<sub>DD</sub> = 3.6V



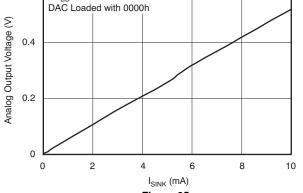
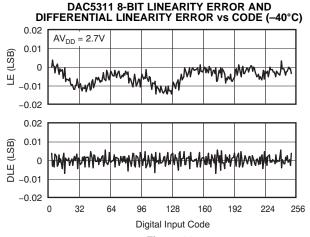


Figure 35.

0.6

### TYPICAL CHARACTERISTICS: AV<sub>DD</sub> = 2.7 V

At  $T_A = 25$ °C,  $AV_{DD} = 2.7$  V, and DAC loaded with midscale code (unless otherwise noted)





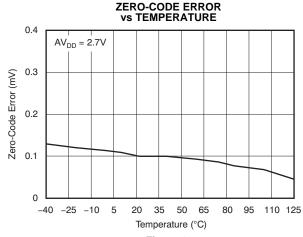


Figure 37.

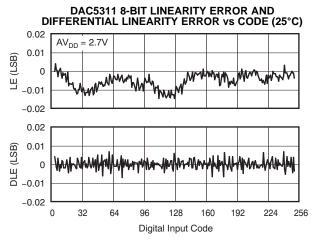


Figure 38.

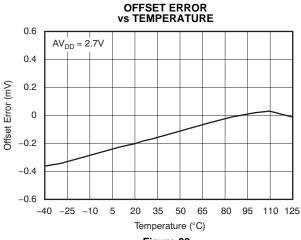
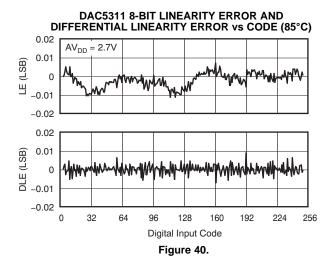


Figure 39.



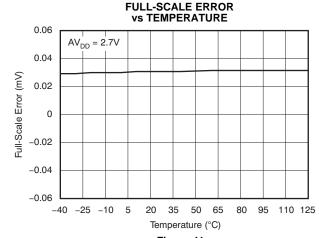
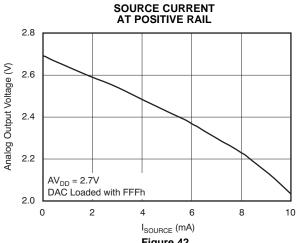
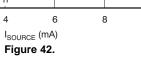


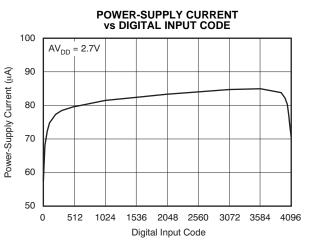
Figure 41.

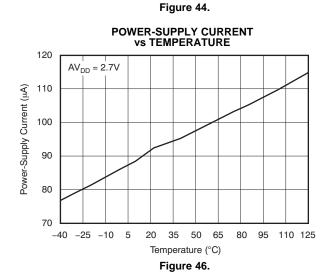
## TYPICAL CHARACTERISTICS: AV<sub>DD</sub> = 2.7 V (continued)

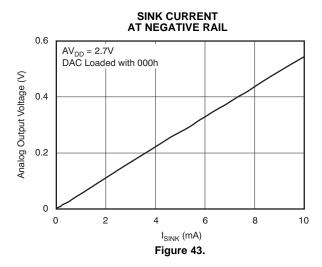
At  $T_A = 25$ °C,  $AV_{DD} = 2.7$  V, and DAC loaded with midscale code (unless otherwise noted)



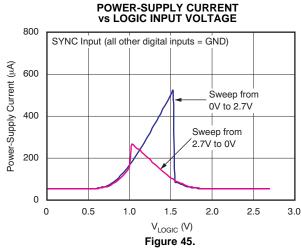


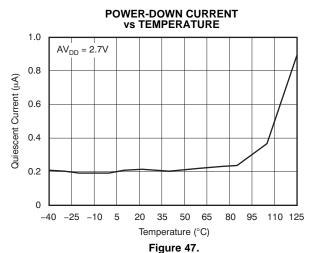






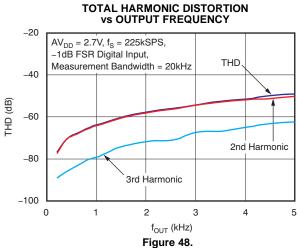
Instruments



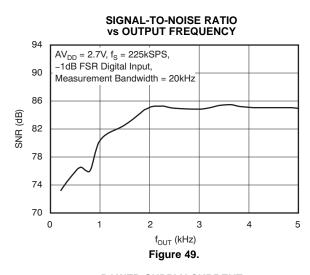


### TYPICAL CHARACTERISTICS: $AV_{DD} = 2.7 \text{ V (continued)}$

At  $T_A = 25$ °C,  $AV_{DD} = 2.7$  V, and DAC loaded with midscale code (unless otherwise noted)







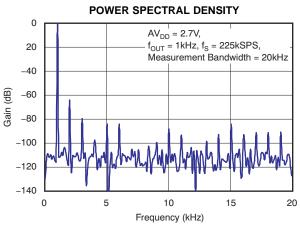
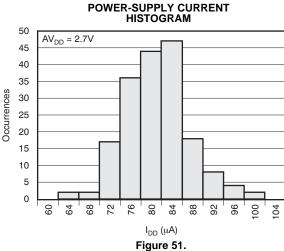
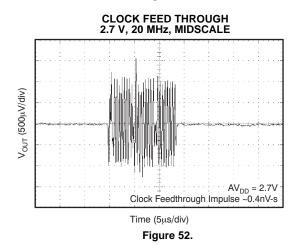


Figure 50.







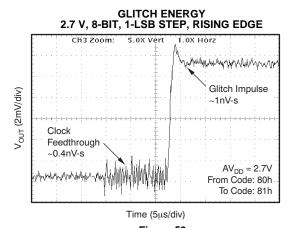
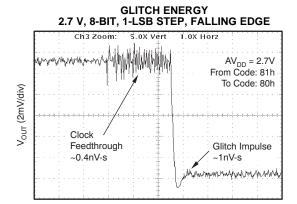


Figure 53.

## TYPICAL CHARACTERISTICS: AV<sub>DD</sub> = 2.7 V (continued)

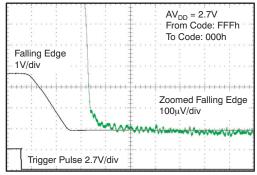
At  $T_A = 25$ °C,  $AV_{DD} = 2.7$  V, and DAC loaded with midscale code (unless otherwise noted)



Time (5µs/div)

Figure 54.

#### FULL-SCALE SETTLING TIME 2.7-V FALLING EDGE



Time (2µs/div)

Figure 56.

## HALF-SCALE SETTLING TIME 2.7-V FALLING EDGE

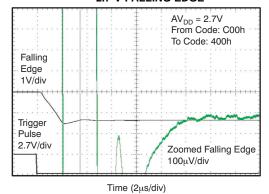


Figure 58.

#### FULL-SCALE SETTLING TIME 2.7-V RISING EDGE

**INSTRUMENTS** 

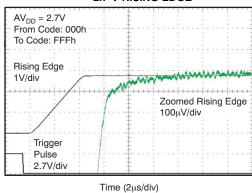
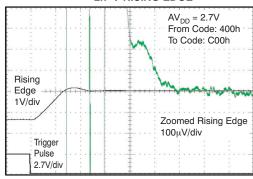


Figure 55.

#### HALF-SCALE SETTLING TIME 2.7-V RISING EDGE



Time (2μs/div)

Figure 57.

#### POWER-ON RESET TO 0 V POWER-ON GLITCH

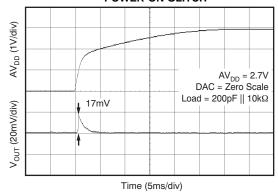


Figure 59.



## TYPICAL CHARACTERISTICS: $AV_{DD} = 2.7 \text{ V (continued)}$

At  $T_A = 25$  °C,  $AV_{DD} = 2.7$  V, and DAC loaded with midscale code (unless otherwise noted)

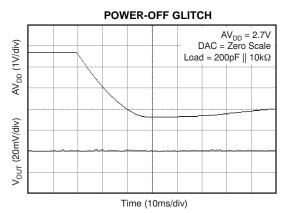
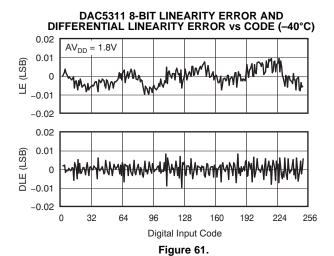
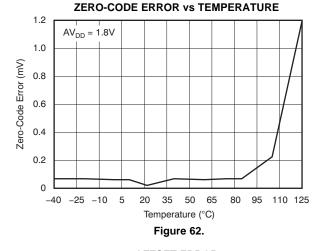


Figure 60.

## TYPICAL CHARACTERISTICS: AVDD = 1.8 V

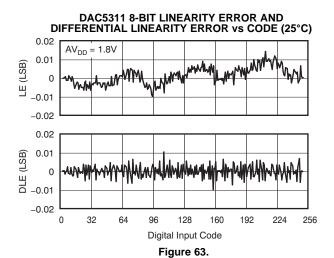
At T<sub>A</sub> = 25°C, AV<sub>DD</sub> = 1.8 V, and DAC loaded with midscale code (unless otherwise noted)

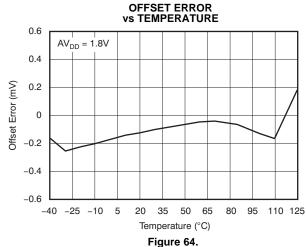


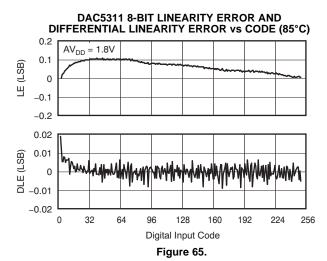


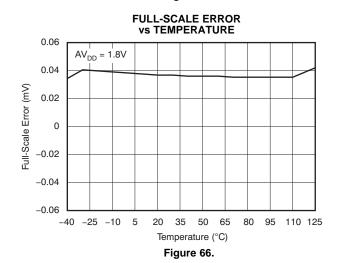
Texas

**I**NSTRUMENTS





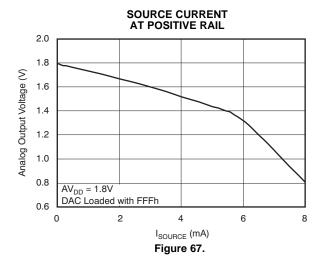


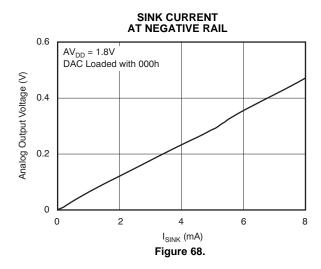


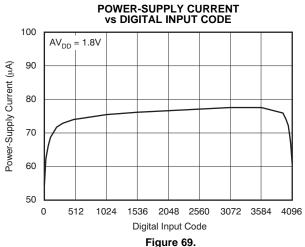


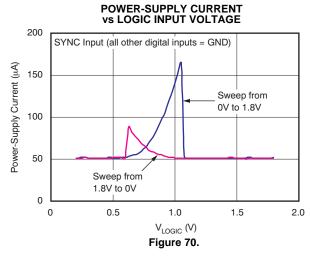
## TYPICAL CHARACTERISTICS: AV<sub>DD</sub> = 1.8 V (continued)

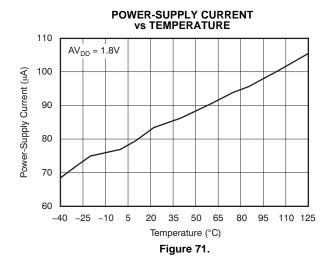
At  $T_A = 25$ °C,  $AV_{DD} = 1.8$  V, and DAC loaded with midscale code (unless otherwise noted)

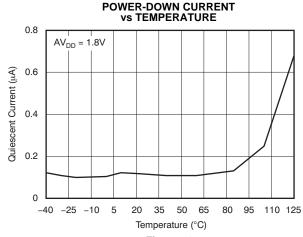












#### TEXAS INSTRUMENTS

## TYPICAL CHARACTERISTICS: AV<sub>DD</sub> = 1.8 V (continued)

At  $T_A = 25$ °C,  $AV_{DD} = 1.8$  V, and DAC loaded with midscale code (unless otherwise noted)

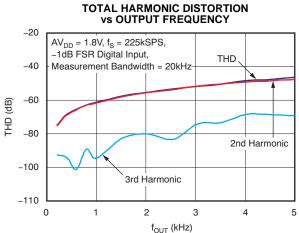
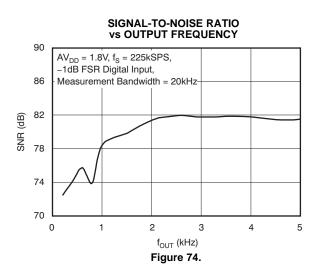
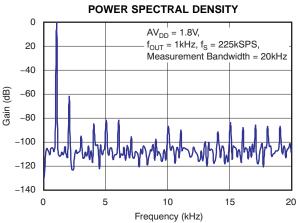


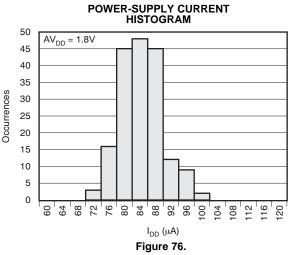
Figure 73.

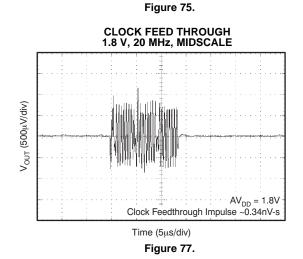












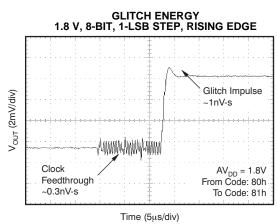
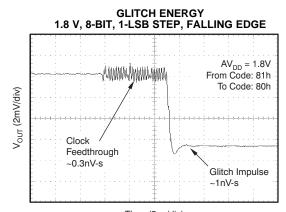


Figure 78.

20

### TYPICAL CHARACTERISTICS: AV<sub>DD</sub> = 1.8 V (continued)

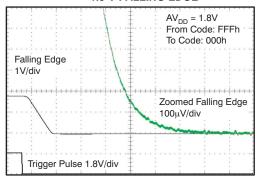
At  $T_A = 25$ °C,  $AV_{DD} = 1.8$  V, and DAC loaded with midscale code (unless otherwise noted)



Time (5 $\mu$ s/div)

Figure 79.

#### FULL-SCALE SETTLING TIME 1.8-V FALLING EDGE



Time (2µs/div)

Figure 81.

#### HALF-SCALE SETTLING TIME 1.8-V FALLING EDGE

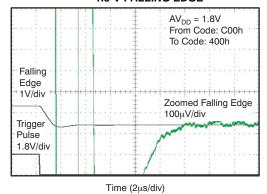
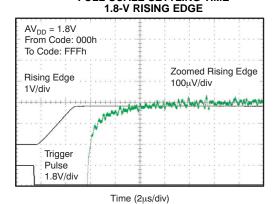


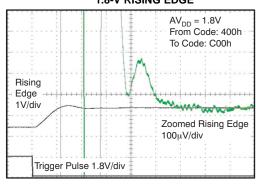
Figure 83.



**FULL-SCALE SETTLING TIME** 

Figure 80.

#### HALF-SCALE SETTLING TIME 1.8-V RISING EDGE



Time (2µs/div)

Figure 82.

#### POWER-ON RESET TO 0 V POWER-ON GLITCH

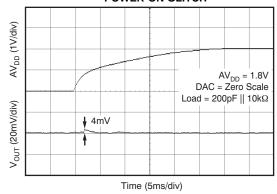


Figure 84.

## TYPICAL CHARACTERISTICS: AV<sub>DD</sub> = 1.8 V (continued)

At  $T_A = 25$  °C,  $AV_{DD} = 1.8$  V, and DAC loaded with midscale code (unless otherwise noted)

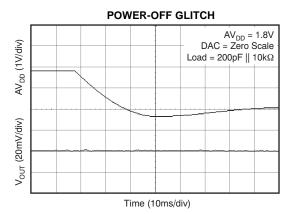


Figure 85.

#### THEORY OF OPERATION

#### **DAC SECTION**

The DAC5311 is fabricated using TI's proprietary HPA07 process technology. The architecture consists of a string DAC followed by an output buffer amplifier. Because there is no reference input pin, the power supply (AV<sub>DD</sub>) acts as the reference. Figure 86 shows a block diagram of the DAC architecture.

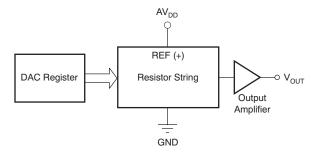


Figure 86. DAC5311 Architecture

The input coding to the DAC5311 is straight binary, so the ideal output voltage is given by:

$$V_{OUT} = AV_{DD} \times \frac{D}{2^n}$$

#### Where:

n = resolution in bits (8)

D = decimal equivalent of the binary code that is loaded to the DAC register. It ranges from 0 to 255 for 8-bit DAC5311.



#### RESISTOR STRING

The resistor string section is shown in Figure 87. It is simply a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. It is tested monotonic because it is a string of resistors.

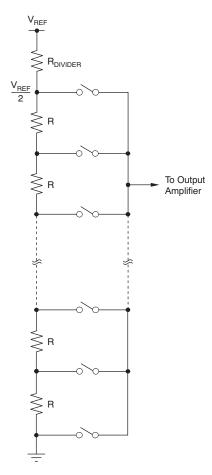


Figure 87. Resistor String

#### **OUTPUT AMPLIFIER**

The output buffer amplifier is capable of generating rail-to-rail voltages on its output which gives an output range of 0 V to  $AV_{DD}$ . It is capable of driving a load of 2 k $\Omega$  in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in the Typical Characteristics section for the given voltage input. The slew rate is 0.7 V/ $\mu$ s with a half-scale settling time of typically 6 $\mu$ s with the output unloaded.

#### **SERIAL INTERFACE**

The DAC5311 has a 3-wire serial interface (SYNC, SCLK, and DIN) compatible with SPI, QSPI, and Microwire interface standards, as well as most DSPs. See the Serial Write Operation timing diagram for an example of a typical write sequence.

#### Input Shift Register

The input shift register is 16 bits wide, as shown in Table 2. The first two bits (PD0 and PD1) are reserved control bits that set the desired mode of operation (normal mode or any one of three power-down modes) as indicated in Table 3.

The remaining data bits are eight data bits, followed by don't care bits, as shown in Table 2.

24

The write sequence begins by bringing the SYNC line low. Data from the DIN line are clocked into the 16-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 50 MHz, making the DAC5311 compatible with high-speed DSPs. On the 16th falling edge of the serial clock, the last data bit is clocked in and the programmed function is executed.

At this point, the SYNC line may be kept low or brought high. In either case, it must be brought high for a minimum of 20 ns before the next write sequence so that a falling edge of SYNC can initiate the next write sequence. As previously mentioned, it must be brought high again before the next write sequence.

#### **SYNC** Interrupt

In a normal write sequence, the SYNC line is kept <u>low for</u> at least 16 falling edges of SCLK and the DAC is updated on the 16th falling edge. However, bringing SYNC high before the 16th falling edge acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs, as shown in Figure 88.

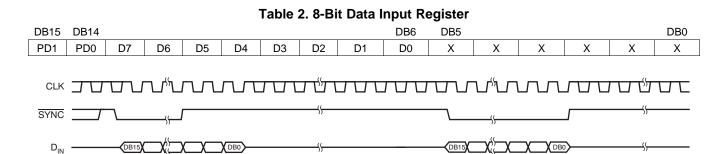


Figure 88. DAC5311 SYNC Interrupt Facility

Valid Write Sequence:

Output Updates on 16th Falling Edge

#### POWER-ON RESET TO ZERO-SCALE

Invalid Write Sequence:

SYNC HIGH before 16th Falling Edge

The DAC5311 contains a power-on reset circuit that controls the output voltage during power-up. On power-up, the DAC register is filled with zeros and the output voltage is 0 V. The DAC register remains that way until a valid write sequence is made to the DAC. This design is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

The occurring power-on glitch impulse is only a few millivolts (typically, 17 mV; see Figure 25).



#### **POWER-DOWN MODES**

The DAC5311 contains four separate modes of operation. These modes are programmable by setting two bits (PD1 and PD0) in the control register. Table 3 shows how the state of the bits corresponds to the mode of operation of the device.

PD1	PD0	OPERATING MODE							
Normal Mod	Normal Mode								
0	0	Normal Operation							
Power-Down	Power-Down Modes								
0	1	Output 1 kΩ to GND							
1	0	Output 100 kΩ to GND							
1	1	High-Z							

When both bits are set to '0', the device works normally with a standard power consumption of typically 80  $\mu$ A at 1.8 V. However, for the three power-down modes, the typical supply current falls to 0.5  $\mu$ A at 5 V, 0.4  $\mu$ A at 3V, and 0.1  $\mu$ A at 1.8 V. Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. The advantage of this architecture is that the output impedance of the part is known while the part is in power-down mode. There are three different options. The output is connected internally to GND either through a 1-k $\Omega$  resistor or a 100-k $\Omega$  resistor, or is left open-circuited (High-Z). Figure 89 illustrates the output stage.

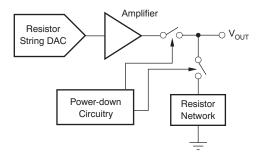


Figure 89. Output Stage During Power-Down

All linear circuitry is shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 50  $\mu$ s for AV<sub>DD</sub> = 5 V and AV<sub>DD</sub> = 3 V.

#### **DAC NOISE PERFORMANCE**

Typical noise performance is shown in *Typical Characteristics*. Output noise spectral density at the  $V_{OUT}$  pin versus frequency is depicted for full-scale, midscale, and zero-scale input codes. The typical noise density for midscale code is 110 nV/ $\sqrt{\text{Hz}}$  at 1 kHz and at 1 MHz.

6 Submit Documentation Feedback

#### **APPLICATION INFORMATION**

#### USING THE REF5050 AS A POWER SUPPLY FOR THE DAC5311

As a result of the extremely low supply current required by the DAC5311, an alternative option is to use a REF5050 5 V precision voltage reference to supply the required voltage to the part, as shown in Figure 90. This option is especially useful if the power supply is too noisy or if the system supply voltages are at some value other than 5 V. The REF5050 outputs a steady supply voltage for the DAC5311. If the REF5050 is used, the current needed to supply DAC5311 is typically 110  $\mu$ A at 5 V, with no load on the output of the DAC. When the DAC output is loaded, the REF5050 also needs to supply the current to the load. The total current required (with a 5-k $\Omega$  load on the DAC output) is:

110 
$$\mu$$
A + (5 V/5 k $\Omega$ ) = 1.11 mA

The load regulation of the REF5050 is typically 0.002%/mA, which results in an error of 90  $\mu$ V for the 1.1 mA current drawn from it.

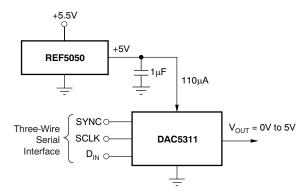


Figure 90. REF5050 as Power Supply to DAC5311

For other power-supply voltages, alternative references such as the REF3030 (3 V), REF3033 (3.3 V), or REF3220 (2.048 V) are recommended. For a full list of available voltage references from TI, see the TI web site at www.ti.com.

#### **BIPOLAR OPERATION**

The DAC5311 has been designed for single-supply operation but a bipolar output range is also possible using the circuit in Figure 91. The circuit shown gives an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an OPA211, OPA340, or OPA703 as the output amplifier. For a full list of available operational amplifiers from TI, see the TI web site at www.ti.com

The output voltage for any input code can be calculated as follows:

$$V_{O} = \left[ AV_{DD} \times \left( \frac{D}{2^{n}} \right) \times \left( \frac{R_{1} + R_{2}}{R_{1}} \right) - AV_{DD} \times \left( \frac{R_{2}}{R_{1}} \right) \right]$$
(1)

Where:

n = resolution in bits (8)

D = decimal equivalent of the binary code that is loaded to the DAC register. It ranges from 0 to 255 for 8-bit DAC5311.

With  $AV_{DD} = 5 \text{ V}$ ,  $R_1 = R_2 = 10 \text{ k}\Omega$ :

$$V_{O} = \left(\frac{10 \times D}{2^{n}}\right) - 5V \tag{2}$$

This is an output voltage range of ±5 V with 00h corresponding to a -5 V output and FFh corresponding to a 5-V output.

TEXAS INSTRUMENTS

SBAS470-JUNE 2009 www.ti.com

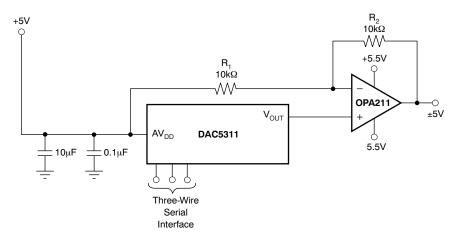
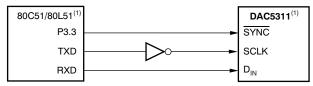


Figure 91. Bipolar Operation with the DAC5311

#### MICROPROCESSOR INTERFACING

#### DAC5311 to 8051 Interface

Figure 92 shows a serial interface between the DAC5311 and a typical 8051-type microcontroller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DAC5311, while RXD drives the serial data line of the part. The SYNC signal is derived from a bit programmable pin on the port. In this case, port line P3.3 is used. When data are to be transmitted to the DAC5311, P3.3 is taken low. The 8051 transmits data only in 8-bit bytes; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 remains low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 8051 outputs the serial data in a format which has the LSB first. The DAC5311 requires its data with the MSB as the first bit received. Therefore, the 8051 transmit routine must take this requirement into account, and *mirror* the data as needed.

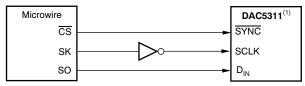


NOTE: (1) Additional pins omitted for clarity.

Figure 92. DAC5311 to 80C51/80L51 Interfaces

#### **DAC5311 to Microwire Interface**

Figure 93 shows an interface between the DAC5311 and any Microwire-compatible device. Serial data are shifted out on the falling edge of the serial clock and are clocked into the DAC5311 on the rising edge of the SK signal.



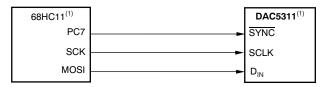
NOTE: (1) Additional pins omitted for clarity.

Figure 93. DAC5311 to Microwire Interface

28

#### DAC5311 to 68HC11 Interface

Figure 94 shows a serial interface between the DAC5311 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC5311, while the MOSI output drives the serial data line of the DAC. The SYNC signal is derived from a port line (PC7), similar to what was done for the 8051.



NOTE: (1) Additional pins omitted for clarity.

Figure 94. DAC5311 to 68HC11 Interface

The 68HC11 should be configured so that its CPOL bit is a '0' and its CPHA bit is a '1'. This configuration causes data appearing on the MOSI output to be valid on the falling edge of SCK. When data are being transmitted to the DAC, the SYNC line is taken low (PC7). Serial data from the 68HC11 are transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data are transmitted MSB first. In order to load data to the DAC5311, PC7 is held low after the first eight bits are transferred, and a second serial write operation is performed to the DAC; PC7 is taken high at the end of this procedure.

TEXAS INSTRUMENTS

SBAS470-JUNE 2009 www.ti.com

#### **LAYOUT**

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The DAC5311 offers single-supply operation; it is often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to achieve good performance from the converter.

Because of the single ground pin of the DAC5311, all return currents, including digital and analog return currents, must flow through the GND pin. Ideally, GND is connected directly to an analog ground plane. This plane should be separate from the ground connection for the digital components until they are connected at the power entry point of the system.

The power applied to  $AV_{DD}$  should be well-regulated and low-noise. Switching power supplies and dc/dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as the internal logic switches state. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. This condition is particularly true for the DAC5311, as the power supply is also the reference voltage for the DAC.

As with the GND connection,  $AV_{DD}$  should be connected to a 5 V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. In addition, the 1  $\mu$ F to 10  $\mu$ F and 0.1  $\mu$ F bypass capacitors are strongly recommended. In some situations, additional bypassing may be required, such as a 100 $\mu$ F electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors—all designed to essentially low-pass filter the 5 V supply, removing the high-frequency noise.

#### PARAMETER DEFINITIONS

With the increased complexity of many different specifications listed in product data sheets, this section summarizes selected specifications related to digital-to-analog converters.

#### STATIC PERFORMANCE

Static performance parameters are specifications such as differential nonlinearity (DNL) or integral nonlinearity (INL). These are dc specifications and provide information on the accuracy of the DAC. They are most important in applications where the signal changes slowly and accuracy is required.

#### Resolution

Generally, the DAC resolution can be expressed in different forms. Specifications such as IEC 60748-4 recognize the numerical, analog, and relative resolution. The numerical resolution is defined as the number of digits in the chosen numbering system necessary to express the total number of steps of the transfer characteristic, where a step represents both a digital input code and the corresponding discrete analogue output value. The most commonly-used definition of resolution provided in data sheets is the numerical resolution expressed in bits.

#### Least Significant Bit (LSB)

The least significant bit (LSB) is defined as the smallest value in a binary coded system. The value of the LSB can be calculated by dividing the full-scale output voltage by  $2^n$ , where n is the resolution of the converter.

#### Most Significant Bit (MSB)

The most significant bit (MSB) is defined as the largest value in a binary coded system. The value of the MSB can be calculated by dividing the full-scale output voltage by 2. Its value is one-half of full-scale.

#### Relative Accuracy or Integral Nonlinearity (INL)

Relative accuracy or integral nonlinearity (INL) is defined as the maximum deviation between the real transfer function and a straight line passing through the endpoints of the ideal DAC transfer function. INL is measured in LSBs.

#### **Differential Nonlinearity (DNL)**

Differential nonlinearity (DNL) is defined as the maximum deviation of the real LSB step from the ideal 1 LSB step. Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. If the DNL is within ±1 LSB, the DAC is said to be monotonic.

#### **Full-Scale Error**

Full-scale error is defined as the deviation of the real full-scale output voltage from the ideal output voltage while the DAC register is loaded with the full-scale code (0xFFFF). Ideally, the output should be  $V_{DD}-1$  LSB. The full-scale error is expressed in percent of full-scale range (%FSR).

#### **Offset Error**

Offset error is defined as the difference between actual output voltage and the ideal output voltage in the linear region of the transfer function. This difference is calculated by using a straight line defined by two codes (for example, for 16-bit resolution, codes 485 and 64714). Since the offset error is defined by a straight line, it can have a negative or positive value. Offset error is measured in mV.

#### **Zero-Code Error**

Zero-code error is defined as the DAC output voltage, when all '0's are loaded into the DAC register. Zero-scale error is a measure of the difference between actual output voltage and ideal output voltage (0 V). It is expressed in mV. It is primarily caused by offsets in the output amplifier.

#### **Gain Error**

Gain error is defined as the deviation in the slope of the real DAC transfer characteristic from the ideal transfer function. Gain error is expressed as a percentage of full-scale range (%FSR).

#### **Full-Scale Error Drift**

Full-scale error drift is defined as the change in full-scale error with a change in temperature. Full-scale error drift is expressed in units of %FSR/°C.

#### Offset Error Drift

Offset error drift is defined as the change in offset error with a change in temperature. Offset error drift is expressed in  $\mu V/^{\circ}C$ .

#### **Zero-Code Error Drift**

Zero-code error drift is defined as the change in zero-code error with a change in temperature. Zero-code error drift is expressed in  $\mu V/^{\circ}C$ .

#### **Gain Temperature Coefficient**

The gain temperature coefficient is defined as the change in gain error with changes in temperature. The gain temperature coefficient is expressed in ppm of FSR/°C.

#### Power-Supply Rejection Ratio (PSRR)

Power-supply rejection ratio (PSRR) is defined as the ratio of change in output voltage to a change in supply voltage for a full-scale output of the DAC. The PSRR of a device indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is measured in decibels (dB).

#### Monotonicity

Monotonicity is defined as a slope whose sign does not change. If a DAC is monotonic, the output changes in the same direction or remains at least constant for each step increase (or decrease) in the input code.

#### **DYNAMIC PERFORMANCE**

Dynamic performance parameters are specifications such as settling time or slew rate, which are important in applications where the signal rapidly changes and/or high frequency signals are present.

#### **Slew Rate**

The output slew rate (SR) of an amplifier or other electronic circuit is defined as the maximum rate of change of the output voltage for all possible input signals.

$$SR = \max\left[\left|\frac{\Delta V_{OUT}(t)}{\Delta t}\right|\right]$$
(3)

Where  $\Delta V_{OUT}(t)$  is the output produced by the amplifier as a function of time t.

#### **Output Voltage Settling Time**

Settling time is the total time (including slew time) for the DAC output to settle within an error band around its final value after a change in input. Settling times are specified to within ±0.003% (or whatever value is specified) of full-scale range (FSR).

#### Code Change/Digital-to-Analog Glitch Energy

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nanovolts-second (nV-s), and is measured when the digital input code is changed by 1 LSB at the major carry transition.

32



#### **Digital Feed Through**

Digital feed through is defined as impulse seen at the output of the DAC from the digital inputs of the DAC. It is measured when the DAC output is not updated. It is specified in nV-s, and measured with a full-scale code change on the data bus; that is, from all '0's to all '1's and vice versa.

#### **Channel-to-Channel DC Crosstalk**

Channel-to-channel dc crosstalk is defined as the dc change in the output level of one DAC channel in response to a change in the output of another DAC channel. It is measured with a full-scale output change on one DAC channel while monitoring another DAC channel remains at midscale. It is expressed in LSB.

#### **Channel-to-Channel AC Crosstalk**

AC crosstalk in a multi-channel DAC is defined as the amount of ac interference experienced on the output of a channel at a frequency (f) (and its harmonics), when the output of an adjacent channel changes its value at the rate of frequency (f). It is measured with one channel output oscillating with a sine wave of 1-kHz frequency, while monitoring the amplitude of 1-kHz harmonics on an adjacent DAC channel output (kept at zero scale). It is expressed in dB.

#### Signal-to-Noise Ratio (SNR)

Signal-to-noise ratio (SNR) is defined as the ratio of the root mean-squared (RMS) value of the output signal divided by the RMS values of the sum of all other spectral components below one-half the output frequency, not including harmonics or dc. SNR is measured in dB.

#### **Total Harmonic Distortion (THD)**

Total harmonic distortion + noise is defined as the ratio of the RMS values of the harmonics and noise to the value of the fundamental frequency. It is expressed in a percentage of the fundamental frequency amplitude at sampling rate  $f_S$ .

#### Spurious-Free Dynamic Range (SFDR)

Spurious-free dynamic range (SFDR) is the usable dynamic range of a DAC before spurious noise interferes or distorts the fundamental signal. SFDR is the measure of the difference in amplitude between the fundamental and the largest harmonically or non-harmonically related spur from dc to the full Nyquist bandwidth (half the DAC sampling rate, or f<sub>S</sub>/2). A spur is any frequency bin on a spectrum analyzer, or from a Fourier transform, of the analog output of the DAC. SFDR is specified in decibels relative to the carrier (dBc).

#### Signal-to-Noise Plus Distortion (SINAD)

SINAD includes all the harmonic and outstanding spurious components in the definition of output noise power in addition to quantizing any internal random noise power. SINAD is expressed in dB at a specified input frequency and sampling rate, f<sub>S</sub>.

#### **DAC Output Noise Density**

Output noise density is defined as internally-generated random noise. Random noise is characterized as a spectral density  $(nV/\sqrt{Hz})$ . It is measured by loading the DAC to midscale and measuring noise at the output.

#### **DAC Output Noise**

DAC output noise is defined as any voltage deviation of DAC output from the desired value (within a particular frequency band). It is measured with a DAC channel kept at midscale while filtering the output voltage within a band of 0.1 Hz to 10 Hz and measuring its amplitude peaks. It is expressed in terms of peak-to-peak voltage  $(V_{DD})$ .

## Full-Scale Range (FSR)

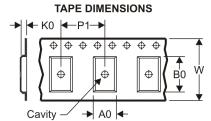
Full-scale range (FSR) is the difference between the maximum and minimum analog output values that the DAC is specified to provide; typically, the maximum and minimum values are also specified. For an n-bit DAC, these values are usually given as the values matching with code 0 and  $2^n - 1$ .

**PACKAGE MATERIALS INFORMATION** 

www.ti.com 19-Aug-2010

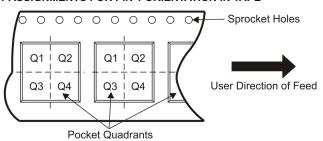
## TAPE AND REEL INFORMATION





	A0	Dimension designed to accommodate the component width
		Dimension designed to accommodate the component length
	K0	Dimension designed to accommodate the component thickness
	W	Overall width of the carrier tape
Γ	P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC5311IDCKRQ1	SC70	DCK	6	3000	177.8	9.7	2.3	2.52	1.2	4.0	8.0	Q3

www.ti.com 19-Aug-2010



#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC5311IDCKRQ1	SC70	DCK	6	3000	184.0	184.0	50.0

## DCK (R-PDSO-G6)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AB.



## DCK (R-PDSO-G6)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



#### IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
RF/IF and ZigBee® Solutions	www.ti.com/lprf		

**TI E2E Community Home Page** 

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2011, Texas Instruments Incorporated

e2e.ti.com