

DIFFERENTIAL VIDEO AMPLIFIER

FEATURES

- Adjustable Gain to 400 (Typ)
- No Frequency Compensation Required
- Low Noise . . . 3-mV V_n (Typ)

DESCRIPTION

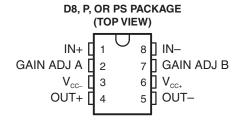
This device is a monolithic two-stage video amplifier with differential inputs and differential outputs. It features internal series-shunt feedback that provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

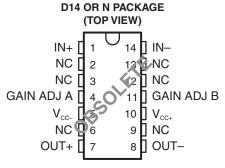
The differential gain is typically 400 when the gain adjust pins are connected together, or amplification may be adjusted for near 0 to 400 by the use of a single external resistor connected between the gain adjustment pins A and B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disk-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general-purpose video and pulse amplifiers.

The device achieves low equivalent noise voltage through special processing and a new circuit layout incorporating input transistors with low base resistance.

The TL592B is characterized for operation from 0°C to 70°C.

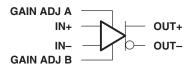




NC - No internal connection

Note: D8 and D14 are the codes to differentiate the 8-pin and 14-pin versions, respectively.

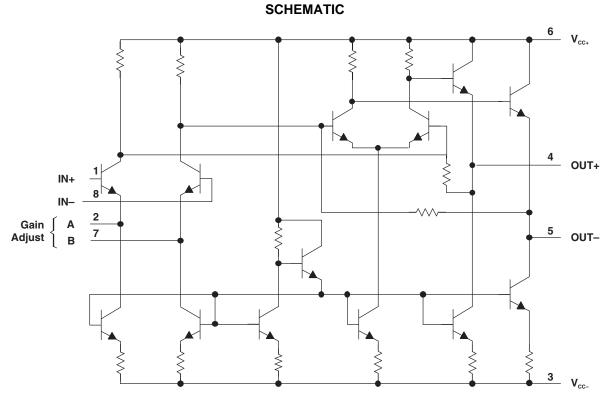
SYMBOL





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NOTE: Pin numbers shown are for D, P, and PS packages.

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

V _{CC+}	Positive supply voltage	8 V
V _{CC} -	Negative supply voltage	-8 V
V_{DI}	Differential input voltage	±5 V
VI	Voltage range, any input	V _{CC+} to V _{CC-}
Io	Output current	10 mA
P _D	Continuous total power dissipation	See Dissipation Rating Table
T _A	Operating free-air temperature range	0°C to 70°C
T _{stg}	Storage temperature range	−65°C to 150°C
T _{lead}	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR	DERATE ABOVE T _A	T _A = 70°C POWER RATING
D8	530 mW	5.8 mW/°C	59	464 mW
D14	530 mW	N/A	N/A	530 mW
N	530 mW	N/A	N/A	530 mW
Р	530 mW	N/A	N/A	530 mW
PS	530 mW	N/A	N/A	530 mW

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⁽²⁾ All voltage values except differential input voltages are with respect to the midpoint between V_{CC+} and V_{CC-}



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V _{CC+}	Positive supply voltage	3	6	8	V
V _{CC} -	Negative supply voltage	-3	-6	8–	V
T _A	Operating free-air temperature	0		70	°C

ELECTRICAL CHARACTERISTICS

at specified free-air temperature, $V_{CC\pm}$ = ±6 V, R_L = 2 k Ω (unless otherwise noted)

	PARAMETER	TEST FIGURE	TEST CO	NDITIONS ⁽¹⁾	T _A	MIN	TYP	MAX	UNIT
				D 0	25°C	300	400	500	
A_{VD}	Large-signal differential voltage amplification	1	$V_{OPP} = 3 V$, $R_1 = 2 k\Omega$	$R_{AB} = 0$	0°C to 70°C	250		600	V/V
	voltage amplification		11 - 2 1132	$R_{AB} = 1 k\Omega$	25°C		13		ı
BW	Bandwidth (-3 dB)	2	$V_{OPP} = 1 \text{ V, } R_{AB}$	₃ = 0	25°C		50		MHz
	Lamest affact accommod				25°C		0.4	5	
I _{IO}	Input offset current				0°C to 70°C			6	μΑ
	Land bio a summed				25°C		9	30	
I _{IB}	Input bias current				0°C to 70°C			40	μΑ
	Common-mode input	0			25°C	±1			
V_{ICR}	voltage range	3			0°C to 70°C	±1			V
V _{oc}	Common-mode output voltage	1	R _L = ∞		25°C	2.4	2.9	3.4	V
.,	0 "						0.35	0.75	.,
V_{OO}	Output offset voltage	1	$V_{ID} = 0$, $R_{AB} = \infty$, $R_L = \infty$		0°C to 70°C			1.5	V
.,	Peak-to-peak output		$R_L = 2 k\Omega, R_{AB} = 0$		25°C	3	4		.,
V_{OPP}	voltage swing	1			0°C to 70°C	2.8			V
_	Land and later and		V _{OD} = 1 V, R _{AB} = 0		25°C		4		
r _i	Input resistance				0°C to 70°C		3.6		kΩ
r _o	Output resistance				0°C to 70°C			30	Ω
C _i	Input capacitance				0°C to 70°C		5		pF
				f = 100 kHz	0500	60	86		- dB
01400	Common-mode rejection	•	$V_{IC} = \pm 1 V$, $R_{AB} = 0$	f = 5 MHz	25°C		60		
CMRR	ratio	3		f = 100 kHz	000 1- 7000	50			
				f = 5 MHz	0°C to 70°C		60		ı
L	Supply voltage rejection		$\Delta V_{CC+} = \pm 0.5 \text{ V}$	$\Delta V_{CC-} = \pm 0.5 \text{ V},$	25°C	50	70		ī
k _{SVR}	ratio $(\Delta V_{CC}/\Delta V_{IO})$	4	$R_{AB} = 0$. 00-	0°C to 70°C	50			dB
V _n	Broadband equivalent input noise voltage	4	BW = 1 kHz to 10 MHz		25°C		3		μV
t _{pd}	Propagation delay time	2	$\Delta V_O = 1 V$		25°C		7.5		ns
t _r	Rise time	2	$\Delta V_O = 1 V$		25°C		10.5		ns
I _{sink(max)}	Maximum output sink current		V _{ID} = 1 V, V _O =	3 V		3	4		mA
	Cumply ourse at		No lood No star	a a l	25°C		18	24	^
ICC	Supply current		No load, No sign	naı	0°C to 70°C			27	mA

⁽¹⁾ R_{AB} is the gain-adjustment resistor connected between gain-adjust pins A and B. If not specified for a particular parameter, its value is irrelevant to that parameter.

Product Folder Link(s): TL592B



PARAMETER MEASUREMENT INFORMATION

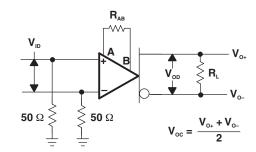
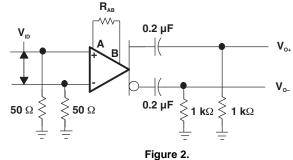


Figure 1.



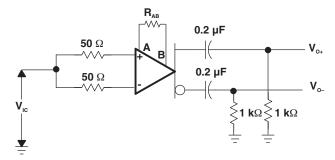


Figure 3.

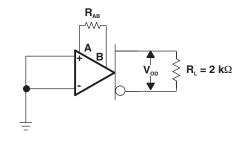


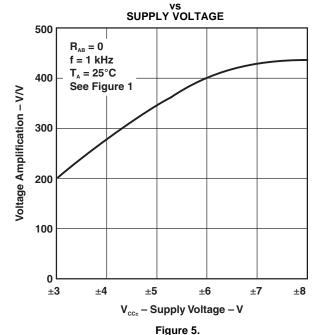
Figure 4.

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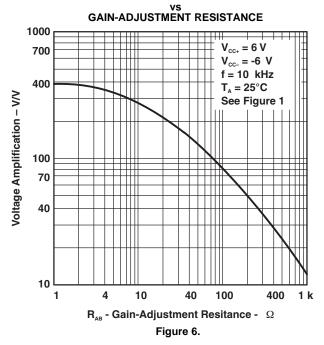


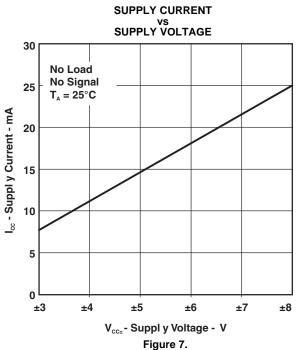
TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION



LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION









i.com 17-Mar-2008

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TL592B-8D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL592B-8DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL592B-8DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL592B-8DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL592B-8DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL592B-8DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL592BI-8D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL592BN	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
TL592BP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL592BPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL592BPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL592BPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL592BPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL592B-8DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL592BPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL592B-8DR	SOIC	D	8	2500	340.5	338.1	20.6
TL592BPSR	SO	PS	8	2000	346.0	346.0	33.0

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.





NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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