



,QUAD, 10-Bit, LOW-POWER, VOLTAGE OUTPUT, I^C INTERFACE DIGITAL-TO-ANALOG CONVERTER

FEATURES

- Micropower Operation: 500 µA at 3 V V_{DD}
- Fast Update Rate: 188 kSPS
- Power-On Reset to Zero
- 2.7-V to 5.5-V Analog Power Supply
- **10-Bit Monotonic**
- I²C[™] Interface up to 3.4 Mbps
- **Data Transmit Capability**
- **Rail-to-Rail Operation Output Buffer Amplifier**
- **Double-Buffered Input Register**
- Address Support for up to Sixteen DAC6573s
- Synchronous Update for up to 64 Channels
- Voltage Translators for all Digital Inputs
- Operation From -40°C to 105°C
- Small 16 Lead TSSOP Package

APPLICATIONS

- Process Control
- **Data Acquisition Systems**
- **Closed-Loop Servo Control**
- PC Peripherals
- **Portable Instrumentation**

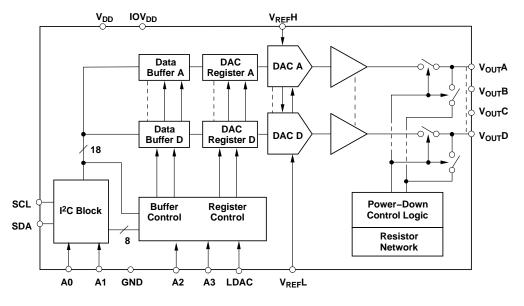
DESCRIPTION

The DAC6573 is a low-power, quad channel, 10-Bit buffered voltage output DAC. Its on-chip precision output amplifier allows rail-to-rail output swing. The DAC6573 utilizes an I²C compatible two wire serial interface supporting high-speed interface mode with address support of up to sixteen DAC6573s for a total of 64 channels on the bus.

The DAC6573 requires an external reference voltage to set the output range of the DAC. The DAC6573 incorporates a power-on-reset circuit that ensures that the DAC output powers up at zero volts and remains there until a valid write takes place in the device. The DAC6573 contains a power-down feature, accessed via the internal control register, that reduces the current consumption of the device to 200 nA at 5 V.

The low power consumption of this part in normal operation makes it ideally suited to portable battery operated equipment. The power consumption is less than 3 mW at V_{DD}=5 V reducing to 1 μ W in power-down mode.

The DAC6573 is available in a 16-lead TSSOP package.



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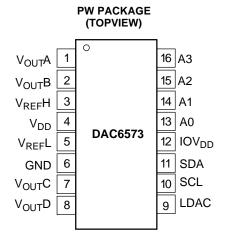


This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUC	T PACKAGE	PACKAGE DRAWING NUMBER	SPECIFICATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
DAC657	3 16-TSSOP	PW	–40°C TO +105°C	D6573I	DAC6573IPW	90 Piece Tube
					DAC6573IPWR	2000 Piece Tape and Reel



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	V _{OUT} A	Analog output voltage from DAC A
2	V _{OUT} B	Analog output voltage from DAC B
3	$V_{REF}H$	Positive reference voltage input
4	V_{DD}	Analog voltage supply input
5	$V_{REF}L$	Negative reference voltage input
6	GND	Ground reference point for all circuitry on the part
7	V _{OUT} C	Analog output voltage from DAC C
8	V _{OUT} D	Analog output voltage from DAC D
9	LDAC	H/W synchronous V _{OUT} update
10	SCL	Serial clock input
11	SDA	Serial data input
12	IOV_{DD}	I/O voltage supply input
13	A0	Device address select - I ² C
14	A1	Device address select - I ² C
15	A2	Device address select - Extended
16	A3	Device address select - Extended

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

V _{DD} to GND		–0.3 V to +6 V
Digital input voltage to GND		–0.3 V to V _{DD} + 0.3 V
V _{OUT} to GND		–0.3 V to V _{DD} + 0.3 V
Operating temperature range		-40°C to +105°C
Storage temperature range		-65°C to +150°C
Junction temperature range (T	ן max)	+150°C
Power dissipation	Thermal impedance (_{ROJA})	161°C/W
	Thermal impedance (R _{OJC})	29°C/W
Lead temperature, soldering	Vapor phase (60s)	215°C
	Infrared (15s)	220°C

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

 V_{DD} = 2.7 V to 5.5 V, R_L = 2 k Ω to GND; C_L = 200 pF to GND; all specifications -40°C to +105°C, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE ⁽¹⁾⁽²⁾					
Resolution		10			Bits
Relative accuracy			±0.5	±2	LSB
Differential nonlinearity	Specified monotonic by design		±0.1	± 0.5	LSB
Zero-scale error			5	20	mV
Full-scale error			-0.15	±1.0	% of FSR
Gain error				±1.0	% of FSR
Zero code error drift			±7		μV/°C
Gain temperature coefficient			± 3		ppm of FSR/°0
OUTPUT CHARACTERISTICS ⁽³⁾					
Output voltage range		0		V _{REF} H	V
Output voltage settling time (full scale)	R _L = ∞; 0 pF < C _L < 200 pF		7	9	μs
	$R_L = \infty$; $C_L = 500 \text{ pF}$		12		μs
Slew rate			1		V/µs
dc crosstalk (channel-to-channel)			0.01		LSB
ac crosstalk (channel-to-channel)	1 kHz Sine Wave		-100		dB
Capacitive load stability	R _L = ∞		470		pF
	$R_{L}=2 k\Omega$		1000		pF
Digital-to-analog glitch impulse	1 LSB change around major carry		12		nV-s
Digital feedthrough			0.3		nV-s
dc output impedance			1		Ω
Short-circuit current	V _{DD} = 5 V		50		mA
	V _{DD} = 3 V		20		mA
Power-up time	Coming out of power-down mode, V _{DD} = +5 V		2.5		μs
	Coming out of power-down mode, V _{DD} = +3 V		5		μs
REFERENCE INPUT					
V _{REF} H Input range		0		V _{DD}	V
V _{REF} L Input range	V _{REF} L <v<sub>REFH</v<sub>	0	GND	V _{DD} /2	V
Reference input impedance			25		kΩ
Reference current	$V_{REF} = V_{DD} = +5 V$		185	260	μA
	V _{REF} =V _{DD} = +3 V		122	200	-
LOGIC INPUTS ⁽³⁾	1				I
Input current				±1	μA
V _{INL} , Input low voltage				0.3xIOV _{DD}	V
V _{IN H} , Input high voltage		0.7xIOV _{DD}			V
Pin Capacitance		20		3	pF
POWER REQUIREMENTS	<u> </u>	1			1*
V _{DD} , IOV _{DD}		2.7		5.5	V
I_{DD} (normal operation), including reference current	Excluding load current				
I_{DD} @ V_{DD} =+3.6V to +5.5V	V_{IH} = IOV _{DD} and V_{IL} =GND		600	900	μA
I_{DD} @ V_{DD} =+2.7V to +3.6V	V_{IH} = IOV _{DD} and V_{IL} =GND		500	750	μA
I _{DD} (all power-down modes)					1

Linearity tested using a reduced code range of 12 to 1012; output unloaded. $V_{REF}H = V_{DD} - 0.1$, $V_{REF}L = GND$ Specified by design and characterization, not production tested. (1)

(2) (3)

ELECTRICAL CHARACTERISTICS (continued)

 V_{DD} = 2.7 V to 5.5 V, R_L = 2 k Ω to GND; C_L = 200 pF to GND; all specifications -40°C to +105°C, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN TYP		MAX	UNITS
I _{DD} @ V _{DD} =+3.6V to +5.5V	V_{IH} = IOV _{DD} and V_{IL} =GND		0.2	1	μA
I _{DD} @ V _{DD} =+2.7V to +3.6V	V _{IH} = IOV _{DD} and V _{IL} =GND		0.05	1	μA
POWER EFFICIENCY					
I _{OUT} /I _{DD}	I _{LOAD} = 2 mA, V _{DD} = +5 V	93%			
TEMPERATURE RANGE				<u>.</u>	
Specified performance		-40		+105	°C

TIMING CHARACTERISTICS

 V_{DD} = 2.7 V to 5.5 V, R_L = 2 k Ω to GND; all specifications -40°C to +105°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	ΤΥΡ	MAX	UNITS
		Standard mode			100	kHz
4		Fast mode			400	kHz
f _{SCL}	SCL clock frequency	High-Speed mode, $C_B = 100 \text{ pF} \text{ max}$			3.4	MHz
		High-speed mode, C _B = 400 pF max			1.7	MHz
	Bus free time between a	Standard mode	4.7			μs
t _{BUF}	STOP and START condition	Fast mode	1.3			μs
		Standard mode	4.0			μs
t _{HD} ; t _{STA}	Hold time (repeated) START condition	Fast mode	600			ns
	condition	High-speed mode	160			ns
		Standard mode	4.7			μs
	LOW period of the CCL shack	Fast mode	1.3			μs
t _{LOW}	LOW period of the SCL clock	High-speed mode, C _B = 100 pF max	160			ns
		High-speed mode, C _B = 400 pF max	320			ns
		Standard mode	4.0			μs
		Fast mode	600			ns
t _{HIGH}	HIGH period of the SCL clock	High-Speed Mode, C _B = 100 pF max	60			ns
		High-speed mode, C _B = 400 pF max	120			ns
		Standard mode	4.7			μs
t _{SU} ; t _{STA}	Setup time for a repeated START condition	Fast mode	600			ns
		High-speed mode	160			ns
		Standard mode	250			ns
t _{SU} ; t _{DAT}	Data setup time	Fast mode	100			ns
		High-speed mode	10			ns
		Standard mode	0		3.45	μs
	Data hald for a	Fast mode	0		0.9	μs
t _{HD} ; t _{DAT}	Data hold time	High-speed mode, C _B = 100 pF max	0		70	ns
		High-speed mode, $C_B = 400 \text{ pF} \text{ max}$	0		150	ns
		Standard mode			1000	ns
	Diag time of CCL signal	Fast mode	20 + 0.1C _B		300	ns
t _{RCL}	Rise time of SCL signal	High-speed mode, C _B = 100 pF max	10		40	ns
		High-speed mode, C _B = 400 pF max	20		80	ns
	Disa time of CCL signal after	Standard mode			1000	ns
	Rise time of SCL signal after – a repeated START condition	Fast mode	20 + 0.1C _B		300	ns
t _{RCL1}	and after an acknowledge	High-speed mode, C _B = 100 pF max	10		80	ns
	BIT	High-speed mode, $C_B = 400 \text{ pF}$ max	20		160	ns

TIMING CHARACTERISTICS (continued)

 V_{DD} = 2.7 V to 5.5 V, R_L = 2 k Ω to GND; all specifications -40°C to +105°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		Standard mode			300	ns
	Fall time of SCI signal	Fast mode	20 + 0.1C _B		300	ns
t _{FCL}	Fall time of SCL signal	High-speed mode, C _B = 100 pF max	10		40	ns
		High-speed mode, C _B = 400 pF max	20		80	ns
		Standard mode			1000	ns
		Fast mode	20 + 0.1C _B		300	ns
t _{RDA}	Rise time of SDA signal	High-speed mode, C _B = 100 pF max	10		80	ns
		High-speed mode, $C_B = 400 \text{ pF} \text{ max}$	20		160	ns
		Standard mode			300	ns
	Fall time of SDA signal	Fast mode	20 + 0.1C _B		300	ns
t _{FDA}	Fall time of SDA signal	High-speed mode, C _B = 100 pF max	10		80	ns
		High-speed mode, $C_B = 400 \text{ pF} \text{ max}$	20		160	ns
		Standard mode	4.0			μs
t _{SU} ; t _{STO}	Setup time for STOP condition	Fast mode	600			ns
		High-speed mode	160			ns
C _B	Capacitive load for SDA and SCL				400	pF
	Pulse width of spike	Fast mode			50	ns
t _{SP}	suppressed	High-speed mode			10	ns
	Noise margin at the HIGH	Standard mode				
V _{NH}	level for each connected device (including	Fast mode	0.2 V _{DD}			V
	hysteresis)	High-speed mode	1			
	Noise margin at the LOW	Standard mode				
V _{NL}	level for each connected device (including	Fast mode	0.1 V _{DD}			V
	hysteresis)	High-speed mode	1			



TYPICAL CHARACTERISTICS

At $T_A = +25^{\circ}C$, unless otherwise noted.

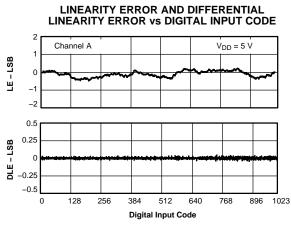
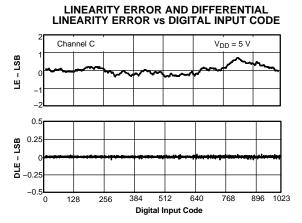


Figure 1.





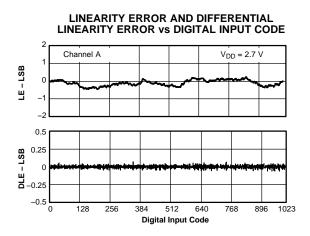


Figure 5.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

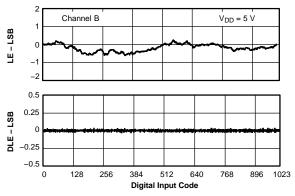


Figure 2.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

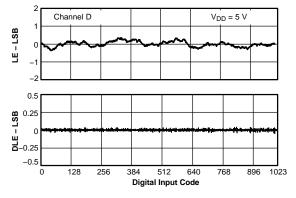


Figure 4.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

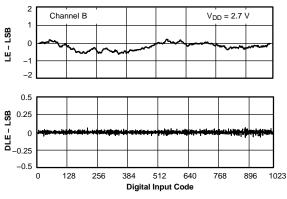


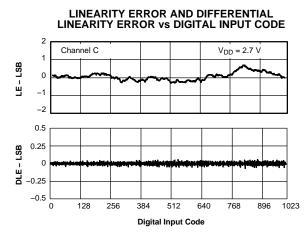
Figure 6.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^{\circ}C$, unless otherwise noted.

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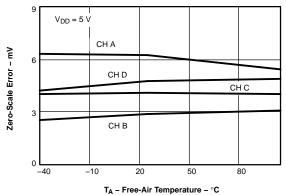


Figure 9.

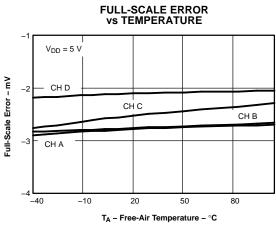


Figure 11.

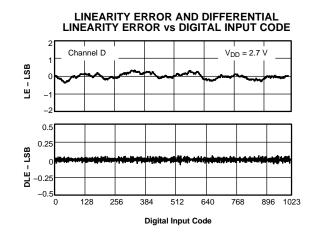


Figure 8.

ZERO-SCALE ERROR vs TEMPERATURE

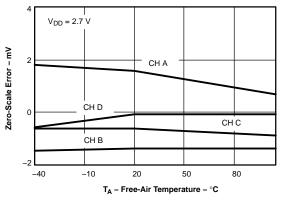


Figure 10.

FULL-SCALE ERROR vs TEMPERATURE

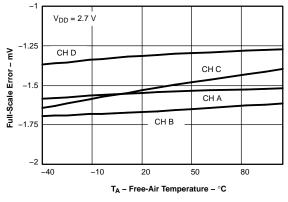


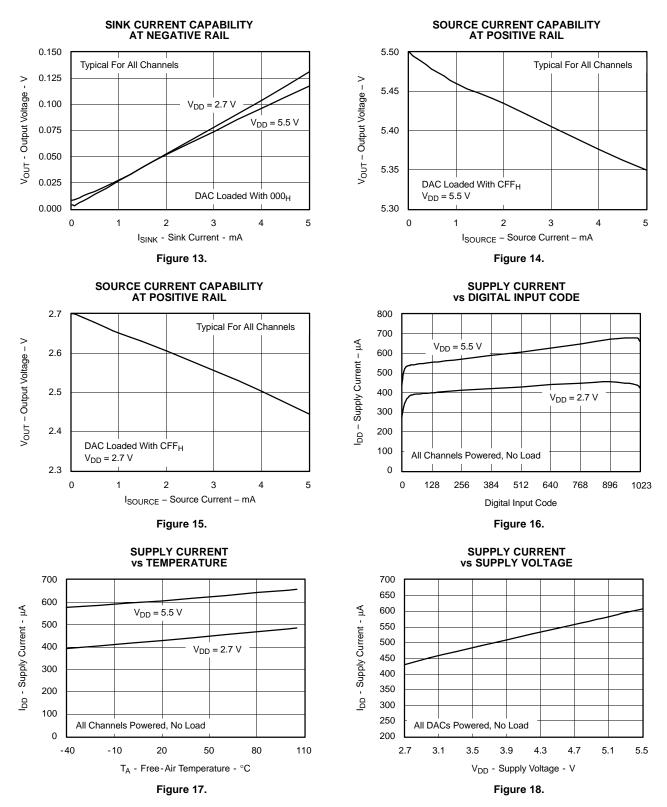
Figure 12.

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TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^{\circ}C$, unless otherwise noted.

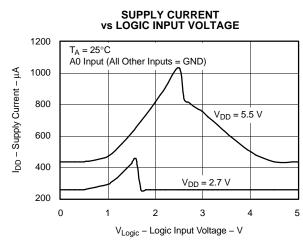


TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^{\circ}C$, unless otherwise noted.

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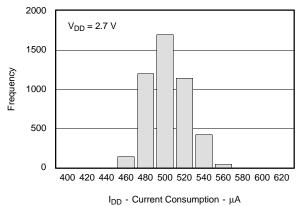
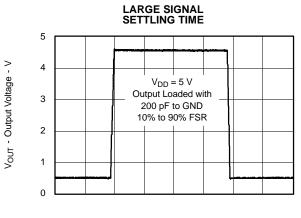
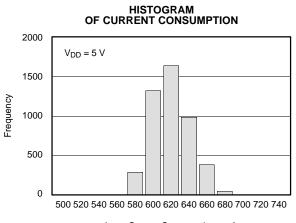


Figure 21.





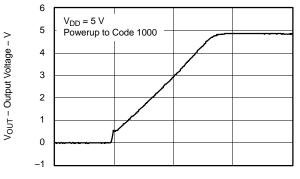




 I_{DD} - Current Consumption - μA



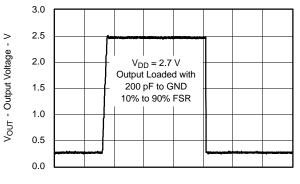




Time (2 µs/div)

Figure 22.

LARGE SIGNAL SETTLING TIME



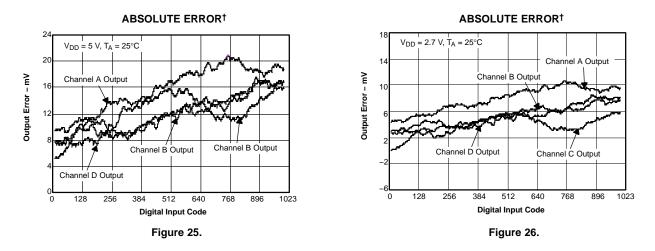
Time (25 µs/div)

Figure 24.



TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^{\circ}C$, unless otherwise noted.



[†]Absolute error is the deviation from ideal DAC characteristics. It includes affects of offset, gain, and integral linearity.

THEORY OF OPERATION

D/A SECTION

The architecture of the DAC6573 consists of a string DAC followed by an output buffer amplifier. Figure 27 shows a generalized block diagram of the DAC architecture.

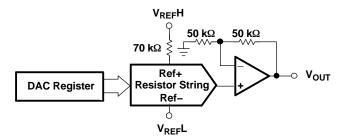


Figure 27. R-String DAC Architecture

The input coding to the DAC6573 is unsigned binary, which gives the ideal output voltage as:

$$V_{OUT} = 2 \times V_{REF}L + (V_{REF}H - V_{REF}L) \times \frac{D}{1024}$$

Where D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 1023.

RESISTOR STRING

The resistor string section is shown in Figure 28. It is basically a divide-by-2 resistor, followed by a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. Because the architecture consists of a string of resistors, it is specified monotonic.

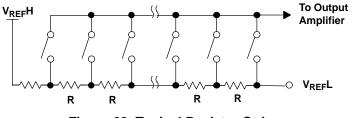


Figure 28. Typical Resistor String

Output Amplifier

The output buffer is a gain-of-2 noninverting amplifier, capable of generating rail-to-rail voltages on its output, which gives an output range of 0V to V_{DD} . It is capable of driving a load of 2 k Ω in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical curves. The slew rate is 1 V/µs with a half-scale settling time of 7 µs with the output unloaded.

I²C Interface

I²C is a 2-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I²C-compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives and/or transmits data on the bus under control of the master device.



THEORY OF OPERATION (continued)

The DAC6573 works as a slave and supports the following data transfer modes, as defined in the I²C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps), and high-speed mode (3.4 Mbps). The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from the F/S-mode, and it is referred to as H/S-mode. The DAC6573 supports 7-bit addressing; 10-bit addressing and general call address are *not* supported.

F/S-Mode Protocol

- The *master* initiates data transfer by generating a *start condition*. The *start condition* is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 29. All I²C-compatible devices recognize a *start condition*.
- The master then generates the SCL pulses, and transmits the 7-bit address and the *read/write direction bit* R/W on the SDA line. During all transmissions, the master ensures that data is *valid*. A *valid data* condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 30). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge* (see Figure 31) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.
- The master generates further SCL cycles to either *transmit* data to the slave (R/W bit 1) or *receive* data from the slave (R/W bit 0). In either case, the *receiver* must acknowledge the data sent by the *transmitter*. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-Bit data and 1-bit acknowledge can continue as long as necessary.
- To signal the end of the data transfer, the master generates a *stop condition* by pulling the SDA line from low to high while the SCL line is high (see Figure 29). This releases the bus and stops the communication link with the addressed slave. All I²C-compatible devices must recognize the stop condition. Upon the receipt of a *stop condition*, all devices know that the bus is released, and they wait for a *start condition* followed by a matching address.

H/S-Mode Protocol

- When the bus is idle, both SDA and SCL lines are pulled high by the pullup devices.
- The master generates a start condition followed by a valid serial byte containing H/S master code 00001XXX. This transmission is made in F/S mode at no more than 400 Kbps. No device is allowed to acknowledge the H/S master code, but all devices must recognize it and switch their internal setting to support 3.4 Mbps operation.
- The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the H/S-mode and switches all the internal settings of the slave devices to support the F/S-mode. Instead of using a stop condition, repeated start conditions must be used to secure the bus in H/S-mode.

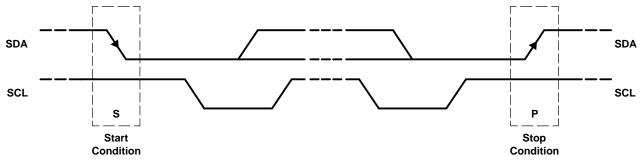


Figure 29. START and STOP Conditions

THEORY OF OPERATION (continued)

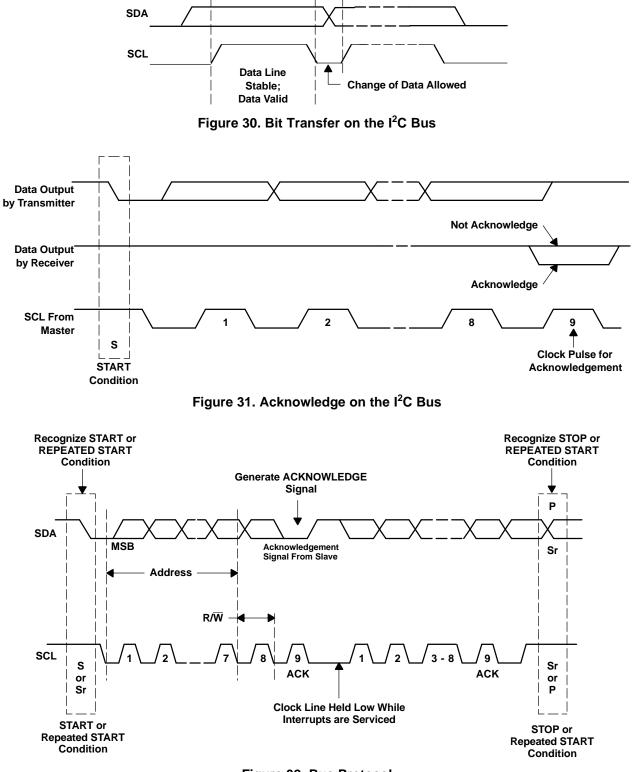


Figure 32. Bus Protocol

DAC6573 I²C Update Sequence

The DAC6573 requires a start condition, a valid I²C address, a control byte, an MSB byte, and an LSB byte for a single update. After the receipt of each byte, DAC6573 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the DAC6573. The control byte sets the operational mode of the selected DAC6573. Once the operational mode is selected by the control byte, DAC6573 expects an MSB byte followed by an LSB byte for data update to occur. DAC6573 performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

TRUMENTS

The control byte needs not to be resent until a change in operational mode is required. The bits of the control byte continuously determine the type of update performed. Thus, for the first update, DAC6573 requires a start condition, a valid I²C address, a control byte, an MSB byte and an LSB byte. For all consecutive updates, DAC6573 needs an MSB byte, and an LSB byte as long as the control command remains the same.

Using the I²C high-speed mode (f_{scl} = 3.4 MHz), the clock running at 3.4 MHz, each 10-Bit DAC update other than the first update can be done within 18 clock cycles (MSB byte, acknowledge signal, LSB byte, acknowledge signal), at 188.88 kSPS. Using the fast mode (f_{scl} = 400 kHz), clock running at 400 kHz, maximum DAC update rate is limited to 22.22 kSPS. Once a stop condition is received, DAC6573 releases the I²C bus and awaits a new start condition.

Address Byte

MSB							LSB
1	0	0	1	1	A1	A0	R/W

The address byte is the first byte received following the START condition from the master device. The first five bits (MSBs) of the address are factory preset to 10011. The next two bits of the address are the device select bits A1 and A0. The A1, A0 address inputs can be connected to V_{DD} or digital GND, or can be actively driven by TTL/CMOS logic levels. The device address is set by the state of these pins during the power-up sequence of the DAC6573. Up to 16 devices (DAC6573) can still be connected to the same I²C-bus.

Broadcast Address Byte

MSB							LSB
1	0	0	1	0	0	0	0

Broadcast addressing is also supported by DAC6573. Broadcast addressing can be used for synchronously updating or powering down multiple DAC6573 devices. DAC6573 is designed to work with other members of the DAC857x, DAC757x, and DAC557x families to support multichannel synchronous update. Using the broadcast address, DAC6573 responds regardless of the states of the address pins. Broadcast is supported only in write mode (master writes to DAC6573).

Control Byte

MSB							LSB
A3	A2	L1	L0	Х	Sel1	Sel0	PD0

Table 1. Control Register Bit Descriptions

Bit Name	Bit Number/D	Description							
A3	Extended add	ress bit	The state of these bits must match the state of pins A3 and A2 in order for a proper						
A2	Extended add	ress bit	DAC6573 data update, except in broadcast update mode.						
L1	Load1 (mode	select) bit	An used for extention the undetermede						
L2	Load0 (mode	select) bit	Are used for selecting the update mode.						
	00		a. The contents of MS-BYTE and LS-BYTE (or power down information) are stored in the sister of a selected channel. This mode does not change the DAC output of the selected						
	01	LS-BYTE (or	Update selected DAC with I ² C data. Most commonly utilized mode. The contents of MS-BYTE and LS-BYTE (or power down information) are stored in the temporary register and in the DAC register of the selected channel. This mode changes the DAC output of the selected channel with the new data.						
	10	stored in the other three c	4-channel synchronous update. The contents of MS-BYTE and LS-BYTE (or power down information) are stored in the temporary register and in the DAC register of the selected channel. Simultaneously, the other three channels get updated with previously stored data from the temporary register. This mode updates all four channels together.						
	11	regardless of	odate mode. This mode has two functions. In broadcast mode, DAC6573 responds f local address matching, and channel selection becomes irrelevant as all channels update. Intended to enable up to 64 channels simultaneous update, if used with the I ² C broadcast 01 0000).						
		If Sel1=0	All four channels are updated with the contents of their temporary register data.						
		If Sel1=1	All four channels are updated with the MS-BYTE and LS-BYTE data or powerdown.						
Sel1	Buff Sel1 Bit								
Sel0	Buff Sel0 Bit		Channel select bits						
	00	Channel A							
	01	Channel B							
	10	Channel C							
	11	Channel D							
PD0	Power Down I	Flag							
	0	Normal oper	ation						
	1	Power-down	flag (MSB7 and MSB6 indicate a power-down operation, as shown in Table 2).						

DAC6573

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					Та	able 2. Co	ontrol E	Byte						
C7	C6	C5	C4	C3	C2	C1	C0	MSB7	MSB6	MSB5				
A3	A2	Load1	Load0	Don't Care	Ch Sel 1	Ch Sel 0	PD0	MSB (PD1)	MSB-1 (PD2)	MSB-2 LSB	DESCRIPTION			
	lress ect)													
(A3 and A2 should corre- spond to the package ad- dress, set via pins A3 and A2)		0	0	Х	0	0	0		Data		Write to temporary register A (TRA) with data			
		0	0	х	0	1	0		Data		Write to temporary register B (TRB) with data			
,	_)	0	0	х	1	0	0		Data		Write to temporary register C (TRC) with data			
		0	0	х	1	1	0	Data						Write to temporary register D (TRD) with data
		0	0	х	(00, 01, 10), or 11)	1	See T	able 8	0	Write to TRx (selected by C2 & C1 w/Powerdown Command			
		0	1	х	(00, 01, 10), or 11)	0		Data		Write to TRx (selected by C2 & C1 and load DACx w/data			
		0	1	х	(00, 01, 10, or 11) (00, 01, 10, or 11)		1	See T	able 8	0	Power-down DACx (selected by C2 and C1)			
		1	0	х			0		Data		Write to TRx (selected by C2 & C1 w/ data and load all DACs			
		1	0	х	(00, 01, 10), or 11)	1	See T	able 8	0	Power-down DACx (selected by C2 and C1) & load all DACs			
		Br	oadcast Mo	odes (con	trols up to	4 devices o	n a sing	le serial b	us)					
х	х	1	1	х	0	х	х	x			Update all DACs, all devices with previously stored TRx data			
х	х	1	1	х	1	х	0	Data			Update all DACs, all devices with MSB[7:0] and LSB[7:0] data			
х	х	1	1	х	1	х	1	see T	able 8	0	Power-down all DACs, all devices			

Most Significant Byte

Most significant byte MSB[7:0] consists of eight most significant bits of 10-bit unsigned binary D/A conversion data. If C0=1, MSB[7], MSB[6] indicate a power-down operation as shown in Table 8.

Least Significant Byte

Least significant byte LSB[7:0] consists of the 2 least significant bits of the 10-Bit unsigned binary D/A conversion data, followed by 6 *don't care* bits. DAC6573 updates at the falling edge of the acknowledge signal that follows the LSB[0] bit.

Default Readback Condition

If the user initiates a readback of a specified channel without first writing data to that specified channel, the default readback is all zeros, since the readback register is initialized to 0 during the power on reset phase.

LDAC Functionality

Depending on the control byte, DACs are synchronously updated on the falling edge of the acknowledge signal that follows LS byte. The LDAC pin is required only when an external timing signal is used to update all the channels of the DAC asynchronously. LDAC is a positive edge triggered asynchronous input that allows four DAC output voltages to be updated simultaneously with temporary register data. The LDAC trigger should only be used after the buffer's temporary registers are properly updated through software.

DAC6573 Registers

REGISTER	DESCRIPTION
CTRL[7:0]	Stores 8-Bit wide control byte sent by the master
MSB[7:0]	Stores the 8 most significant bits of unsigned binary data sent by the master. Can also store 2-bit power-down data.
LSB[7:0]	Stores the 2 least significant bits of unsigned binary data sent by the master (in LSB[7] and LSB[6]).
TRA[11:0], TRB[11:0], TRC[11:0], TRD[11:0]	12-bit temporary storage registers assigned to each channel. Two MSBs store power-down information, 10 LSBs store data.
DRA[11:0], DRB[11:0], DRC[11:0], DRD[11:0]	12-bit DAC registers for each channel. Two MSBs store power-down information, 10 LSBs store DAC data. An update of this register means a DAC update with data or power-down.

Table 3. DAC6573 Architecture Register Descriptions

DAC6573 as a Slave Receiver—Standard and Fast Mode

Figure 33 shows the standard and fast mode master transmitter addressing a DAC6573 *Slave Receiver* with a 7-bit address.

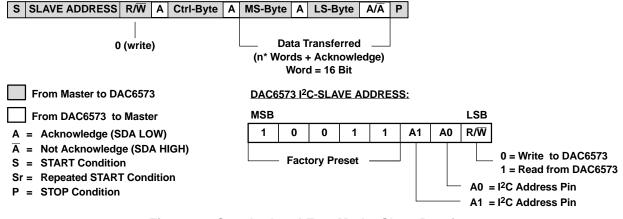


Figure 33. Standard and Fast Mode: Slave Receiver

DAC6573 as a Slave Receiver - High-Speed Mode

Figure 34 shows the high-speed mode master transmitter addressing a DAC6573 Slave Receiver with a 7-bit address.

4	— F/S	6-Mod	ə —		◀—						HS-Mode	. –							- F/S-Mode
S	HS-Ma	aster C	ode	Ā	Sr	Slav	e Adc	Iress	R/W	Α	Ctrl-Byte	Α	MS-By	yte /	۱L:	S-Byte	A/A	Ρ	
<u>HS-</u>	Mode M	laster	Code:					0	(writ	e)			(n* \	Words	5 + A	nsferree cknowl 16 Bit			Mode Continu
MSE	3							LSB											
0	0	0	0	1		Х	Х	R/W]		Contro	Byt	<u>e:</u>						
									1		MSB							LSB	
MS-	Byte:										A3	A2	L1	L0	Х	Sel1	Sel2	PD0]
MSE	3							LSB			A3 =		tended						
D9	D8	D7	D6	D	5	D4	D3	D2]				tended						
LS-	Byte:								1		L0 =	= Lo	oad1 (M oad0 (M uff Sel1	ode S	elec	t) Bit	Bit		
MSE	3							LSB					uff Sel0	•					
D1	D0	X	X)	(X	Х	X]				ower Do	•					
D9 -	D0 = D	ata Bi	ts					•	•		X = D	on't	Care						

X = Don't Care

Figure 34. High-Speed Mode: Slave Receiver

Master Transmitter Writing to a Slave Receiver (DAC6573) in Standard/Fast Modes

All write access sequences begin with the device address (with R/W = 0) followed by the control byte. This control byte specifies the operation mode of DAC6573 and determines which channel of DAC6573 is being accessed in the subsequent read/write operation. The LSB of the control byte (PD0-Bit) determines whether the following data is power-down data or regular data.

With (PD0-Bit = 0) the DAC6573 expects to receive data in the following sequence HIGH-BYTE - LOW-BYTE - HIGH-BYTE - LOW-BYTE..., until a STOP Condition or REPEATED START Condition on the I²C-bus is recognized (refer to the DATA INPUT MODE section of Table 4).

With (PD0-Bit = 1) the DAC6573 expects to receive 2 bytes of power-down data (refer to the POWER DOWN MODE section of Table 4).

DATA INPUT N	IODE									
Transmitter	MSB	6	5	4	3	2	1	LSB	Comment	
Master			1		Start	1	1		Begin sequence	
Master	1	0	0	1	1	A1	A0	R/W	Write addressing (R/W=0)	
DAC6573										
Master	A3	A2	Load 1	Load 0	x	Buff Sel 1	Buff Sel 0	PD0	Control byte (PD0=0)	
DAC6573				DAC6573	Acknowle	edges				
Master	D9 D8 D7 D6 D5 D4 D3 D2						D2	Writing data word, high byte		
DAC6573				DAC6573	Acknowle	edges				
Master	D1	D0	х	х	х	х	х	х	Writing data word, low byte	
DAC6573				DAC6573	Acknowle	edges				
Master			Dat	a or Stop o	r Repeat	ed Start ⁽¹⁾			Data or done ⁽²⁾	
POWER DOWN	MODE									
Transmitter	MSB	6	5	4	3	2	1	LSB	Comment	
Master				ę	Start				Begin sequence	
Master	1	0	0	1	1	A1	A0	R/W	Write addressing (R/W=0)	
DAC6573				DAC6573	Acknowle	edges				
Master	A3	A2	Load 1	Load 0	х	Buff Sel 1	Buff Sel 0	PD0	Control byte (PD0 = 1)	
DAC6573				DAC6573	Acknowle	edges				
Master	PD1	PD2	0	0	0	0	0	0	Writing data word, high byte	
DAC6573										
Master	0 0 x x x x x x							х	Writing data word, low byte	
DAC6573	DAC6573 Acknowledges									
Master				Stop or Re	peated S	Start ⁽¹⁾			Done	

Table 4. Write Sequence in F/S Mode

(1) Use repeated START to secure bus operation and loop back to the stage of write addressing for next Write.

(2) Once DAC6573 is properly addressed and control byte is sent, HIGH–BYTE–LOW–BYTE sequences can repeat until a STOP condition or repeated START condition is received.

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Master Transmitter Writing to a Slave Receiver (DAC6573) in HS Mode

When writing data to the DAC6573 in HS-mode, the master begins to transmit what is called the *HS-Master Code* (0000 1XXX) in F/S-mode. No device is allowed to acknowledge the *HS-Master Code*, so the *HS-Master Code* is followed by a NOT acknowledge.

The master then *switches* to HS-mode and issues a *repeated start* condition, followed by the address byte (with R/W = 0) after which the DAC6573 acknowledges by pulling SDA low. This address byte is usually followed by the control byte, which is also acknowledged by the DAC6573. The LSB of the control byte (PD0-Bit) determines if the following data is *power-down data* or regular data.

With (PD0-Bit = 0) the DAC6573 expects to receive data in the following sequence HIGH-BYTE – LOW-BYTE – HIGH-BYTE – LOW-BYTE..., until a STOP condition or *repeated start* condition on the I^2 C-Bus is recognized (refer to Table 5 HS-MODE WRITE SEQUENCE - DATA).

With (PD0-Bit = 1) the DAC6573 expects to receive 2 bytes of power-down data (refer to Table 5 HS-MODE WRITE SEQUENCE - POWER DOWN).

HS MODE WR	TE SEQUI	ENCE - I	DATA						
Transmitter	MSB	6	5	4	3	2	1	LSB	Comment
Master				5	Start			1	Begin sequence
Master	0	0	0	0	1	Х	Х	Х	HS mode master code
NONE				Not acl	knowled	ge			No device may acknowledge HS mas- ter code
Master				Repea	ated star	t			
Master	1								Write addressing (R/W=0)
DAC6573				DAC6573	acknowle	edges			
Master	0	0	Load 1	PD0	Control byte (PD0=0)				
DAC6573				DAC6573	acknowle	edges			
Master	D9	D8	D7	D6	D5	D4	D3	D2	Writing data word, MSB
DAC6573				DAC6573	acknowle	edges			
Master	D1	D0	х	х	х	х	х	х	Writing data word, LSB
DAC6573									
Master			Da	ata or stop o	r repeate	ed start ⁽¹⁾			Data or done ⁽²⁾
HS MODE WR	TE SEQUI	ENCE - F	POWER DO	OWN					
Transmitter	MSB	6	5	4	3	2	1	LSB	Comment
Master				5	Start				Begin sequence
Master	0	0	0	0	1	Х	Х	Х	HS mode master code
NONE				Not acl	knowled	ge			No device may acknowledge HS mas- ter code
Master				Repea	ated star	t			
Master	1	0	0	1	1	A1	A0	R/W	Write addressing (R/W = 0)
DAC6573				DAC6573	acknowle	edges			
Master	0	0	Load 1	Load 2	0	Buff Sel 1	Buff Sel 0	PD0	Control byte (PD0=1)
DAC6573	DAC6573 acknowledges								
Master	PD1	PD2	0	0	0	0	0	0	Writing data word, high byte
DAC6573				DAC6573	acknowle	edges			
Master	0	0	х	х	х	х	х	х	Writing data word, low byte
DAC6573		DAC6573 acknowledges							
Master				Stop or rep	peated s	tart ⁽¹⁾			Done

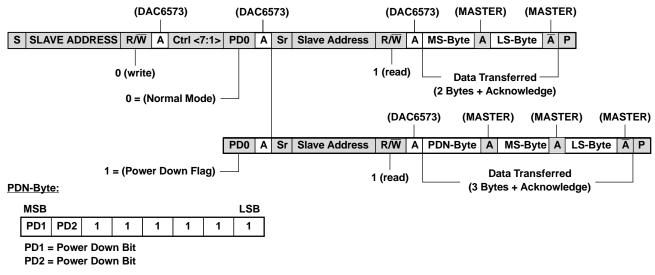
Table 5. Master Transmitter Writes to Slave Receiver (DAC6573) in HS-Mode

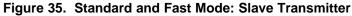
(1) Use repeated start to secure bus operation and loop back to the stage of write addressing for next Write.

(2) Once DAC6573 is properly addressed and control byte is sent, high-byte-low-byte sequences can repeat until a stop or repeated start condition is received.

DAC6573 as a Slave Transmitter—Standard and Fast Mode

Figure 35 shows the standard and fast mode master receiver addressing a DAC6573 *Slave Transmitter* with a 7-bit address.





DAC6573 as a Slave Transmitter - High-Speed Mode

Figure 36 shows an I^2 C-Master addressing DAC6573 in high-speed mode (with a 7-bit address), as a *Slave Transmitter*.

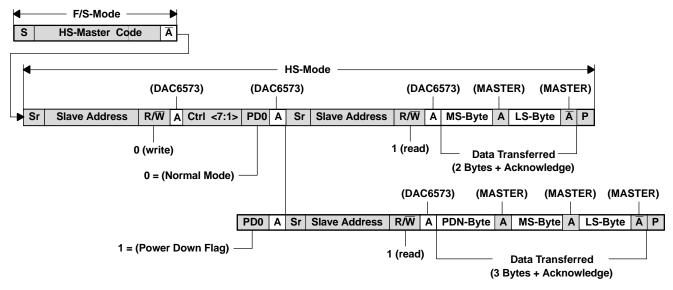


Figure 36. High-Speed Mode: Slave Transmitter

Master Receiver Reading From a Slave Transmitter (DAC6573) in Standard/Fast Modes

When reading data back from the DAC6573, the user begins with an address byte (with R/W = 0) after which the DAC6573 acknowledges by pulling SDA low. This address byte is usually followed by the control byte, which is also acknowledged by the DAC6573. Following this there is a REPEATED START condition by the master and the address is resent with (R/W = 1). This is acknowledged by the DAC6573, indicating that it is prepared to transmit data. Two or three bytes of data are then read back from the DAC6573, depending on the (PD0-Bit). The value of *Buff-Sel1* and *Buff-Sel0* determines, which channel data is read back. A STOP Condition follows.

With the (PD0-Bit = 0) the DAC6573 transmits 2 bytes of data, *HIGH-BYTE* followed by the *LOW-BYTE* (refer to Table 6. Data Readback Mode - 2 bytes).

With the (PD0-Bit = 1) the DAC6573 transmits 3 bytes of data, POWER-DOWN-BYTE followed by the HIGH-BYTE followed by the LOW-BYTE (refer to Table 6. Data Readback Mode - 3 bytes).

DATA READ	ВАСК МО	DE - 2 B	YTES						
Transmitter	MSB	6	5	4	3	2	1	LSB	Comment
Master					Start				Begin sequence
Master	1	0	0	1	1	A1	A0	R/W	Write addressing (R/W=0)
DAC6573				DAC657	3 acknowle	edges			
Master	A3	A2	Load 1	Load 0	х	Buff Sel 1	Buff Sel 0	PD0	Control byte (PD0=0)
DAC6573				DAC657	3 acknowle	edges			
Master				Rep	peated star	t			
Master	1 0 0 1 1 A1 A0 R/W							R/W	Read addressing (R/W = 1)
DAC6573	DAC6573 acknowledges								
DAC6573	D9	D8	D7	D6	D5	D4	D3	D2	Reading data word, high byte
Master				Master	acknowled	ges			
DAC6573	D1	D0	х	х	х	х	х	х	Reading data word, low byte
Master				Master n	ot acknowle	edges			Master signal end of read
Master				Stop or	repeated st	art ⁽¹⁾			Done
DATA READ	ВАСК МО	DE - 3 B	YTES						
Transmitter	MSB	6	5	4	3	2	1	LSB	Comment
Master					Start				Begin sequence
Master	1	0	0	1	1	A1	A0	R/W	Write addressing (R/W=0)
DAC6573				DAC657	3 acknowle	edges			
Master	A3	A2	Load 1	Load 0	х	Buff Sel 1	Buff Sel 0	PD0	Control byte (PD0=1)
DAC6573				DAC657	3 acknowle	edges			
Master				Rep	peated star	t			
Master	1	0	0	1	1	A1	A0	R/W	Read addressing (R/W = 1)
DAC6573				DAC657	3 acknowle	edges			
DAC6573	PD1	PD2	1	1	1	1	1	1	Read power down byte
Master									
DAC6573	D9	D8	D7	D6	D5	D4	D3	D2	Reading data word, high byte
Master		•	•	Master	acknowled	ges	· · ·		
DAC6573	D1	D0	х	х	х	х	х	х	Reading data word, low byte
Master		•			Master signal end of read				
Master				Stop or	repeated st	art ⁽¹⁾			Done

Table 6. Read Sequence in F/S Mode

(1) Use repeated start to secure bus operation and loop back to the stage of write addressing for next Write.

Master Receiver Reading From a Slave Transmitter (DAC6573) in HS-Mode

When reading data to the DAC6573 in HS-MODE, the master begins to transmit, what is called the *HS-Master Code* (0000 1XXX) in F/S mode. No device is allowed to acknowledge the *HS-Master Code*, so the *HS-Master Code* is followed by a NOT acknowledge.

The master then *switches* to HS-mode and issues a REPEATED START condition, followed by the address byte (with R/W = 0) after which the DAC6573 acknowledges by pulling SDA low. This address byte is usually followed by the control byte, which is also acknowledged by the DAC6573.

Then there is a REPEATED START condition initiated by the master and the address is resent with (R/W = 1). This is acknowledged by the DAC6573, indicating that it is prepared to transmit data. Two or three bytes of data are then read back from the DAC6573, depending on the (PD0-Bit). The value of *Buff-Sel1* and *Buff-Sel0* determines, which channel data is read back. A STOP condition follows.

With the (PD0-Bit = 0) the DAC6573 transmits 2 bytes of data, HIGH-BYTE followed by LOW-BYTE (refer to Table 7 HS-Mode Readback Sequence).

With the (PD0-Bit = 1) the DAC6573 transmits 3 bytes of data, *POWER-DOWN-BYTE* followed by the *HIGH-BYTE* followed by the *LOW-BYTE* (refer to Table 7 HS-Mode Readback Sequence).

HS MODE RE	ADBAC	K SEQU	ENCE						
Transmitter	MSB	6	5	4	3	2	1	LSB	Comment
Master					Start				Begin sequence
Master	0	0	0	0	1	Х	Х	Х	HS mode master code
NONE	Not acknowledge								No device may acknowledge HS master code
Master				Re	peated s	start			
Master	1	0	0	1	1	A1	A0	R/W	Write addressing (R/W=0)
DAC6573				DAC65	73 ackno	wledges			
Master	A3	A2	Load 1	Load 0	Х	Buff Sel 1	Buff Sel 0	PD0	Control byte (PD0 = 1)
DAC6573				DAC65	73 ackno	wledges			
Master				Re	peated s	start			
Master	1	0	0	1	1	A1	A0	R/W	Read addressing (R/W=1)
DAC6573				DAC65	73 ackno	wledges			
DAC6573	PD1	PD2	1	1	1	1	1	1	Power-down byte
Master				Maste	r acknow	ledges			
DAC6573	D9	D8	D7	D6	D5	D4	D3	D2	Reading data word, high byte
Master									
DAC6573	D1	D0	х	х	х	х	х	х	Reading data word, low byte
Master			•		Master signal end of read				
Master					Done				

Table 7. Master Receiver Reading Slave Transmitter (DAC6573) in HS-Mode

Power-On Reset

The DAC6573 contains a power-on-reset circuit that controls the output voltage during power up. On power up, the DAC register is filled with zeros and the output voltage is 0 V; it remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up. Device pins must not be brought high before supply is applied.

Power-Down Modes

The DAC6573 contains four separate power-down modes of operation. The modes are programmable via two most significant bits of the MSB byte, while (CTRL[0] = PD0 = 1). Table 8 shows how the state of these bits corresponds to the mode of operation of the device.



	Table 8. Power-Down Modes of Operation for the DAC6573							
CTRL[0]	MSB[7]	MSB[6]	OPERATING MODE					
1	0	0	PWD, high impedance DAC output					
1	0	1	PWD, 1 k Ω to GND DAC ouptut					
1	1	0	PWD, 100 k Ω to GND DAC output					
1	1	1	PWD, high impedance DAC output					

When (CTRL[0] = PD0 = 0), the device works normally with its normal power consumption of 150 μ A at 5 V per channel. However, for the power-down modes, the supply current falls to 200 nA at 5 V (50 nA at 3 V). Not only does the supply current fall but also the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the device is known while in power-down mode. There are three different options: The output is connected internally to GND through a 1 k Ω resistor, a 100 k Ω resistor or left open-circuit (high impedance). The output stage is illustrated in Figure 37.

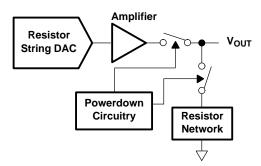


Figure 37. Output Stage During Power Down

All linear circuitry is shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power down is typically 2.5 μ s for V_{DD} = 5 V and 5 μ s for V_{DD} = 3 V. (See the Typical Curves section for additional information.)

The DAC6573 offers a flexible power-down interface based on channel register operation. A channel consists of a single 10-bit DAC with power-down circuitry, a temporary storage register (TR) and a DAC register (DR). TR and DR are both 12 bits wide. Two MSBs represent the power-down condition and the 10 LSBs represent data for TR and DR. By using bits 11 and 10 of TR and DR, a power-down condition can be temporarily stored and used just like data. Internal circuits ensure that MSB[7] and MSB[6] get transferred to TR[11] and TR[10] (DR[11] and DR[10]) when the power-down flag (CTRL[0] = PD0) is set. Therefore, DAC6573 treats power-down conditions like data and all the operational modes are still valid for power down. It is possible to broadcast a power-down condition to all the DAC6573s in the system, or it is possible to simultaneously power down a channel while updating data on other channels.

CURRENT CONSUMPTION

The DAC6573 typically consumes 150 μ A at V_{DD} = 5 V and 125 μ A at V_{DD} = 3 V for each active channel, including reference current consumption. Additional current consumption can occur at the digital inputs if V_{IH} << V_{DD}. For most efficient power operation, CMOS logic levels are recommended at the digital inputs to the DAC. In power-down mode, typical current consumption is 200 nA.

IOV_{DD} AND VOLTAGE TRANSLATORS

 IOV_{DD} pin powers the digital input structures of the DAC6573. For single-supply operation, IOV_{DD} can be tied to V_{DD} . For dual-supply operation, the IOV_{DD} pin provides interface flexibility with various CMOS logic families—connect it to the logic supply of the system. Analog circuits and internal logic of the DAC6573 use V_{DD} as the supply voltage. The external logic high inputs get translated to V_{DD} by level shifters. These level shifters use the IOV_{DD} voltage as a reference to shift the incoming logic HIGH levels to V_{DD} . IOV_{DD} operates from 2.7 V to 5.5 V regardless of the V_{DD} voltage, ensuring compatibility with various logic families. Although specified down to 2.7 V, IOV_{DD} operates as low as 1.8 V with degraded timing and temperature performance. For lowest power consumption, ensure that logic V_{IH} levels are as close as possible to IOV_{DD} , and logic V_{IL} levels as close as possible to GND voltages.

DRIVING RESISTIVE AND CAPACITIVE LOADS

The DAC6573 output stage is capable of driving loads of up to 1000 pF while remaining stable. Within the offset and gain error margins, the DAC6573 can operate rail-to-rail when driving a capacitive load. Resistive loads of 2 k Ω can be driven by the DAC6573 while achieving a good load regulation. When the outputs of the DAC are driven to the positive rail under resistive loading, the PMOS transistor of each Class-AB output stage can enter into the linear region. When this occurs, the added IR voltage drop deteriorates the linearity performance of the DAC. This only occurs within approximately the top 20 mV of the DAC's digital input-to-voltage output transfer characteristic. The reference voltage applied to the DAC6573 may be reduced below the supply voltage applied to V_{DD} in order to eliminate this condition if good linearity is a requirement at full scale (under resistive loading conditions).

CROSSTALK

The DAC6573 architecture uses separate resistor strings for each DAC channel in order to achieve ultra-low crosstalk performance. DC crosstalk seen at one channel during a full-scale change on the neighboring channel is typically less than 0.01 LSBs. The ac crosstalk measured (for a full-scale, 1-kHz sine wave output generated at one channel, and measured at the remaining output channel) is typically under -100 dB.

OUTPUT VOLTAGE STABILITY

The DAC6573 exhibits excellent temperature stability of $\pm 3 \text{ ppm/°C}$ typical output voltage drift over the specified temperature range of the device. This enables the output voltage of each channel to stay within a $\pm 25 \text{-}\mu\text{V}$ window for a $\pm 1^{\circ}\text{C}$ ambient temperature change. Combined with good dc noise performance and true 10-Bit differential linearity, the DAC6573 becomes a perfect choice for closed-loop control applications.

SETTLING TIME AND OUTPUT GLITCH PERFORMANCE

Settling time to within the 10-bit accurate range of the DAC6573 is achievable within 7 μ s for a full-scale code change at the input. Worst case settling times between consecutive code changes is typically less than 2 μ s. The high-speed serial interface of the DAC6573 is designed in order to support up to 188-kSPS update rate. For full-scale output swings, the output stage of each DAC6573 channel typically exhibits less than 100 mV of overshoot and undershoot when driving a 200 pF capacitive load. Code-to-code change glitches are extremely low (~10 μ V) given that the code-to-code transition does not cross an Nx64 code boundary. Due to internal segmentation of the DAC6573, code-to-code glitches occur at each crossing of an Nx64 code boundary. These glitches can approach 100 mVs for N = 15, but settle out within ~2 μ s.

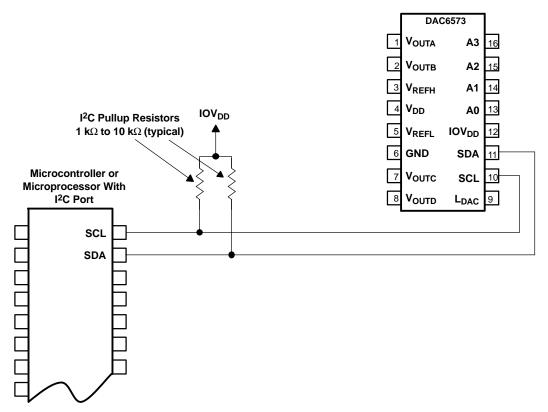


APPLICATION INFORMATION

The following sections give example circuits and tips for using the DAC6573 in various applications. For more information, contact your local TI representative, or visit the Texas Instruments website at http://www.ti.com.

BASIC CONNNECTIONS

For many applications, connecting the DAC6573 is extremely simple. A basic connection diagram for the DAC6573 is shown in Figure 38. The 0.1 μ F bypass capacitors provide the momentary bursts of extra current needed from the supplies.



NOTE: DAC6573 power and input/output connections are omitted for clarity, except I²C Inputs.

Figure 38. Typical DAC6573 Connections

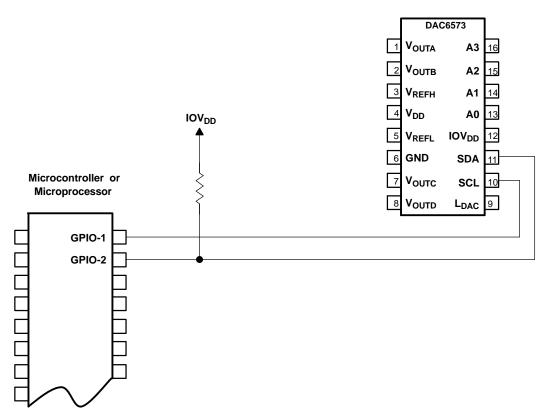
The DAC6573 interfaces directly to standard mode, fast mode and high-speed mode I^2C controllers. Any microcontroller's I^2C peripheral, including master-only and non-multiple-master I^2C peripherals, work with the DAC6573. The DAC6573 does not perform clock-stretching (i.e., it never pulls the clock line low), so it is not necessary to provide for this unless other devices are on the same I^2C bus.

Pullup resistors are necessary on both the SDA and SCL lines because I²C bus drivers are open-drain. The size of the these resistors depend on the bus operating speed and capacitance on the bus lines. Higher-value resistors consume less power, but increase the transition times on the bus, limiting the bus speed. Lower-value resistors allow higher speed at the expense of higher power consumption. Long bus lines have higher capacitance and require smaller pullup resistors to compensate. If the pullup resistors are too small the bus drivers may not be able to pull the bus line low.

USING GPIO PORTS FOR I²C

Most microcontrollers have programmable input/output pins that can be set in software to act as inputs or outputs. If an I²C controller is not available, the DAC6573 can be connected to GPIO pins, and the I²C bus protocol simulated, or bit-banged, in software. An example of this for a single DAC6573 is shown in Figure 39.

APPLICATION INFORMATION (continued)



NOTE: DAC6573 power and input/output connections are omitted for clarity, except I²C Inputs.

Figure 39. Using GPIO With a Single DAC6573

Bit-banging I²C with GPIO pins can be done by setting the GPIO line to zero and toggling it between input and output modes to apply the proper bus states. To drive the line low, the pin is set to output a zero; to let the line go high, the pin is set to input. When the pin is set to input, the state of the pin can be read; if another device is pulling the line low, this reads as a zero in the port's input register.

Note that no pullup resistor is shown on the SCL line. In this simple case the resistor is not needed. The microcontroller can simply leave the line on output, and set it to one or zero as appropriate. It can do this because the DAC6573 never drives its clock line low. This technique can also be used with multiple devices, and has the advantage of lower current consumption due to the absence of a resistive pullup.

If there are any devices on the bus that may drive their clock lines low, do not use the above method. The SCL line must be high-Z or zero, and a pullup resistor must be provided as usual. Note also that this cannot be done on the SDA line in any case, because the DAC6573 drives the SDA line low from time to time, as all I²C devices do.

Some microcontrollers have selectable strong pullup circuits built in to their GPIO ports. In some cases, these can be switched on and used in place of an external pullup resistor. Weak pullups are also provided on some microcontrollers, but usually these are too weak for I²C communication. Test any circuit before committing it to production.

USING REF02 AS A POWER SUPPLY FOR DAC6573

Due to the extremely low supply current required by the DAC6573, a possible configuration is to use a REF02 +5-V precision voltage reference to supply the required voltage to the DAC6573 supply input as well as the reference input, as shown in Figure 40. This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V. The REF02 outputs a steady supply voltage for the DAC6573. If the REF02 is used, the current it needs to supply to the DAC6573 is 600 µA typical and 900 µA max for

APPLICATION INFORMATION (continued)

 V_{DD} = 5 V. When a DAC output is loaded, the REF02 also needs to supply the current to the load. The total typical current required (with a 5-k Ω load on a single DAC output) is:

 $600 \ \mu\text{A} + (5 \ \text{V} / 5 \ \text{k}\Omega) = 1.6 \ \text{mA}$

The load regulation of the REF02 is typically 0.005%/mA, which results in an error of 400 μ V for 1.6 mA of current drawn from it. This corresponds to a 0.08 LSB error for a 0 V to 5 V output range.

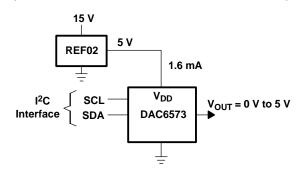


Figure 40. REF02 Power Supply

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

For best performance, the power applied to V_{DD} must be well-regulated and low noise. Switching power supplies and dc/dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, V_{DD} must be connected to a positive power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, a 1-µF to 10-µF capacitor in parallel with a 0.1-µF bypass capacitor is strongly recommended. In some situations, additional bypassing may be required, such as a 100 µF electrolytic capacitor or even a Pi filter made up of inductors and capacitors—all designed to essentially low-pass filter the –5-V supply, removing the high-frequency noise.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
DAC6573IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
DAC6573IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
DAC6573IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
DAC6573IPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal	

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC6573IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TEXAS INSTRUMENTS

www.ti.com

PACKAGE MATERIALS INFORMATION

25-Sep-2009



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC6573IPWR	TSSOP	PW	16	2000	346.0	346.0	29.0

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. β . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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