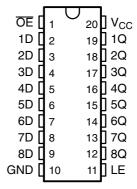
# SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

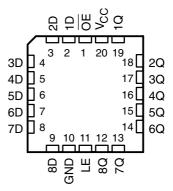
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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Packages, and Ceramic (J) DIPs

SN54LVT573 . . . J OR W PACKAGE SN74LVT573 . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT573 . . . FK PACKAGE (TOP VIEW)



#### description

These octal latches are designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight latches of the 'LVT573 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable  $(\overline{OE})$  input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.  $\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT573 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT573 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to  $125^{\circ}$ C. The SN74LVT573 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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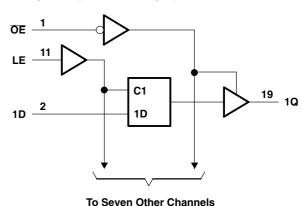
#### **FUNCTION TABLE** (each latch)

	INPUTS	OUTPUT	
OE	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	$Q_0$
Н	Χ	Χ	Z

#### logic symbol<sup>†</sup>

#### ΟE ΕN 11 LE C1 2 19 1D $\nabla$ 1Q 3 18 2D 2Q 4 17 3Q 3D 5 16 4Q 4D 6 15 5D 5Q 14 6D 6Q 8 13 7D 9 12 8D 8Q

#### logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>‡</sup>

Supply voltage range, V <sub>CC</sub>	0.5 V to 4.6 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub> (see Note 1)	0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT573	
SN74LVT573	128 mA
Current into any output in the high state, I <sub>O</sub> (see Note 2): SN54LVT573	48 mA
SN74LVT573	64 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3): DB package	0.6 W
DW package	1.6 W
PW package	
Storage temperature range, T <sub>stq</sub>	

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  - 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
  - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS SCBS138D - MAY 1992 - REVISED JULY 1995

### recommended operating conditions (see Note 4)

			SN54L	/T573	SN74L	/T573	
			MIN	MAX	MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage		2		2		V
$V_{IL}$	Low-level input voltage		0.8		8.0	V	
VI	Input voltage			5.5		5.5	V
I <sub>OH</sub>	High-level output current			-24		-32	mA
I <sub>OL</sub>	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

### SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	_	SN	54LVT5	73	SN	74LVT5	73				
PARAMETER	Ι Τ	EST CONDITIONS		MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT	
$V_{IK}$	$V_{CC} = 2.7 \text{ V},$	$I_I = -18 \text{ mA}$				-1.2			-1.2	V	
	$V_{CC} = MIN \text{ to } MAX^{\ddagger},$	$I_{OH} = -100  \mu A$		V <sub>CC</sub> -0.	.2		V <sub>CC</sub> -0	.2			
.,	$V_{CC} = 2.7 \text{ V},$	$I_{OH} = -8 \text{ mA}$		2.4			2.4			٧	
$V_{OH}$	V 0V	$I_{OH} = -24 \text{ mA}$		2						V	
	V <sub>CC</sub> = 3 V	$I_{OH} = -32 \text{ mA}$				2					
	V 07V	$I_{OL} = 100 \mu A$			0.2			0.2			
	$V_{CC} = 2.7 \text{ V}$	I <sub>OL</sub> = 24 mA				0.5			0.5		
.,		I <sub>OL</sub> = 16 mA				0.4			0.4	.,	
$V_{OL}$	, ov	I <sub>OL</sub> = 32 mA			0.5			0.5	V		
	V <sub>CC</sub> = 3 V	I <sub>OL</sub> = 48 mA		0.55							
		I <sub>OL</sub> = 64 mA						0.55			
	$V_{CC} = 0$ or $MAX^{\ddagger}$ ,				50			10			
l <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	Control inputs			±1			±1	μΑ	
·	$V_{CC} = 3.6 \text{ V}$	$V_I = V_{CC}$				1			1	•	
		$V_I = 0$	Data inputs			-5			-5		
I <sub>off</sub>	$V_{CC} = 0$ ,	$V_{I}$ or $V_{O} = 0$ to 4.5 V	-						±100	μΑ	
	V 0V	$V_{I} = 0.8 V$	Data innuta	75			75			A	
l <sub>l(hold)</sub>	V <sub>CC</sub> = 3 V	V <sub>I</sub> = 2 V	Data inputs	-75			-75			μΑ	
I <sub>OZH</sub>	$V_{CC} = 3.6 \text{ V},$	V <sub>O</sub> = 3 V				1			1	μΑ	
$I_{OZL}$	$V_{CC} = 3.6 \text{ V},$	$V_0 = 0.5 V$				-1			-1	μΑ	
			Outputs high		0.13	0.39		0.13	0.19		
Icc	$V_{CC} = 3.6 \text{ V},$	$I_{O}=0$ ,	Outputs low		8.6	14		8.6	12	mA	
icc	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled		0.13	0.39		0.13	0.19	IIIA	
Δl <sub>CC</sub> §	$V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND					0.3			0.2	mA	
C <sub>i</sub>	V <sub>I</sub> = 3 V or 0		4			4		pF			
Co	V <sub>O</sub> = 3 V or 0				8			8	_	pF	

 $<sup>^{\</sup>dagger}$  All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54L	VT573			SN74L	VT573		
		V <sub>CC</sub> = ± 0.3	3.3 V 3 V	V <sub>CC</sub> =	2.7 V	V <sub>CC</sub> = ± 0.3	3.3 V 3 V	V <sub>CC</sub> =	2.7 V	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high	3.3		3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time, data before LE↓	1		0.9		0.7		0.6		ns
t <sub>h</sub>	Hold time, data after LE↓	1.8		2		1.6		1.8		ns



<sup>‡</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

## SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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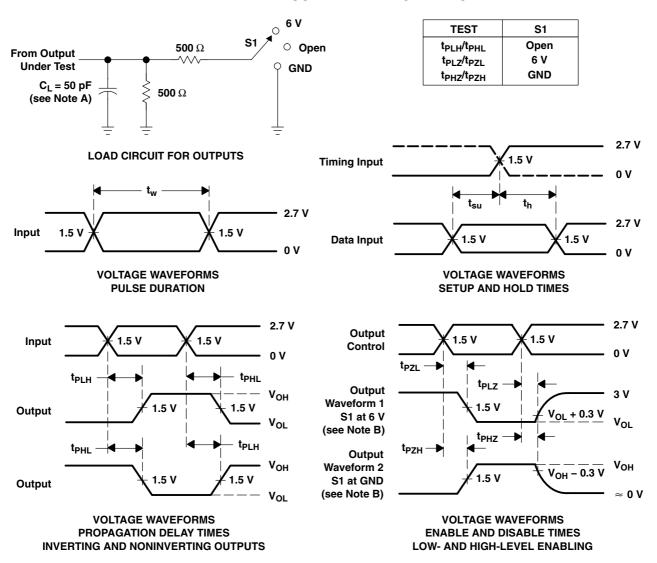
## switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

				SN54L	VT573			SN74LVT573				
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$ = 3.3 V $\pm$ 0.3 V		V <sub>CC</sub> = 2.7 V		$V_{CC}$ = 3.3 V $\pm$ 0.3 V			V <sub>CC</sub> = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
t <sub>PLH</sub>	D	0	0.5	4.7		4.9	1	2.5	4.2		4.7	20
t <sub>PHL</sub>	D	Q	0.5	4.9		5.4	1	2.7	4.3		5.2	ns
t <sub>PLH</sub>	LE	0	1	6		6.9	1.6	3.5	5.6		6.3	
t <sub>PHL</sub>	LE	Q	1.4	6.9		7.6	2.5	4.3	6.5		7.2	ns
t <sub>PZH</sub>	ŌĒ	0	0.5	5.3		6.4	1	2.8	5.1		6.2	
t <sub>PZL</sub>	OE .	Q	0.7	5.7		7.2	1.3	3.3	5.5		6.6	ns
t <sub>PHZ</sub>	OF.	0	1.2	5.9		6.9	2	3.7	5.7		6.7	20
t <sub>PLZ</sub>	ŌĒ	Q	1	5.4		5.5	1.5	3	4.6		5.1	ns

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>1</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_Q = 50 \Omega$ ,  $t_f \leq 2.5$  ns.  $t_f \leq 2.5$  ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms







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#### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74LVT573DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	Replaced by SN74LVTH573DBR
SN74LVT573DBR	NRND	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Replaced by SN74LVTH573DBR
SN74LVT573DW	NRND	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Replaced by SN74LVTH573DW
SN74LVT573DWR	NRND	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Replaced by SN74LVTH573DWR
SN74LVT573NSR	OBSOLETE	SO	NS	20		TBD	Call TI	Call TI	Replaced by SN74LVTH573NSR
SN74LVT573PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	Replaced by SN74LVTH573PWR
SN74LVT573PWR	NRND	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Replaced by SN74LVTH573PWR
SNJ54LVT573FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	Samples Not Available
SNJ54LVT573J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	Samples Not Available
SNJ54LVT573W	OBSOLETE	CFP	W	20		TBD	Call TI	Call TI	Samples Not Available

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



#### **PACKAGE OPTION ADDENDUM**

7-Jun-2010

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#### OTHER QUALIFIED VERSIONS OF SN54LVT573, SN74LVT573:

Catalog: SN74LVT573

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Military: SN54LVT573

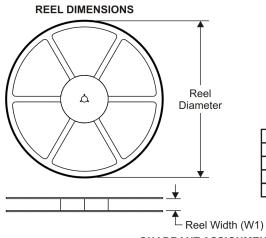
NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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#### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

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Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVT573DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVT573DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LVT573PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**PACKAGE MATERIALS INFORMATION** 

www.ti.com 5-May-2011



\*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVT573DBR	SSOP	DB	20	2000	346.0	346.0	33.0
SN74LVT573DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74LVT573PWR	TSSOP	PW	20	2000	346.0	346.0	33.0

#### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## W (R-GDFP-F20)

## CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



## FK (S-CQCC-N\*\*)

### LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



DW (R-PDSO-G20)

#### PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G20)

#### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



#### **MECHANICAL DATA**

### NS (R-PDSO-G\*\*)

## 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



#### DB (R-PDSO-G\*\*)

#### PLASTIC SMALL-OUTLINE

#### **28 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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