



# 16-Bit, Single-Channel, ±18V Output (Unbuffered), Ultra-Low Power, Serial Interface DIGITAL-TO-ANALOG CONVERTER

### FEATURES

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- 16-Bit Resolution
- Output: ±18V for ±18V Reference Input
- ±18V Supply Operation
- Very Low Power
- High Accuracy INL: 1LSB
- Low Noise: 10nV/√Hz
- Fast Settling: 1µs to 1LSB
- Fast SPI™ Interface: Up To 50MHz
- 16-Pin TSSOP Package
- Selectable Reset to Zero or Midscale

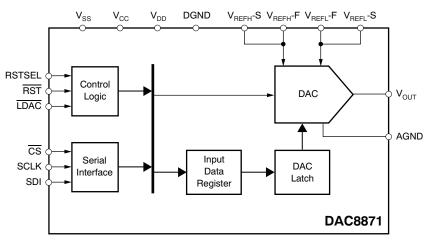
### **APPLICATIONS**

- Portable Equipment
- Automatic Test Equipment
- Industrial Process Control
- Data Acquisition Systems
- Optical Networking

# DESCRIPTION

The DAC8871 is a 16-bit, single-channel, serial input, voltage output digital-to-analog converter (DAC). The output range is determined by the reference voltage,  $V_{REFH}$  and  $V_{REFL}$ . By properly selecting the reference, the output can be unipolar or bipolar, and up to ±18V. The DAC8871 provides excellent linearity (1LSB INL), low noise, and fast settling (1µs to 1LSB of full scale output) over the specified temperature range of -40°C to +105°C. The output is unbuffered, which reduces the power consumption and the error introduced by the buffer. This device features a standard high-speed clock (up to 50MHz), and a 3V or 5V SPI serial interface to communicate with the DSP or microprocessors. For optimum performance, a set of Kelvin connections to external reference are provided.

The DAC8871 is available in a TSSOP-16 package.



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# DAC8871



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	PACKAGE- LEAD	PACKAGE DESIGNATOR
DAC8871B	±1	±1	-40°C to +105°C	8871	TSSOP-16	PW
DAC8871	±3	±1	-40°C to +105°C	8871	TSSOP-16	PW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

#### **ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Over operating free-air temperature range (unless otherwise noted).

		DAC8871	UNIT
V <sub>DD</sub> to GND		-0.3 to +7	V
Digital input voltage to GND		-0.3 to (V <sub>DD</sub> + 0.3)	V
AGND to DGND		-0.3 to +0.3	V
$V_{CC}$ to $V_{SS}$		-0.3 to +39.6	V
V <sub>CC</sub> to AGND		-0.3 to +19.8	V
V <sub>SS</sub> to AGND		+0.3 to -19.8	V
V <sub>REFH</sub> to V <sub>REFL</sub>		-0.3 to +39.6	V
V <sub>REFH</sub> to AGND		–0.3 to +19.8	V
V <sub>REFL</sub> to AGND		-19.8 to +17.5	V
Operating temperature range		-40 to +105	°C
Storage temperature range		-65 to +150	°C
Maximum junction temperature (T <sub>J</sub>	max)	+150	°C
Power dissipation		(T <sub>J</sub> max - T <sub>A</sub> )/θ <sub>JA</sub>	W
Thermal impedance, θ <sub>JA</sub> TSSOP-16		161.4	C/W

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



### **ELECTRICAL CHARACTERISTICS**

All specifications at  $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{CC} = +15V$ ,  $V_{SS} = -15V$ ,  $V_{REFH} = +10V$ ,  $V_{REFL} = -10V$ , and  $V_{DD} = +5V$ , unless otherwise noted; specifications subject to change without notice.

				DAC8871				
	PARAMETER		CONDITIONS	MIN TYP MAX			UNIT	
STATIC	C PERFORMANCE		1			1		
	Resolution			16			Bits	
		DA00074D	$V_{REFH} = 10V, V_{REFL} = -5V$		±0.75	±1	LSB	
	Linearity error	DAC8871B	$V_{REFH} = 10V, V_{REFL} = -10V$		±1	±1.5	LSB	
		DAC8871			±1	±3	LSB	
	Differential linearity	error			±0.25	±1	LSB	
	Gain error		T <sub>A</sub> = +25°C		±0.5	2	LSB	
	Gain drift				±0.1		ppm/°C	
	Bipolar zero error		T <sub>A</sub> = +25°C		±1	±4	LSB	
	Bipolar drift				±0.1		ppm/°C	
	Zero code error		T <sub>A</sub> = +25°C		±0.5	±2	LSB	
	Zero code drift				±0.05		ppm/°C	
DUTPI	JT CHARACTERIST	ICS	1			1		
	Voltage output			V <sub>REFL</sub>		V <sub>REFH</sub>	V	
	Output impedance				6.25		kΩ	
	Settling time		To 1LSB of FS, $C_L = 15 \text{ pF}$		1		μs	
	Slew rate <sup>(1)</sup>		C <sub>L</sub> = 15pF		40		V/µs	
	Digital feedthrough <sup>(2)</sup>				0.2		nV-s	
	Output noise		T <sub>A</sub> = +25°C		10		nV/√Hz	
Power supply rejection		tion	Supplies vary ±10%			1	LSB	
REFEF	RENCE INPUT		L	H		1		
/ <sub>REFH</sub>	Ref high input volta	ige range		0		+18	V	
/ <sub>REFL</sub>	Ref low input voltage	ge range		-18	V <sub>R</sub>	<sub>EFH</sub> – 1.25	V	
	Ref high input curre	ent			1.3		mA	
	Ref low input current	nt			-1.3		mA	
	Reference input im	pedance <sup>(3)</sup>		7.5			kΩ	
		•	Code = 0000h		75		pF	
	Reference input ca	pacitance	Code = FFFFh		120		pF	
DIGIT/	AL INPUTS		L	H		1		
,			$V_{DD} = +5V$	DGND		0.8	V	
/⊫	Input low voltage		$V_{DD} = +3V$	DGND		0.6	V	
,	langest bilants sould		$V_{DD} = +5V$	2.6		V <sub>DD</sub>	V	
V <sub>IH</sub> Input high voltage			$V_{DD} = +3V$	2.1		V <sub>DD</sub>	V	
	Input current					±1	μA	
	Input capacitance					10	pF	

(1) Slew Rate is measured from 10% to 90% of transition when the output changes from 0 to full scale.

(2) Digital feedthrough is defined as the impulse injected into the analog output from the digital input. It is measured when the DAC output does not change; CS is held high, while SCLK and DIN signals are toggled. It is specified with a full-scale code change on the SDI bus (that is, from all 0s to all 1s and vice versa).

(3) Reference input resistance is code-dependent, with a minimum at 8555h



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# **ELECTRICAL CHARACTERISTICS (continued)**

All specifications at  $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{CC} = +15V$ ,  $V_{SS} = -15V$ ,  $V_{REFH} = +10V$ ,  $V_{REFL} = -10V$ , and  $V_{DD} = +5V$ , unless otherwise noted; specifications subject to change without notice.

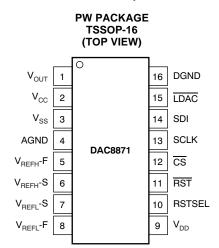
		DAC8871			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY					
V <sub>cc</sub>		+13.5	+15	+19.8	V
V <sub>SS</sub>		-19.8	-15	-13.5	V
V <sub>DD</sub>		+2.7		+5.5	V
lcc			0.01	2	μA
I <sub>SS</sub>			-0.01	-2	μA
I <sub>DD</sub>			3	10	μA
Power			15	30	μW
TEMPERATURE RANGE	·				
Specified performance		-40		+105	°C

TEXAS INSTRUMENTS

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#### **PIN CONFIGURATION (NOT TO SCALE)**

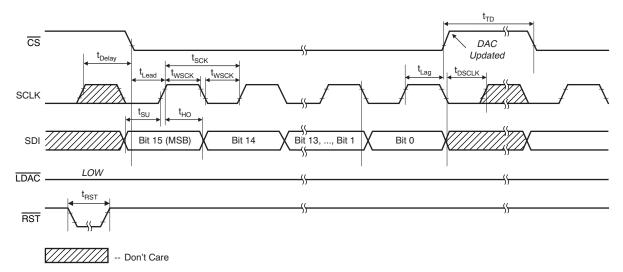


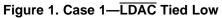
#### **TERMINAL FUNCTIONS**

TER	MINAL	DESCRIPTION
NO.	NAME	DESCRIPTION
1	V <sub>OUT</sub>	Analog output of the DAC
2	V <sub>CC</sub>	Positive analog power supply: +15V
3	V <sub>SS</sub>	Negative analog power supply: -15V
4	AGND	Analog ground
5	V <sub>REFH-</sub> F	V <sub>REFH</sub> reference input (Force). Connect to external V <sub>REFH</sub> .
6	V <sub>REFH-</sub> S	V <sub>REFH</sub> reference input (Sense). Connect to external V <sub>REFH</sub> .
7	V <sub>REFL-</sub> S	V <sub>REFL</sub> reference input (Sense). Connect to external V <sub>REFL</sub> .
8	$V_{REFL}$ -F	V <sub>REFL</sub> reference input (Force). Connect to external V <sub>REFL</sub> .
9	V <sub>DD</sub>	Digital power. +5V for 5V interface logic; +3V for 3V logic.
10	RSTSEL	Power-On-Reset select. Determines $V_{OUT}$ after power-on reset. If tied to $V_{DD}$ , the DAC latch is set to mid-scale after power-on, and $V_{OUT}$ is $(V_{REFH} - V_{REFL})/2$ . If tied to DGND, the DAC latch is cleared ('0'), and $V_{OUT}$ is $V_{REFL}$ .
11	RST	Reset (active low)
12	CS	Chip select input (active low). Data are not clocked into SDI unless CS is low.
13	SCLK	Serial clock input
14	SDI	Serial data input. Data are latched into input register on the rising edge of SCLK.
15	LDAC	Load DAC control input (active low). When LDAC is low, the DAC latch is simultaneously updated with the content of the input register.
16	DGND	Digital ground



#### **TIMING DIAGRAMS**





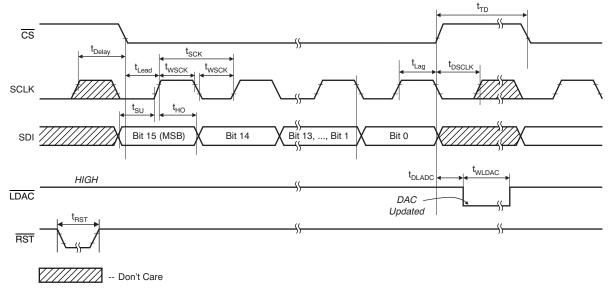


Figure 2. Case 2—LDAC Active

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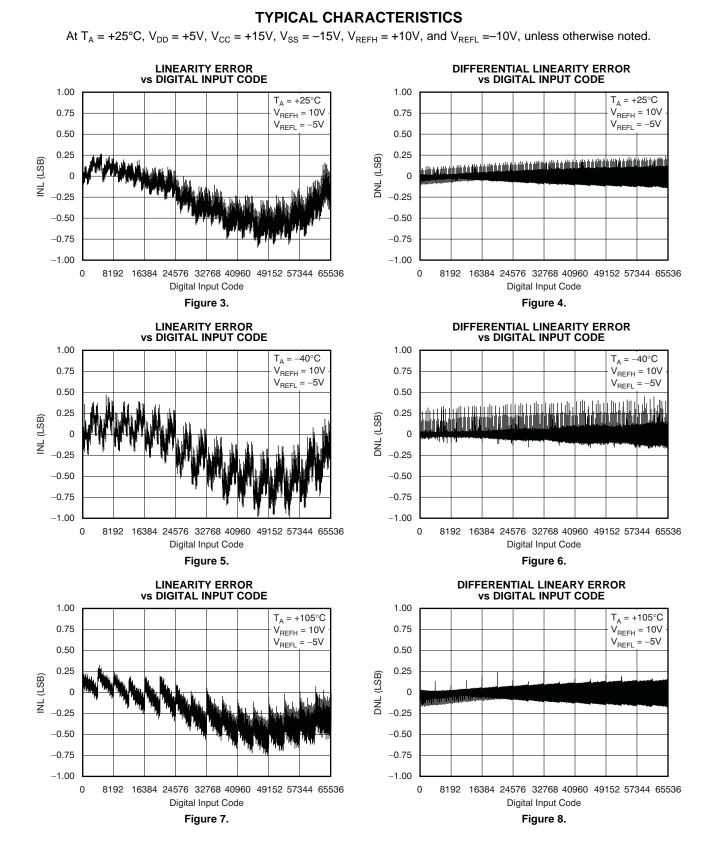
# TIMING CHARACTERISTICS: $V_{DD} = +5V^{(1)}$ <sup>(2)</sup>

At -40°C to +105°C, unless otherwise noted.

	PARAMETER	MIN	MAX	UNIT
t <sub>SCK</sub>	SCLK period	20		ns
t <sub>WSCK</sub>	SCLK high or low time	10		ns
t <sub>Delay</sub>	Delay from SCLK high to $\overline{CS}$ low	10		ns
t <sub>Lead</sub>	CS enable lead time	10		ns
t <sub>Lag</sub>	CS enable lag time	10		ns
t <sub>DSCLK</sub>	Delay from CS high to SCLK high	10		ns
t <sub>TD</sub>	CS high between active period	30		ns
t <sub>SU</sub>	Data setup time (input)	10		ns
t <sub>HO</sub>	Data hold time (input)	0		ns
t <sub>WLDAC</sub>	LDAC width	30		ns
t <sub>DLDAC</sub>	Delay from CS high to LDAC low	30		ns
t <sub>RST</sub>	Reset (RST) low	10		ns
	V <sub>DD</sub> high to <del>CS</del> low (power-up delay)	10		μs

Assured by design. Not production tested.
Sample tested during the initial release and after any redesign or process changes that may affect this parameter.





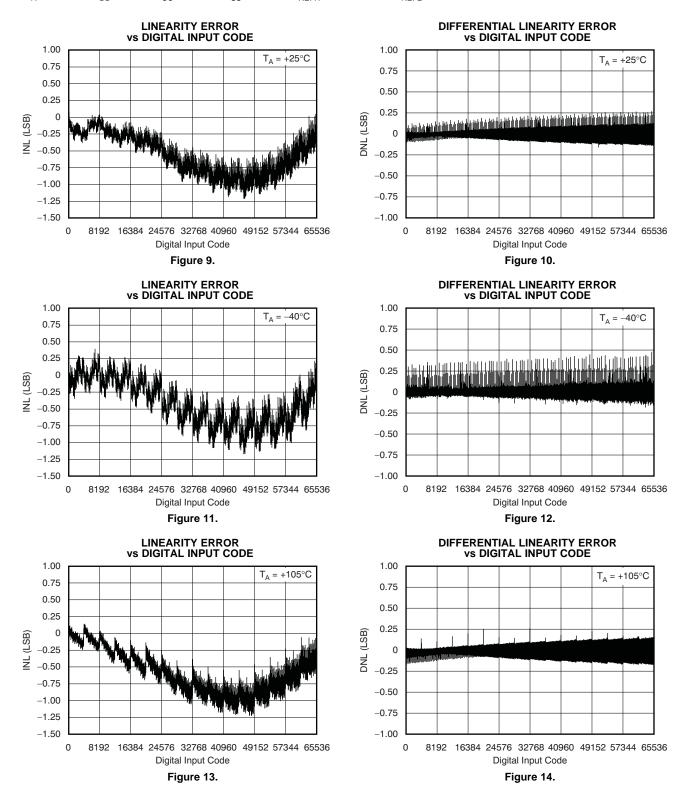
#### Submit Documentation Feedback



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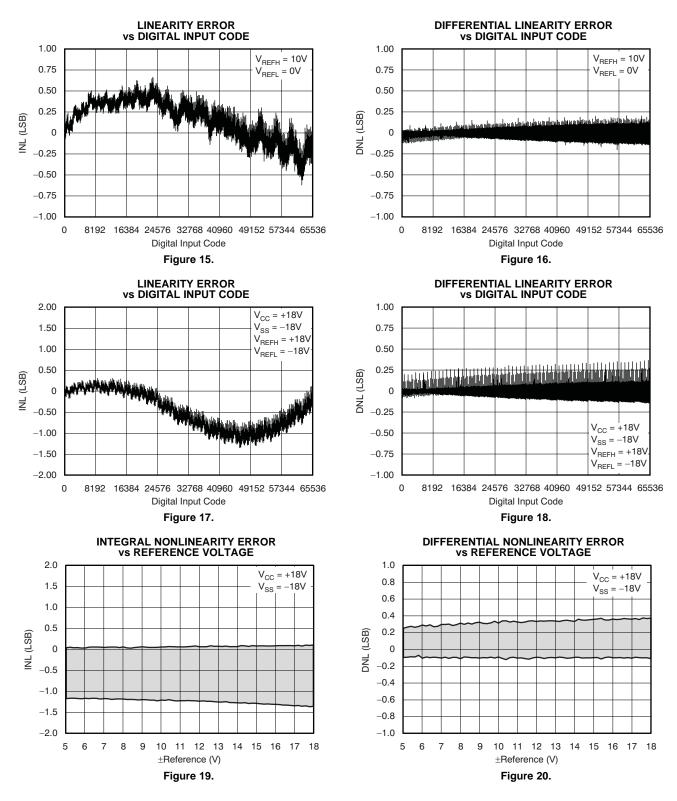
### **TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^{\circ}C$ ,  $V_{DD} = +5V$ ,  $V_{CC} = +15V$ ,  $V_{SS} = -15V$ ,  $V_{REFH} = +10V$ , and  $V_{REFL} = -10V$ , unless otherwise noted.



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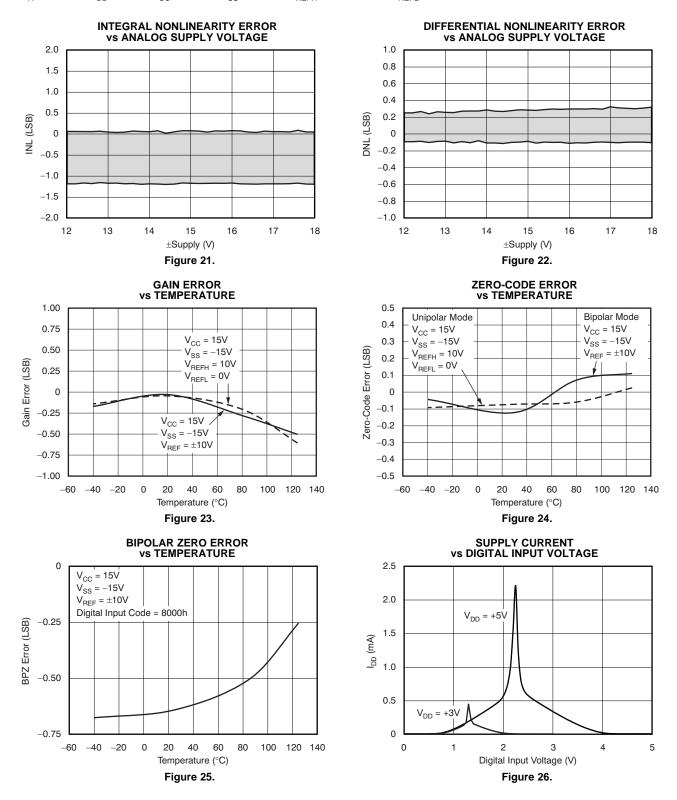
### **TYPICAL CHARACTERISTICS (continued)**

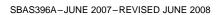




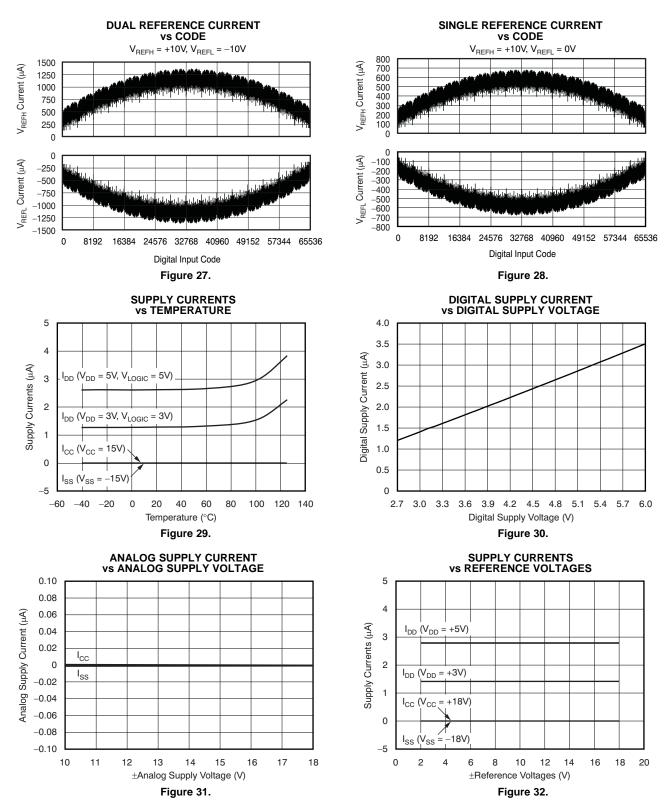
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### **TYPICAL CHARACTERISTICS (continued)**





### **TYPICAL CHARACTERISTICS (continued)**

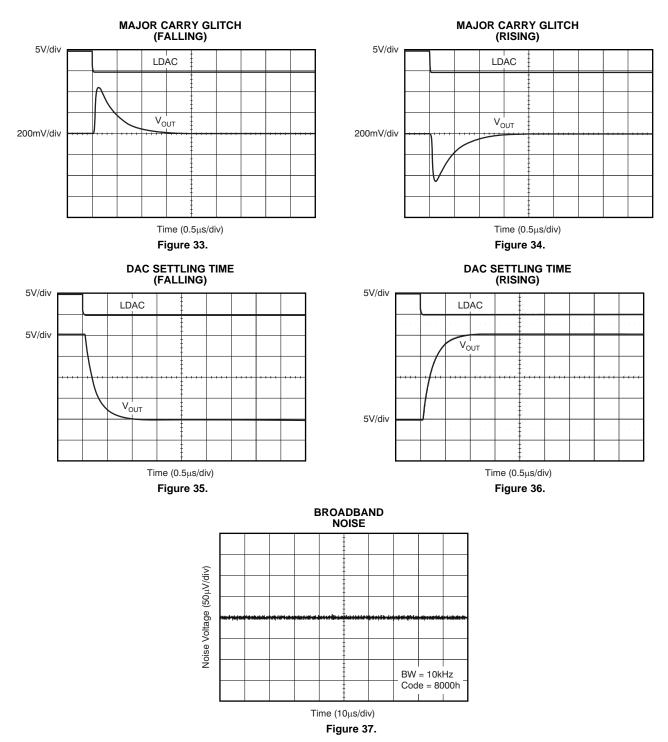




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#### **TYPICAL CHARACTERISTICS (continued)**





(1)

## THEORY OF OPERATION

#### **GENERAL DESCRIPTION**

The DAC8871 is a 16-bit, single-channel, serial-input, voltage-output DAC. It operates from a dual power supply ranging from  $\pm 13.5V$  to  $\pm 19.8V$ , and typically consumes  $10\mu$ A. The output range is from V<sub>REFL</sub> to V<sub>REFH</sub>. Data are written to this device in a 16-bit word format, via an SPI serial interface. To ensure a known power-up state, the DAC8871 is designed with a power-on reset function. After power on, the state of the RSTSEL pin sets the value of the input register and DAC latch, which sets the output state of the V<sub>OUT</sub> pin. Refer to the Power-On Reset and Hardware Reset section for more details.

Kelvin sense connections for the reference and analog ground are also included.

#### DIGITAL-TO-ANALOG SECTIONS

The DAC architecture consists of two matched DAC sections and is segmented. A simplified circuit diagram is shown in Figure 38. The four MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either  $V_{REFH}$  or  $V_{REFL}$ . The remaining 12 bits of the data word drive switches S0 to S11 of a 12-bit voltage mode R-2R ladder network.

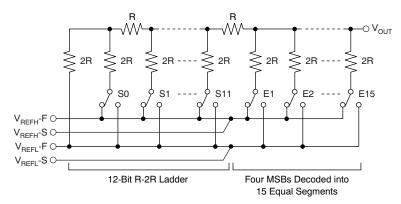


Figure 38. DAC Architecture

### **OUTPUT RANGE**

The output of the DAC is:

$$\mathrm{V_{OUT}} = \frac{\mathrm{V_{REFH}} - \mathrm{V_{REFL}}}{65536} \times \, \mathrm{Code} \, + \, \mathrm{V_{REFL}}$$

Where *Code* is the decimal data word loaded to the DAC latch.

For example, if  $V_{REFH}$  is +10V, and  $V_{REFL}$  is -10V, the range of  $V_{OUT}$  is from -10V (Code = 0000h) to +10V (Code = FFFFh).

The range of  $V_{REFL}$  is from -18V to ( $V_{REFH}$  - 1.25V), and the range of  $V_{REFH}$  is 0V to +18V. The output from the DAC8871 can be unipolar (from 0V to +18V) or bipolar by setting the proper  $V_{REFL}$  and  $V_{REFH}$  values.



**DAC8871** 

#### **POWER-ON RESET AND HARDWARE RESET**

The DAC8871 has a power-on reset function. When the RSTSEL pin is low (tied to DGND), and after power-on or a hardware reset signal is applied to the  $\overline{\text{RST}}$  pin, the DAC latch is cleared ('0') and the V<sub>OUT</sub> pin is set to negative full-scale. When RSTSEL is high, the DAC latch and V<sub>OUT</sub> are set to mid-scale.

#### SERIAL INTERFACE

The DAC8871 digital interface is a standard 3-wire connection compatible with SPI, QSPI<sup>™</sup>, Microwire<sup>™</sup> and TI DSP<sup>™</sup> interfaces, which can operate at speeds up to 50 Mbits/second. The data transfer is framed by the chip select (CS) signal. The DAC works as a bus slave. The bus master generates the synchronize clock (SCLK) and initiates the transmission. When CS is high, the DAC is not accessed, and SCLK and SDI are ignored. The bus master accesses the DAC by driving CS low. Immediately following the high-to-low transition of CS, the serial input data on the SDI pin are shifted out from the bus master synchronously on the falling edge of SCLK and latched on the rising edge of SCLK into the input shift register, MSB first. The low-to-high transition of CS transfers the content of the input shift register to the input register.

All data registers are 16 bits. It takes 16 SCLK cycles to transfer one data word to the device. To complete a whole data word,  $\overrightarrow{CS}$  must be taken high immediately after the 16th SCLK is clocked in. If more than 16 SCLK cycles are applied while  $\overrightarrow{CS}$  is low, the last 16 bits are transferred into the input register on the rising edge of  $\overrightarrow{CS}$ . However, if  $\overrightarrow{CS}$  is not kept low during the entire 16 SCLK cycles, the data are corrupted. In this case, reload the DAC latch with a new 16-bit word.

The DAC8871 has an LDAC pin that allows the DAC latch to be updated asynchronously by bringing LDAC low after CS goes high. In this case, LDAC must be kept high while CS is low. If LDAC is permanently tied low, the DAC latch will be updated immediately after the input register is loaded (caused by the low-to-high transition of CS).

#### **EXTERNAL AMPLIFIER SELECTION**

The output of the DAC8871 is unbuffered. The output impedance is approximately  $6.2k\Omega$ . If the applications require an external buffer amplifier, the selected amplifier must have a low-offset voltage ( $1LSB = 305\mu V$  for  $\pm 10V$  output range), eliminating the need for output offset trims. Input bias current should also be low because the bias current multiplied by the DAC output impedance (approximately  $6.25k\Omega$ ) adds to the zero-code error. Rail-to-rail input and output performance is required. For fast settling, the slew rate of the operational amplifier should not impede the settling time of the DAC. The output impedance of the DAC is constant and code-independent, but in order to minimize gain errors, the input impedance of the output amplifier should be as high as possible. The amplifier should also have a 3dB bandwidth of 1MHz or greater. The amplifier adds another time constant to the system, thus increasing the settling time of the output. A higher 3dB amplifier bandwidth results in a shorter effective settling time of the DAC and amplifier combination.

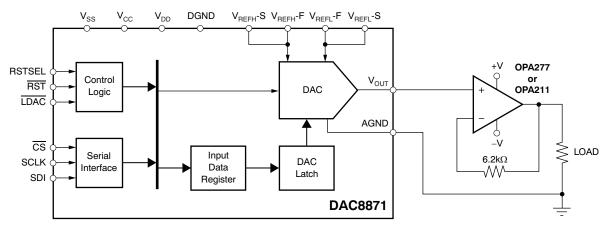


Figure 39. DAC8871 with External Amplifier

DAC8871



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### **APPLICATION INFORMATION**

#### **REFERENCE INPUT**

The DAC full-scale output voltage is determined by the reference voltage, as shown in the Output Range section.

Reference input  $V_{REFH}$  can be any voltage from 0V to +18V. Reference input  $V_{REFL}$  can be any voltage from -18V to ( $V_{REFH} - 1.25V$ ). The current into the  $V_{REFH}$  input and out of  $V_{REFL}$  depends on the DAC output voltages. Refer to Figure 27 and Figure 28 for details. The reference input appears as a varying load to the reference. If the reference can sink or source the required current, a reference buffer is not required. The DAC8871 features a reference drive (force) and sense connection that minimizes the internal errors caused by the changing reference current and the circuit impedances. Figure 40 shows a typical reference configuration.

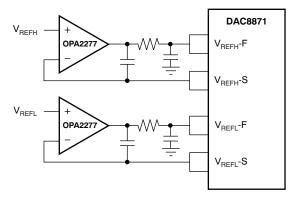


Figure 40. Buffered Reference Connection

#### POWER-SUPPLY BYPASSING

For accurate, high-resolution performance, by passing the supply pins with a  $10\mu$ F tantalum capacitor in parallel with a  $0.1\mu$ F ceramic capacitor is recommended.

#### **POWER-SUPPLY SEQUENCING**

The analog supplies ( $V_{CC}$  and  $V_{SS}$ ) must power up before the digital supply ( $V_{DD}$ ). All three supplies must power up before the reference voltages ( $V_{REFH}$  and  $V_{REFL}$ ) are applied. Additionally, because the DAC input shift register is not reset during a power-on reset (or a hardware reset through the RST pin), the CS pin must not be unintentionally asserted during power-up of the device. It is recommended that the CS pin be connected to  $V_{DD}$  through a pull-up resistor to avoid improper power-up.

Like<u>wise</u>, the state of the  $\overline{\text{LDAC}}$  pin must not be accidentally changed during power-up. It is recommended that the  $\overline{\text{LDAC}}$  pin be connected to V<sub>DD</sub> through a pull-up resistor, unless it is permanently tied to ground.

To ensure that the ESD protection circuitry of this device is not activated, all other digital pins must be kept at ground potential until  $V_{DD}$  is applied.



#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
DAC8871SBPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8871SBPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8871SBPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8871SBPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8871SPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8871SPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8871SPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DAC8871SPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



21-May-2010

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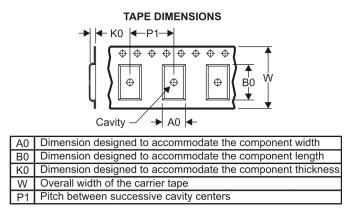
# PACKAGE MATERIALS INFORMATION

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#### TAPE AND REEL INFORMATION





#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8871SBPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DAC8871SPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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# PACKAGE MATERIALS INFORMATION

25-Sep-2009



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8871SBPWR	TSSOP	PW	16	2000	346.0	346.0	29.0
DAC8871SPWR	TSSOP	PW	16	2000	346.0	346.0	29.0

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  $\beta$ . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



# LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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