## SN74AC373-EP **OCTAL D-TYPE TRANSPARENT LATCH** WITH 3-STATE OUTPL SCAS725 - OCTOBER 2003

- **Controlled Baseline** - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of** –55°C to 125°C
- **Enhanced Diminishing Manufacturing** Sources (DMS) Support
- **Enhanced Product-Change Notification**
- **Qualification Pedigree<sup>†</sup>**
- 2-V to 6-V V<sub>CC</sub> Operation
- Inputs Accept Voltages to 6 V
- <sup>†</sup> Component gualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

### description/ordering information

This 8-bit latch features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are D-type transparent latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines in bus-organized systems without need for interface or pullup components.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, OE should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

T <sub>A</sub>	PACKAG	E‡	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC – DW	Tape and reel	SN74AC373MDWREP	SAC373MEP

#### ORDERING INFORMATION

<sup>‡</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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- Max tpd of 9.5 ns at 5 V
- **3-State Noninverting Outputs Drive Bus** Lines Directly
- Full Parallel Access for Loading

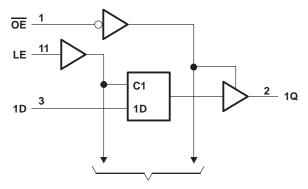
D	DW PACKAGE (TOP VIEW)										
	1	σ	20	]v <sub>cc</sub>							
1Q [	2		19	8Q							
1D 🛛	3		18	8D							
2D 🛛	4		17	7D							
2Q 🛛	5		16	] 7Q							
3Q 🛛	6		15	] 6Q							
3D 🛛	7		14	6D							
4D 🛛	8		13	5D							
4Q 🛛	9		12	] 5Q							
GND [	10		11	LE							

## **SN74AC373-EP** OCTAL D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUTS

SCAS725 – OCTOBER 2003

FUNCTION TABLE (each latch)									
	INPUTS		OUTPUT						
OE	LE	D	Q						
L	Н	Н	Н						
L	Н	L	L						
L	L	Х	Q <sub>0</sub>						
Н	Х	Х	Z						

## logic diagram (positive logic)



**To Seven Other Channels** 

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	$\ldots$ –0.5 V to 7 V
Input voltage range, VI (see Note 1)	$\dots \dots -0.5$ V to V <sub>CC</sub> + 0.5 V
Output voltage range, V <sub>O</sub> (see Note 1)	$\dots \dots -0.5$ V to V <sub>CC</sub> + 0.5 V
Input clamp current, $I_{IK}$ (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> )	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through V <sub>CC</sub> or GND	±200 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2)	58°C/W
Storage temperature range, T <sub>stg</sub> (see Note 3)	65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The package thermal impedance is calculated in accordance with JESD 51-7.
  - 3. Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep\_quality for additional information on enhanced plastic packaging.



# **SN74AC373-EP OCTAL D-TYPE TRANSPARENT LATCH** WITH 3-STATE OUTPUTS SCAS725 - OCTOBER 2003

## recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2	6	V
		$V_{CC} = 3 V$	2.1		
VIH	High-level input voltage	V <sub>CC</sub> = 4.5 V	3.15		V
		V <sub>CC</sub> = 5.5 V	3.85		
		$V_{CC} = 3 V$		0.9	
VIL	Low-level input voltage	$V_{CC} = 4.5V$		1.35	V
		V <sub>CC</sub> = 5.5 V		1.65	
$\vee_{I}$	Input voltage		0	VCC	V
VO	Output voltage		0	VCC	V
		$V_{CC} = 3 V$		-12	
IOH	High-level output current	V <sub>CC</sub> = 4.5 V		-24	mA
		V <sub>CC</sub> = 5.5 V		-24	
		$V_{CC} = 3 V$		12	
IOL	Low-level output current	V <sub>CC</sub> = 4.5 V		24	mA
		V <sub>CC</sub> = 5.5 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			8	ns/V
TA	Operating free-air temperature		-55	125	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			Т	<b>₄ = 25°C</b>	;			
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	UNIT
		3 V	2.9			2.9		
	I <sub>OH</sub> = -50 μA	4.5 V	4.4			4.4		
Maria		5.5 V	5.4			5.4		V
VOH	$I_{OH} = -12 \text{ mA}$	3 V	2.56			2.4		V
	1 04 mA	4.5 V	3.86			3.7		
	I <sub>OH</sub> = -24 mA	5.5 V	4.86			4.7		
					0.1		0.1	
	l <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1	
N		5.5 V			0.1		0.1	V
V <sub>OL</sub>	I <sub>OL</sub> = 12 mA	3 V			0.36		0.5	V
		4.5 V			0.36		0.5	
	I <sub>OL</sub> = 24 mA	5.5 V			0.36		0.5	
lj	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μΑ
IOZ	$V_{O} = V_{CC} \text{ or } GND$	5.5 V			±0.25		±5	μΑ
ICC	$V_{I} = V_{CC} \text{ or } GND,$ $I_{O} = 0$	5.5 V			4		80	μΑ
Ci	$V_{I} = V_{CC} \text{ or } GND$	5 V		4.5				pF



## SN74AC373-EP OCTAL D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUTS

SCAS725 - OCTOBER 2003

### timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

		T <sub>A</sub> = 2	T <sub>A</sub> = 25°C			
		MIN	MAX	MIN	MAX	UNIT
tw	Pulse duration, LE high	5.5		6.5		ns
t <sub>su</sub>	Setup time, data before LE $\downarrow$	5.5		6.5		ns
th	Hold time, data after LE $\downarrow$	1		1		ns

# timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

		T <sub>A</sub> = 2	25°C		MAX	UNIT
		MIN	MAX	MIN	MAX	UNIT
tw	Pulse duration, LE high	4		5		ns
t <sub>su</sub>	Setup time, data before LE $\downarrow$	4		5		ns
t <sub>h</sub>	Hold time, data after LE $\downarrow$	1		1		ns

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

	то	то	Т	<b>₄ = 25°C</b>	;			
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNIT
<sup>t</sup> PLH	(		1.5	10	13.5	1	16.5	
<sup>t</sup> PHL	D	Q	1.5	9.5	13.0	1	16	ns
<sup>t</sup> PLH	15	0	1.5	10	13.5	1	16.5	20
<sup>t</sup> PHL	LE	Q	1.5	9.5	12.5	1	15	ns
<sup>t</sup> PZH	OE	0	1.5	9	11.5	1	14	20
<sup>t</sup> PZL	OE	Q	1.5	8.5	11.5	1	13.5	ns
<sup>t</sup> PHZ	OE	Q	1.5	10	12.5	1	16	ns
<sup>t</sup> PLZ	UE	2	1.5	8	11.5	1	13	115

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

DADAMETER	то	то	Т	ן = 25°C	;	MAINI		
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNIT
<sup>t</sup> PLH	ſ	0	1.5	7	9.5	1	11.5	
<sup>t</sup> PHL	D	Q	1.5	7	9.5	1	11.5	ns
<sup>t</sup> PLH	15	0	1.5	7.5	9.5	1	12	~~
<sup>t</sup> PHL	LE	Q	1.5	7	9.5	1	11	ns
<sup>t</sup> PZH	OE	0	1.5	7	8.5	1	10.5	20
<sup>t</sup> PZL	OE	Q	1.5	6.5	8.5	1	10	ns
<sup>t</sup> PHZ	OE	Q	1.5	8	11	1	13.5	ns
<sup>t</sup> PLZ	UE	Q.	1.5	6.5	8.5	1	10.5	115

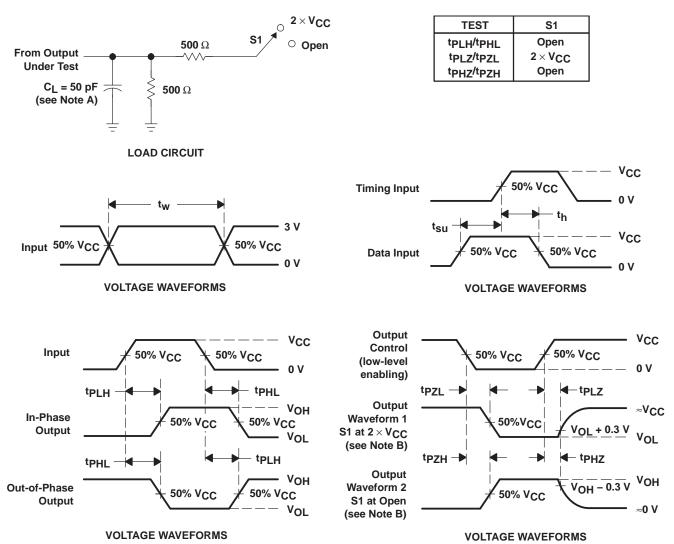
## operating characteristics, $V_{CC} = 5 V$ , $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
Cpd	Power dissipation capacitance	$C_L = 50 \text{ pF},  f = 1 \text{ MHz}$	40	pF



## SN74AC373-EP **OCTAL D-TYPE TRANSPARENT LATCH** WITH 3-STATE OUTPUTS

SCAS725 - OCTOBER 2003



### PARAMETER MEASUREMENT INFORMATION

NOTES: A. Cl includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz, Z<sub>Q</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one input transition per measurement.

#### Figure 1. Load Circuit and Voltage Waveforms



## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins I	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74AC373MDWREP	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04621-01XE	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. **TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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• Catalog: SN74AC373

• Military: SN54AC373

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION





## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal	

Device	Package Type	Package Drawing	Pins		Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC373MDWREP	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1



## PACKAGE MATERIALS INFORMATION

5-Aug-2008



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC373MDWREP	SOIC	DW	20	2000	346.0	346.0	41.0

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