FUNCTION TABLE (each latch)

11	NPUTS	OUTPUTS				
D	С	a	ā			
L	Н	L	н			
Н	Н	Н	L			
X	L	Ο0	$\overline{\alpha}_0$			

H = high level, L = low level, X = irrelevant $Q_0 = the level of Q before the high-to-low transition of G$

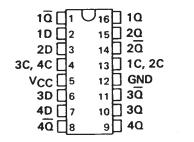
description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

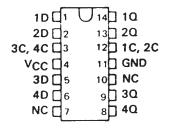
The '75 and 'LS75 feature complementary Q and $\overline{\rm Q}$ outputs from a 4-bit latch, and are available in various 16-pin packages. For higher component density applications, the '77 and 'LS77 4-bit latches are available in 14-pin flat packages.

These circuits are completely compatible with all popular TTL families. All inputs are diode-clamped to minimize transmission-line effects and simplify system design. Series 54 and 54LS devices are characterized for operation over the full military temperature range of –55°C to 125°C; Series 74, and 74LS devices are characterized for operation from 0°C to 70°C.

SN5475, SN54LS75 . . . J OR W PACKAGE SN7475 . . . N PACKAGE SN74LS75 . . . D OR N PACKAGE (TOP VIEW)

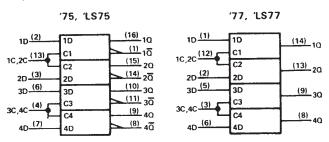


SN5477, SN54LS77 . . . W PACKAGE (TOP VIEW)



NC - No internal connection

logic symbols†



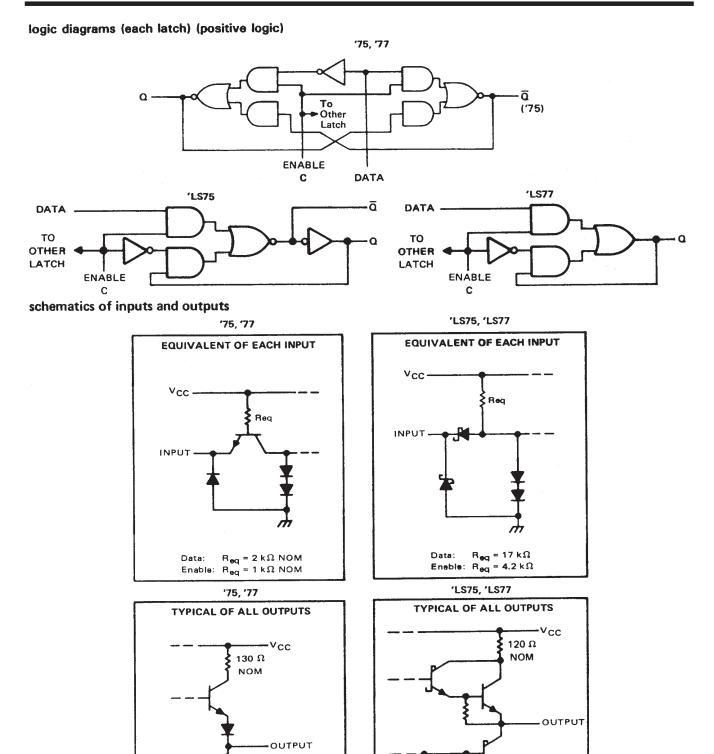
[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (See Note 1)	
Input voltage: '75, '77	5.5 V
	7 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range:	SN54'
, , ,	SN74'
Storage temperature range	65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter input transistor and is not applicable to the 'LS75 and 'LS77.





recommended operating conditions

	SN5475, SN5477			SN7475			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	CIVII
Supply voltage, V _{CC}	4.5	5	5.5	4.75	5	5,25	٧
High-level output current, IOH			-400			-400	μА
Low-level output current, IOL			16			16	mA
Width of enabling pulse, tw	20			20			กร
Setup time, t _{SU}	20			20	-		ns
Hold time, th	5			5			ns
Operating free-air temperature, TA	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CO	ONDITIONS [†]	MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	٧
VIK	Input clamp voltage		V _{CC} = MIN,	I _I = -12 mA			-1.5	V
V _{OH}	High-level output voltage		V _{CC} = M1N, V _{1L} = 0.8 V,	V _{1H} = 2 V, I _{OH} = -400 μA	2.4	3.4		٧
VOL	Low-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V,	V _{IH} = 2 V, I _{OL} = 16 mA		0.2	0.4	٧	
11	Input current at maximum input voltage	Input current at maximum input voltage					1	mA
Чн	High-level input current	D input C input	V _{CC} = MAX,	V _I = 2.4 V			80 160	μΑ
IIL	Low-level input current	D input	V _{CC} = MAX,	V ₁ = 0.4 V			-3.2 -6.4	mA
	Short-circuit output current §		V _{CC} = MAX	SN54'	-20		-57	mA
los	onort-circuit output currents		VCC WAX	SN74'	-18		-57	
Icc	Supply current		V _{CC} = MAX,	SN54'	-	32	46	mA
	•••		See Note 3	SN74'		32	53	<u> </u>

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, VCC = 5 V, TA = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN T	/P MA	K UNIT
†PLH	_			1	6 30	
^t PHL	D	Q		1	4 25	25 ns
tPLH¶	5	ā	C. = 15 = 5	2	4 40	ns
tPHL¶	D	l u	$C_L = 15 pF$, $R_L = 400 \Omega$,		7 15	113
^t PLH		Q	See Figure 1	1	6 30	ns
^t PHL	С	u	See rigure i		7 15	一 '''
tPLH¶		ā	1	1	6 30	ns
tPHL¶	С	u ·			7 15	

 $t_{PLH} \equiv propagation delay time, low-to-high-level output$



 $^{^{\}ddagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25^{\circ}\text{C}$.

Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is tested with all inputs grounded and all outputs open.

tpHL = propagation delay time, high-to-low-level output

These parameters are not applicable for the SN5477.

SN5475, SN5477, SN54LS75, SN54LS77 SN7475, SN74LS75 **4-BIT BISTABLE LATCHES**

SDLS120 - MARCH 1974 - REVISED MARCH 1988

recommended operating conditions

	1	SN54LS75 SN54LS77			SN74LS75		
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH			-400			-400	μΑ
Low-level output current, IQL			4			8	mA
Width of enabling pulse, tw	20			20			ns
Setup time, t _{su}	20			20			ns
Hold time, th	5			5			ns
Operating free-air temperature, TA	-55		125	0		70	°c

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST	TEST CONDITIONS [†]			SN54LS75 SN54LS77			SN74LS75		
					MIN	TYP‡	MAX	MIN TYPI M		MAX	
VIH	High-level input voltage				2			2			V
VIL	Low-level input voltage						0.7			0.8	V
VIK	Input clamp voltage	V _{CC} = MIN,	l ₁ = -18 mA				-1.5			-1.5	٧
VOH	High-level output voltage	V _{CC} = MIN, V _{IL} = V _{IL} max,	V _{IH} = 2 V, I _{OH} = -400	μA	2.5	3.5		2.7	3.5		٧
	V _{CC} = MIN,	V _{IH} = 2 V,	IOL = 4 mA		0.25	0.4		0.25	0.4	l v	
VOL	ow-level output voltage	VIL = VIL max		I _{OL} = 8 mA					0.35	0.5	
	Input current at			D input			0.1			0.1	mA
Ц	maximum input voltage	VCC = MAX,	V ₁ = 7 V	C input			0.4			0.4	
			V = 2.7.V	D input			20			20	μА
ЧН	High-level input current	V _{CC} = MAX,	V ₁ = 2.7 V	C input			80			80	"^
				D input			-0.4			-0.4	mA
HL	Low-level input current	V _{CC} = MAX,	V _I = 0.4 V	C input			-1.6			-1.6	1""
los	Short-circuit output current§	V _{CC} = MAX			-20		-100	-20		-100	mA
		14 - MAY	Can Note 2	'LS75		6.3	12		6.3	12	mA
1CC	Supply current	V _{CC} = MAX,	See Note 2	'LS77	T	6.9	13				

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, VCC = 5 V, TA = 25° C

	FROM	то			'LS75			'LS77			
PARAMETER¶	(INPUT)	(OUTPUT)	TEST CONDITIONS		TYP	MAX	MIN	TYP	MAX	UNIT	
tPLH					15	27		11	19	ns	
tPHL	P	Q.			9	17	Ī	9	17		
tPLH		-	_		12	20				ns	
tPHL	D	ā	- J J J J J		7	15				,,,,	
tPLH			R _L = 2 kΩ,		15	27		10	18	ns	
tPHL	С	Q	See Figure 1		14	25		10	18		
tPLH		=			16	30				ns	
^t PHL	С	ā			7	15					

[¶] tp_H = propagation delay time, low-to-high-level output



 $[\]ddagger$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

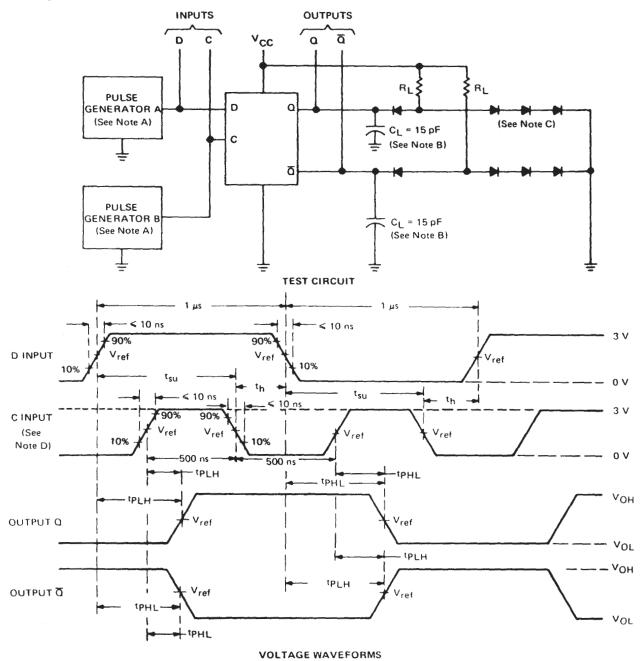
Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second

NOTE 2: ICC is tested with all inputs grounded and all outputs open.

 t_{PLH} = propagation delay time, high-to-low-level output

switching characteristics[†]

PARAMETER MEASUREMENT INFORMATION



[†]Complementary Q outputs are on the '75 and 'LS75 only.

NOTES: A. The pulse generators have the following characteristics: Z_{OUT} ≈ 50 Ω; for pulse generator A, PRR ≤ 500 kHz; for pulse generator B, PRR ≤ 1 MHz. Positions of D and C input pulses are varied with respect to each other to verify setup times.

- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.
- D. When measuring propagation delay times from the D input, the corresponding C input must be held high.
- E. For '75 and '77, V_{ref} = 1.5 V; for 'LS75 and 'LS77, V_{ref} = 1.3 V.

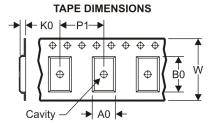
FIGURE 1





TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS75DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS75NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS75DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS75NSR	SO	NS	16	2000	346.0	346.0	33.0

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