### SN74ACT16373Q-EP 16-BIT D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUTS

**DL PACKAGE** 

SCAS678B - MAY 2002 - REVISED JULY 2002

# **Controlled Baseline** - One Assembly/Test Site, One Fabrication

- **Extended Temperature Performance of** -40°C to 125°C
- **Enhanced Diminishing Manufacturing** Sources (DMS) Support
- **Enhanced Product Change Notification**
- Qualification Pedigree<sup>†</sup>
- **Member of the Texas Instruments** Widebus™ Family
- Inputs Are TTL-Voltage Compatible
- 3-State Bus Driving True Outputs
- **Full Parallel Access for Loading**
- Distributed V<sub>CC</sub> and GND Pins Minimize **High-Speed Switching Noise**

#### description

The SN74ACT16373Q-EP is a 16-bit D-type transparent latch with 3-state outputs, designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

(TOP VIEW) 10E [ 48 ¶ 1LE 1Q1 🛮 2 47 ¶ 1D1 1Q2 🛮 3 46 1 1D2 GND ∏4 45 [] GND 1Q3 **[** 5 44 🛮 1D3 1Q4 []<sub>6</sub> 43 ¶ 1D4 42 VCC V<sub>CC</sub> **□** 7 1Q5 🛮 8 41 1D5 1Q6 🛮 9 40 ¶ 1D6 GND 110 39 GND 38 1D7 1Q7 [ 11 1Q8 🛮 12 37 **∏** 1D8 2Q1 [] 13 36 **□** 2D1 2Q2 [] 14 35 2D2 GND [ 15 34 | GND 2Q3 ∏ 16 33 **∏** 2D3 2Q4 **∏** 17 32**∏** 2D4 V<sub>CC</sub> **∐** 18 31 V<sub>CC</sub> 2Q5 [] 19 30 2D5 2Q6 20 29 2D6 GND 1 21 28 | GND 2Q7 22 27 2D7 2Q8 🛮 23 26 2D8 20E 24 25 2LE

This device can be used as two 8-bit latches or one 16-bit latch. The Q outputs of the latches follow the data (D) inputs if the latch-enable (LE) input is taken high. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (OE) input can be used to place the outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines in a bus-organized system, without need for interface or pullup components.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.



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<sup>†</sup> Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, highly accelerated stress test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life.

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#### **ORDERING INFORMATION**

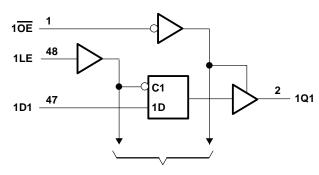
TA	PACKA	∖GE <sup>†</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SSOP - DL	Tape and reel	SN74ACT16373QDLREP	ACT16373QEP

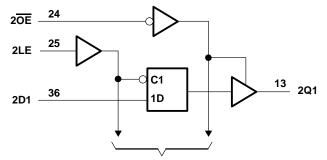
<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE** (each section)

	INPUTS	OUTPUT	
OE	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	$Q_0$
Н	Χ	Χ	Z

#### logic diagram (positive logic)





To Seven Other Channels

To Seven Other Channels

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>‡</sup>

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, V <sub>O</sub> (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±24 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±24 mA
Continuous current through V <sub>CC</sub> or GND	±260 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 2): DL package	1.2 W
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.



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#### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage (see Note 4)	4.5	5.5	V
VIH	High-level input voltage	2		V
VIL	Low-level input voltage		0.8	V
٧ <sub>I</sub>	Input voltage	0	VCC	V
٧o	Output voltage	0	VCC	V
ІОН	High-level output current		-16	mA
loL	Low-level output current		16	mA
Δt/Δν	Input transition rise or fall rate	0	10	ns/V
TA	Operating free-air temperature	-40	125	°C

NOTES: 3. Unused inputs should be tied to  $V_{CC}$  through a pullup resistor of approximately 5 k $\Omega$  or greater to prevent them from floating. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vaa	T,	գ = 25°C	;	MIN	MAX	UNIT
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	IVIIIV	IVIAA	UNIT
	I <sub>OH</sub> = -50 μA	4.5 V	4.4			4.4		
	ΙΟΗ = -50 μΑ	5.5 V	5.4			5.4		
Voн	I <sub>OH</sub> = -16 mA	4.5 V	3.94			3.7		V
	10H = -10 IIIA	5.5 V	4.94			4.7		
	$I_{OH} = -24 \text{ mA}^{\dagger}$	5.5 V				3.85		
	I. = 50 vA	4.5 V			0.1		0.1	
	I <sub>OL</sub> = 50 μA	5.5 V			0.1		0.1	٧
VOL	lo 16 mA	4.5 V			0.36		0.5	
	I <sub>OL</sub> = 16 mA	5.5 V			0.36		0.5	
	$I_{OL} = 24 \text{ mA}^{\dagger}$	5.5 V					0.5	
lį	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μΑ
loz	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10	μΑ
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160	μΑ
ΔlCC <sup>‡</sup>	One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V			0.9		1	mA
C <sub>i</sub>	$V_I = V_{CC}$ or GND	5 V		4.5				pF
Co	$V_I = V_{CC}$ or GND	5 V		12				pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		$T_A = 2$	25°C	MIN	MAY	UNIT
		MIN	MAX	- MIN MAX 4 1 5	ONIT	
t <sub>W</sub>	Pulse duration, LE high	4		4		ns
t <sub>su</sub>	Setup time, data before LE↓	1		1		ns
th	Hold time, data after LE↓	5		5		ns



<sup>4.</sup> All V<sub>CC</sub> and GND pins must be connected to the proper-voltage power supply.

<sup>&</sup>lt;sup>‡</sup> This is the increase in supply current for each input that is at one of the specified TTL-voltage levels rather than 0 V to V<sub>CC</sub>.

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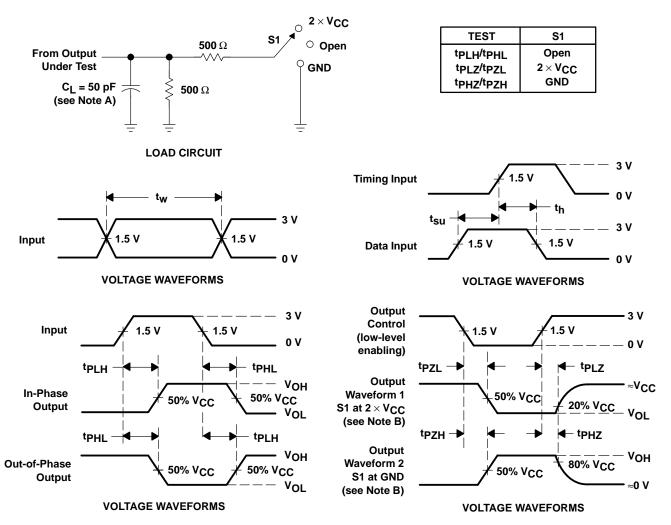
# switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	T,	գ = 25°C	;	MIN	MAX	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	IVIIIV	WAA	UNIT
t <sub>PLH</sub>	D	Q	3.8	7.9	9.4	3.8	11.8	ns
<sup>t</sup> PHL	D	y	3.1	8.2	9.7	3.1	13	115
tPLH	LE	Q	4.6	9.3	10.8	4.6	13.7	22
t <sub>PHL</sub>	LL	y	4.5	9.1	10.5	4.5	13	ns
<sup>t</sup> PZH	ŌĒ	Q	3.1	8	9.5	3.1	13	20
tPZL	OE	y	3.8	9.4	11.1	3.8	15.1	ns
<sup>t</sup> PHZ	ŌĒ	Q	5.3	8.6	9.9	5.3	11	ns
t <sub>PLZ</sub>	OE	3	4.3	7.4	8.7	4.3	9.8	115

## operating characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST COI	NDITIONS	TYP	UNIT	
		Outputs enabled	C <sub>1</sub> = 50 pF,	f = 1 MHz	43	nE.
Cpo	Power dissipation capacitance per laten	Outputs disabled	CL = 50 pr,	I = I IVITZ	4.5	pF

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50~\Omega$ ,  $t_f = 3~ns$ ,  $t_f = 3~ns$ .
  - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



#### PACKAGE OPTION ADDENDUM

5-Feb-2007

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins P	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74ACT16373QDLREP	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/03602-01XE	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

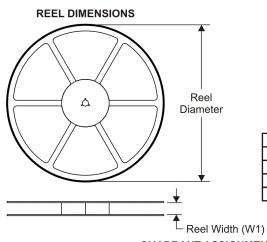
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### TAPE AND REEL INFORMATION



# TAPE DIMENSIONS KO P1 BO W Cavity A0

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT16373QDLREP	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1





#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT16373QDLREP	SSOP	DL	48	1000	346.0	346.0	49.0

#### DL (R-PDSO-G\*\*)

#### **48 PINS SHOWN**

#### PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

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