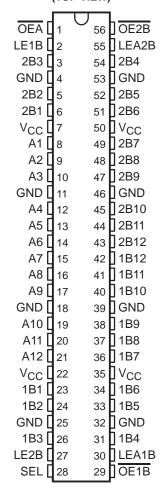
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- **Members of the Texas Instruments** Widebus™ Family
- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per **JEDEC Standard JESD-17**
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$
- **High-Impedance State During Power Up** and Power Down
- Distributed V_{CC} and GND Pin Configuration **Minimizes High-Speed Switching Noise**
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I_{OH}, 64-mA I_{OL})
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown Resistors**
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center **Spacings**

description

The SN54ABT16260 and SN74ABTH16260 are 12-bit to 24-bit multiplexed D-type latches used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and information in microprocessor bus-interface applications. This device is also useful in memory-interleaving applications.

SN54ABT16260 . . . WD PACKAGE SN74ABTH16260 . . . DL PACKAGE (TOP VIEW)



Three 12-bit I/O ports (A1-A12, 1B1-1B12, and 2B1-2B12) are available for address and/or data transfer. The output-enable ($\overline{\text{OE1B}}$, $\overline{\text{OE2B}}$, and $\overline{\text{OEA}}$) inputs control the bus-transceiver functions. The $\overline{\text{OE1B}}$ and $\overline{\text{OE2B}}$ control signals also allow bank control in the A-to-B direction.

Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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description (continued)

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ABT16260 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABTH16260 is characterized for operation from -40°C to 85°C.

Function Tables

B TO A ($\overline{OEB} = H$)

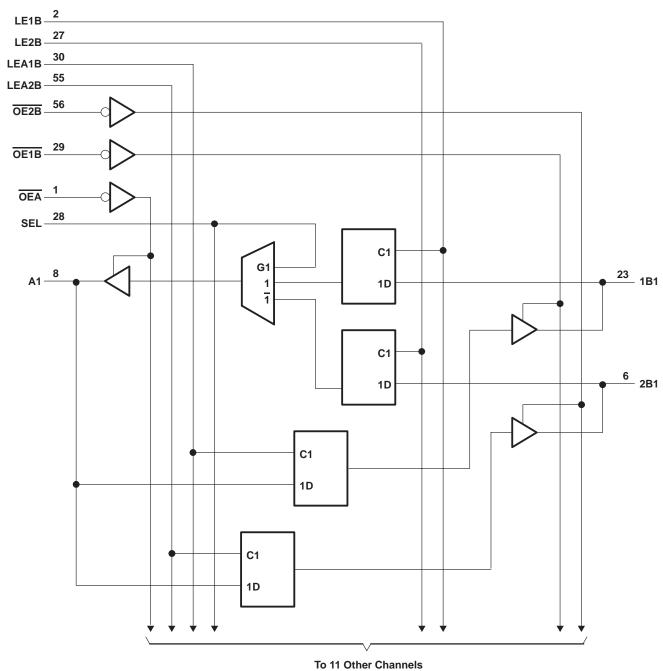
	INPUTS											
1B	2B	OEA	Α									
Н	Χ	Н	Н	Х	L	Н						
L	Χ	Н	Н	X	L	L						
Х	Χ	Н	L	X	L	A ₀						
Х	Н	L	X	Н	L	Н						
Х	L	L	X	Н	L	L						
Х	Χ	L	X	L	L	A ₀						
Χ	Χ	Χ	Χ	Χ	Н	Z						

A TO B ($\overline{OEA} = H$)

		OUTI	PUTS			
Α	LEA1B	LEA2B	OE1B	OE2B	1B	2B
Н	Н	Н	L	L	Н	Н
L	Н	Н	L	L	L	L
Н	Н	L	L	L	Н	2B ₀
L	Н	L	L	L	L	2B ₀
Н	L	Н	L	L	1B ₀	Н
L	L	Н	L	L	1B ₀	L
Х	L	L	L	L	1B ₀	2B ₀
Х	X	Χ	Н	Н	Z	Z
Х	X	X	L	Н	Active	Z
Х	X	X	Н	L	Z	Active
Х	X	Χ	L	L	Active	Active

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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Voltage range applied to any output in the high or power-off state, V _O	
Current into any output in the low state, IO: SN54ABT16260	96 mA
SN74ABTH16260	128 mA
Input clamp current, I _{IK} (V _I < 0)	–18 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DL package	74°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

			SN54AB1	Г16260	SN74ABTI	116260	UNIT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage		2		2		V
V _{IL}	Low-level input voltage			0.8		0.8	V
VI	Input voltage		0	Vcc	0	VCC	V
loн	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate		200		200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: Unused control inputs must be held high or low to prevent them from floating.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DAD	AMETER	TEST CON	DITIONS	Т	A = 25°C	;	SN54AB	Г16260	SN74ABTH	116260	UNIT
PAR	AIVIETER	TEST CON	DITIONS	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNII
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.2		-1.2		-1.2	V
		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$	2.5			2.5		2.5		
Vон		$V_{CC} = 5 V$,	$I_{OH} = -3 \text{ mA}$	3			3		3		V
VОН		V _{CC} = 4.5 V	I _{OH} = -24 mA	2			2				V
		VCC = 4.5 V	$I_{OH} = -32 \text{ mA}$	2*					2		
VoL		V _{CC} = 4.5 V	I _{OL} = 48 mA		0.36			0.5			V
		VCC = 4.5 V	I _{OL} = 64 mA			0.55*				0.55	V
V_{hys}					100						mV
1.	Control inputs	$V_{CC} = 0$ to 5.5 V, $V_{I} = V_{CC}$ or GND				±1		±1		±1	
l _l	A or B ports	$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V}$ $V_{I} = V_{CC} \text{ or GND}$	′,			±20		±100		±20	μΑ
lia i s	A or B ports	V _{CC} = 4.5 V	V _I = 0.8 V				100		100		μA
l(hold)	A OF B PORTS	VCC = 4.5 V	V _I = 2 V				-100		-100		μΑ
lozpu [‡]		$V_{CC} = 0 \text{ to } 2.1 \text{ V},$ $V_{O} = 0.5 \text{ V to } 2.7 \text{ V}, \overline{OE} = X$				±50		±50		±50	μΑ
lozpd‡		$V_{CC} = 2.1 \text{ V to 0},$ $V_{O} = 0.5 \text{ V to 2.7 V},$			±50		±50		±50	μΑ	
IOZH [§]		$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V}$ $V_{O} = 2.7 \text{ V}, \overline{OE} \ge 2 \text{ V}$				10		10		10	μΑ
loz _L §		$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V}$ $V_{O} = 0.5 \text{ V}, \overline{OE} \ge 2 \text{ V}$	/, /			-10		-10		-10	μΑ
l _{off}		$V_{CC} = 0$,	V_I or $V_O \le 4.5 \text{ V}$			±100				±100	μΑ
ICEX		V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high			50		50		50	μΑ
IOI		V _{CC} = 5.5 V,	V _O = 2.5 V	-50	-100	-225	-50	-225	-50	-225	mA
		V _{CC} = 5.5 V,	Outputs high			1.5		1.5		1.5	
ICC		$I_{O} = 0$,	Outputs low			63		63		63	mA
		$V_I = V_{CC}$ or GND	Outputs disabled			1		1		1	
Δl _{CC} #		V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND				1.5		1.5		1.5	mA
Ci		V _I = 2.5 V or 0.5 V			3						pF
C _{io}		V _O = 2.5 V or 0.5 V			11.5						pF

^{*} On products compliant to MIL-PRF-38535, this parameter does not apply.

[†] All typical values are at $V_{CC} = 5 \text{ V}$.

[‡] This parameter is characterized, but not production tested.

[§] The parameters IOZH and IOZL include the input leakage current.

[¶] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[#] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V _{CC} = T _A = 2	= 5 V, 25°C†	SN54AB1	Г16260	SN74ABTI	116260	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	3.3		3.3		3.3		ns
t _{su}	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B↓	1.5		2		1.5		ns
th	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B↓	1		1.5		1		ns

[†] These values apply only to the SN74ABTH16260.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_1 = 50$ pF (unless otherwise noted) (see Figure 1)

				SN5	4ABT16	260		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V ₍	CC = 5 V 4 = 25°C	<i>'</i> ,	MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	A or B	B or A	1	3.1	5.3	1	5.9	ns
^t PHL	AUID	BULA	1	3.4	5.4	1	6.3	115
^t PLH	1.5	A or B	1.1	3.2	5.4	1.1	6.6	ns
^t PHL	LE	AUIB	1.1	3.3	5.3	1.1	5.9	113
+	SEL (B1)		1.3	3.2	5.1	1.3	5.4	
^t PLH	SEL (B2)	A	1.1	3.4	5.4	1.1	6.3	ns
+	SEL (B1)	^	1.5	3.1	4.6	1.5	5	1115
^t PHL	SEL (B2)		1.6	3.6	5.3	1.6	6.2	
^t PZH		A or B	1	3.3	5.6	1	6.4	
tPZL	ŌĒ	AUIB	1.6	3.8	5.9	1.6	6.5	ns
^t PHZ	ŌĒ	A or B	2.2	4.1	5.9	2.2	7.5	no
t _{PLZ}	OE	A UI B	1.3	3.2	5	1.3	5.4	ight ns i

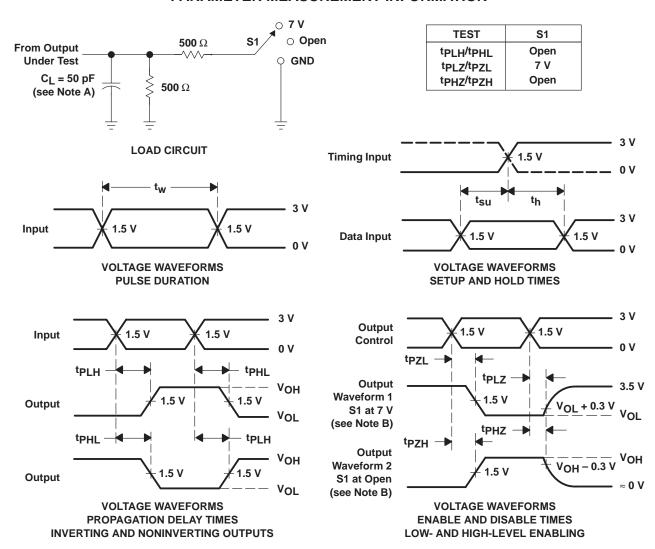
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

				SN74	ABTH1	6260		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V ₍	CC = 5 V 4 = 25°C	/, ;	MIN	MAX	UNIT
			MIN	TYP	MAX	1		
t _{PLH}	A or B	B or A	1	3.1	4.8	1	5.6	ns
t _{PHL}	AOID	BULK	1	3.4	5	1	5.9	115
t _{PLH}		A or B	1.1	3.2	4.9	1.1	5.8	nc
t _{PHL}	LE	AUID	1.1	3.3	4.9	1.1	5.3	ns
t=	SEL (B1)		1.3	3.2	4.6	1.3	5.3	
tPLH	SEL (B2)	A	1.1	3.4	4.9	1.1	6	ns
4	SEL (B1)	A	1.5	3.1	4.4	1.5	4.4	115
^t PHL	SEL (B2)		1.6	3.6	5.1	1.6	5.9	
^t PZH		A or B	1	3.3	4.7	1	5.7	20
t _{PZL}	ŌĒ	AUIB	1.6	3.8	5.1	1.6	5.8	ns
^t PHZ	ŌĒ	A or P	2.2	4.1	5.4	2.2	6.4	no
^t PLZ	OE	A or B		3.2	4.4	1.3	4.8	ns 3



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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ABTH16260DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABTH16260DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABTH16260DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABTH16260DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ABT16260WD	OBSOLETE	CFP	WD	56		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74ABTH16260:

Military: SN54ABTH16260

NOTE: Qualified Version Definitions:

Military - QML certified for Military and Defense Applications



TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABTH16260DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABTH16260DLR	SSOP	DL	56	1000	346.0	346.0	49.0

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