SN54AHC16373, SN74AHC16373 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

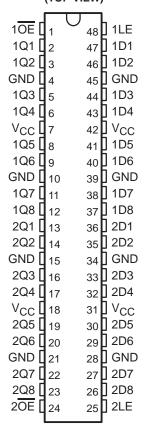
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- Members of the Texas Instruments
 Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Process
- Operating Range 2-V to 5.5-V V_{CC}
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

description

The 'AHC16373 devices are 16-bit transparent D-type latches with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

SN54AHC16373 . . . WD PACKAGE SN74AHC16373 . . . DGG, DGV, OR DL PACKAGE (TOP VIEW)



These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels at the D inputs.

A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

OE does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AHC16373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC16373 is characterized for operation from –40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

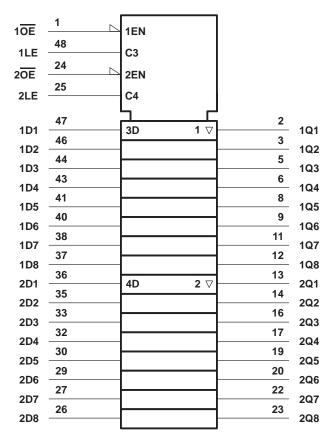
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FUNCTION TABLE (each 8-bit latch)

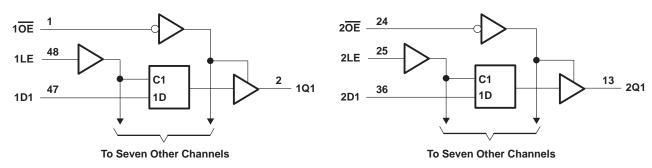
	INPUTS	ОИТРИТ	
OE	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	Q ₀
Н	Χ	Χ	Z

logic symbol†



 $[\]ensuremath{^{\dagger}}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	–0.5 V to 7 V
Output voltage range, V _O (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through each V _{CC} or GND	±75 mA
Package thermal impedance, θ _{JA} (see Note 2): DGG package	70°C/W
DGV package	58°C/W
DL package	63°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

							UNIT		
			MIN	MAX	MIN	MAX	UNII		
Vcc	Supply voltage		2	5.5	2	5.5	V		
		V _{CC} = 2 V	1.5		1.5				
VIH	High-level input voltage	V _{CC} = 3 V	2.1		2.1		V		
		V _{CC} = 5.5 V	3.85		3.85				
		V _{CC} = 2 V		0.5		0.5			
V _{IL} Low	Low-level input voltage	V _{CC} = 3 V		0.9		0.9	V		
		V _{CC} = 5.5 V		1.65		1.65			
٧ı	Input voltage	-	0	5.5	0	5.5	V		
٧o	Output voltage		0,4	Vcc	0	Vcc	V		
		V _{CC} = 2 V	Ú	-50		- 50	μΑ		
ЮН	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	2	-4 -4			4		
		$V_{CC} = 5 V \pm 0.5 V$	Q.	-8		-8	mA		
		V _{CC} = 2 V		50		50	μΑ		
lOL	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4 4			A		
		$V_{CC} = 5 V \pm 0.5 V$		8			mA		
44/454	Input transition vice or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		100		100	20/1		
Δt/Δv	Input transition rise or fall rate	$V_{CC} = 5 V \pm 0.5 V$		20		20	ns/V		
T _A	Operating free-air temperature		-55	125	-40	85	°C		

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Voc	T,	ղ = 25°C	;	SN54AH0	C16373	SN74AHC	16373	UNIT
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		2 V	1.9			1.9		1.9		
	I _{OH} = -50 μA	3 V	2.9			2.9		2.9		
Voн		4.5 V	4.4			4.4		4.4		V
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8	N.	3.8		
		2 V			0.1		0.1		0.1	
	I _{OL} = 50 μA	3 V			0.1	Ġ	0.1		0.1	
VOL		4.5 V			0.1	40	0.1		0.1	V
	I _{OL} = 4 mA	3 V			0.36	20	0.5		0.44	
	I _{OL} = 8 mA	4.5 V			0.36	² O	0.5		0.44	
lլ	V _I = V _{CC} or GND	0 V to 5.5 V			±0.1	y	±1*		±1	μΑ
loz	$V_O = V_{CC}$ or GND, $V_I = V_{IL}$ or V_{IH}	5.5 V			±0.25		±2.5		±2.5	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40		40	μΑ
Ci	V _I = V _{CC} or GND	5 V		2.5	10				10	pF
Co	$V_O = V_{CC}$ or GND	5 V		4						pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC} = 0 \text{ V}$.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

			T _A = 25°C		SN54AHC16373		SN74AHC16373	
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t _W	Pulse duration, LE high	5		5	2011	5		ns
t _{su}	Setup time, data before LE↓	4		4		4		ns
t _h	Hold time, data after LE↓	1		र १		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

		$T_A = 2$	25°C	SN54AH	C16373	SN74AHC	16373	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	ONIT
t _W	Pulse duration, LE high	5		5	100	5		ns
t _{su}	Setup time, data before LE↓	4		4		4		ns
t _h	Hold time, data after LE↓	1		र्श		1		ns

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T	չ = 25°C	;	SN54AHC	16373	SN74AHC	16373	UNIT																				
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT																				
t _{PLH}	D	Q	C _I = 15 pF		7.3*	13*	1*	15*	1	15	ns																				
t _{PHL}	D	Q	C[= 15 pi		7.3*	13*	1*	15*	1	15	115																				
t _{PLH}	LE	0	C _L = 15 pF		7*	13*	1*	15*	1	15	ns																				
tPHL	LE	Q	CL = 15 pr		7*	13*	1**	15*	1	15	110																				
t _{PZH}	ŌĒ	Q	C 15 pE		7.3*	13*	1*	15*	1	15	no																				
tPZL	OE	Q	C _L = 15 pF		7.3*	13*	1*	15*	1	15	15 ns																				
t _{PHZ}	ŌĒ	Q	C 15 pE		10*	14*	1*	16*	1	16	ns																				
t _{PLZ}	OE	Q	C _L = 15 pF		10*	14*	1* 4	16*	1	16	16																				
t _{PLH}	D	Q	C 50 pF		9.8	14	10	16	1	16	ns																				
tPHL	D		$C_L = 50 \text{ pF}$		9.8	14	70	16	1	16	110																				
tPLH	LE	Q	C 50 pF		9.5	14.5	æ 1	16.5	1	16.5	ns																				
tPHL	LE	α	C _L = 50 pF		9.5	14.5	1	16.5	1	16.5	110																				
^t PZH		0	C. 50 pF		9.3	14.9	1	16	1	16																					
tPZL	ŌĒ	Q	C _L = 50 pF		8	14.9	1	16	1	16	ns																				
t _{PHZ}	0.5	0	C. = 50 pE		10.4	15.5	1	17	1	17	ns																				
t _{PLZ}	ŌĒ	Q	Q	Q	3	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q $C_L =$	CL = 50 pr	C _L = 50 pF	C _L = 50 pF		11.6	15.5	1	17	1	17	115
tsk(o)		·	C _L = 50 pF			1.5**		·		1.5	ns																				

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T	չ = 25°C	;	SN54AHC	16373	SN74AHC	16373	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
tPLH	D	Q	C _I = 15 pF		5*	8.2*	1*	9.5*	1	9.5	ns
tPHL	D	Q	CL = 15 pr		5*	8.2*	1*	9.5*	1	9.5	115
tPLH	LE	Q	C: -15 pE		4.9*	8.5*	1*	9.5*	1	9.5	ns
tPHL	LE	Q	C _L = 15 pF		4.9*	8.5*	1*	9.5*	1	9.5	115
t _{PZH}	ŌĒ	Q	C 15 pF		5.5*	9.1*	1*	10*	1	10	no
tPZL	OE		C _L = 15 pF		5.5*	9.1*	1*	10*	1	10	ns
t _{PHZ}	ŌĒ	Q	C. 15 pF		5*	9.5*	1*	10*	1	10	ns
tPLZ	OE	Q	C _L = 15 pF		5*	9.5*	1* <	10*	1	10	10
t _{PLH}	D	Q	C. 50 pF		6.5	9.2	10	10.5	1	10.5	
tPHL			C _L = 50 pF		6.5	9.2	d	10.5	1	10.5	ns
t _{PLH}	LE	Q	C 50 pF		6.4	9.5	<u>ر</u> 1	10.5	1	10.5	ns
tPHL	LE	Q	$C_L = 50 \text{ pF}$		6.4	9.5	1	10.5	1	10.5	115
t _{PZH}	ŌĒ	Q	C: - 50 pF		6	10.1	1	11.5	1	11.5	ns
tPZL	OE	Q	C _L = 50 pF		6	10.1	1	11.5	1	11.5	115
tPHZ	ŌĒ	Q	C: - 50 pF		6.5	10.5	1	11.5	1	11.5	ns
tPLZ	OE	α	C _L = 50 pF		7.5	10.5	1	11.5	1	11.5	118
tsk(o)			C _L = 50 pF			1**				1	ns

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

^{**} On products compliant to MIL-PRF-38535, this parameter does not apply.



^{**} On products compliant to MIL-PRF-38535, this parameter does not apply.

SN54AHC16373, SN74AHC16373 **16-BIT TRANSPARENT D-TYPE LATCHES** WITH 3-STATE OUTPUTS SCLS329G - MARCH 1996 - REVISED JANUARY 2000

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

	PARAMETER	SN74	UNIT		
	PARAMETER	MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.34	0.8	V
VOL(V)	Quiet output, minimum dynamic V _{OL}		-0.1	-0.8	V
VOH(V)	Quiet output, minimum dynamic VOH		4.6		V
VIH(D)	High-level dynamic input voltage	3.5			V
V _{IL} (D)	Low-level dynamic input voltage			1.5	V

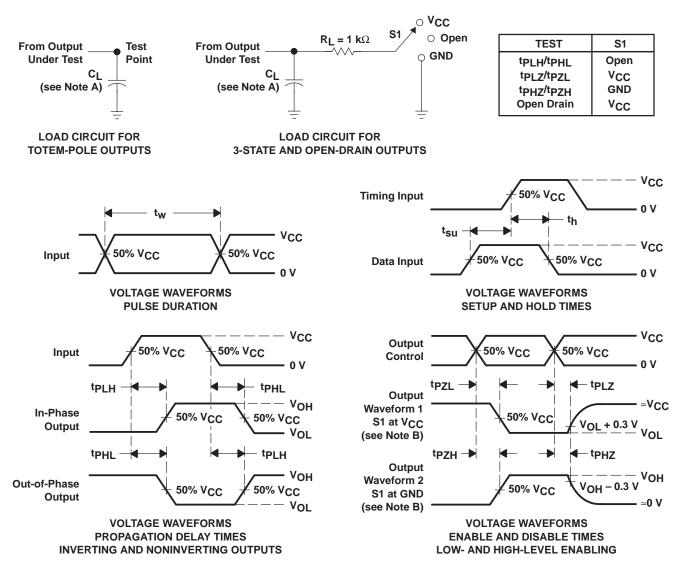
NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capaci	tance No load, f = 1 MHz	21	pF



PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq 3$ ns, $t_f \leq 3$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms







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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74AHC16373DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHC16373DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHC16373DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHC16373DGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC16373DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC16373DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC16373DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC16373DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC16373DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC16373DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

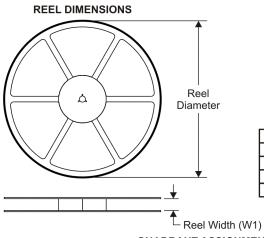
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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC16373DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74AHC16373DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74AHC16373DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

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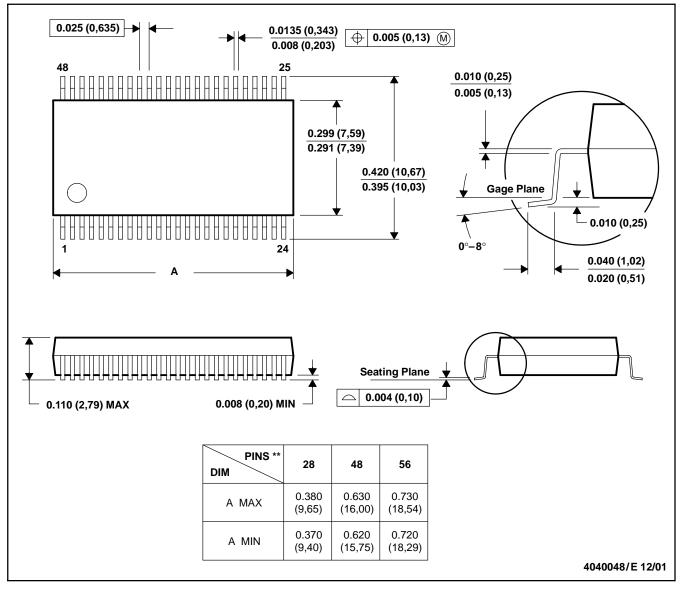
*All dimensions are nominal

7 III GITTIOTOTOTO GITO TTOTTIITIGI								
Device	Package Type	Package Drawing	Pins SPQ		Length (mm)	Width (mm)	Height (mm)	
SN74AHC16373DGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0	
SN74AHC16373DGVR	TVSOP	DGV	48	2000	346.0	346.0	33.0	
SN74AHC16373DLR	SSOP	DL	48	1000	346.0	346.0	49.0	

DL (R-PDSO-G**)

48 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194

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