

# FULL DIFFERENTIAL ANALOG INPUT 24-BIT, 192-kHz STEREO A/D CONVERTER

#### **FEATURES**

- 24-Bit Delta-Sigma Stereo A/D Converter
- High Performance:
  - Dynamic Range: 112 dB (Typical)
  - SNR: 111 dB (Typical)THD+N: -102 dB (Typical)
- High-Performance Linear Phase Antialias Digital Filter:
  - Pass-Band Ripple: ±0.005 dBStop-Band Attenuation: -100 dB
- Fully Differential Analog Input: ±2.5 V
- Audio Interface: Master- or Slave-Mode Selectable
- Data Formats: Left-Justified, I<sup>2</sup>S, Standard 24-Bit, and DSD
- Function:
  - Peak Detection
  - High-Pass Filter (HPF): -3 dB at 1 Hz,
     f<sub>S</sub> = 48 kHz
- Sampling Rate up to 192 kHz
- System Clock: 128 f<sub>S</sub>, 256 f<sub>S</sub>, 384 f<sub>S</sub>, 512 f<sub>S</sub>, or 768 f<sub>S</sub>
- Dual Power Supplies:
  - 5 V for Analog
  - 3.3 V for Digital
- Power Dissipation: 225 mW
- Small 28-Pin SSOP
- DSD Output: 1 Bit, 64 f<sub>S</sub>

#### **APPLICATIONS**

- AV Amplifier
- MD Player
- Digital VTR
- Digital Mixer
- Digital Recorder

#### DESCRIPTION

The PCM1804 is a high-performance, single-chip stereo A/D converter with fully differential analog voltage input. The PCM1804 uses a precision delta-sigma modulator and includes a linear phase antialias digital filter and high-pass filter (HPF) that removes dc offset from the input signal. The PCM1804 is suitable for a wide variety of mid- to high-grade consumer and professional applications, where excellent performance and 5-V analog supply and 3.3-V digital power-supply operation are required. The PCM1804 can achieve both PCM audio and DSD format due to the precision delta-sigma modulator. The PCM1804 is fabricated using an advanced CMOS process and is available in a small 28-pin SSOP package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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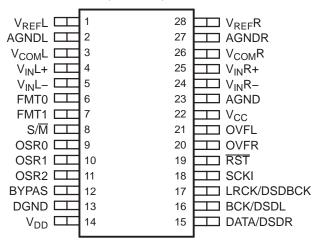




This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground. Specific guidelines for handling devices of this type are contained in the publication *Electrostatic Discharge (ESD)* (SSYA008), available from Texas Instruments.

#### **PIN ASSIGNMENTS**

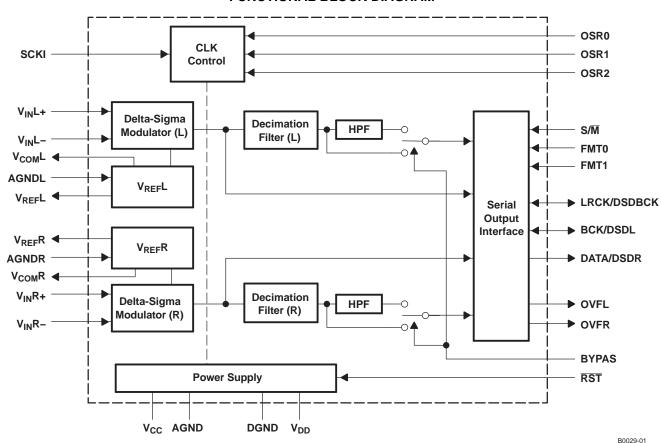
#### PCM1804 PACKAGE (TOP VIEW)



P0007-02



#### **FUNCTIONAL BLOCK DIAGRAM**





#### **Terminal Functions**

TERMINAL		.,,	
NAME	PIN	1/0	DESCRIPTIONS
AGND	23	_	Analog ground
AGNDL	2	_	Analog ground for V <sub>REF</sub> L
AGNDR	27	_	Analog ground for V <sub>REF</sub> R
BCK/DSDL	16	I/O	Bit clock input/output in PCM mode. L-channel audio data output in DSD mode. (1)
BYPAS	12	ı	HPF bypass control. High: HPF disabled, Low: HPF enabled (1)
DATA/DSDR	15	0	L-channel and R-channel audio data output in PCM mode. R-channel audio data output in DSD mode. (DSD output, when in DSD mode)
DGND	13	_	Digital ground
FMT0	6	I	Audio data format 0. See Table 5. (2)
FMT1	7	I	Audio data format 1. See Table 5. (2)
LRCK/DSDBCK	17	I/O	Sampling clock input/output in PCM and DSD modes. (1)
OSR0	9	I	Oversampling ratio 0. See Table 1 and Table 2. (2)
OSR1	10	I	Oversampling ratio 1. See Table 1 and Table 2. (2)
OSR2	11	I	Oversampling ratio 2. See Table 1 and Table 2. (2)
OVFL	21	0	Overflow signal of L-channel in PCM mode. This is available in PCM mode only.
OVFR	20	0	Overflow signal of R-channel in PCM mode. This is available in PCM mode only.
RST	19	I	Reset, power-down input, active-low (2)
SCKI	18	I	System clock input; 128 f <sub>S</sub> , 256 f <sub>S</sub> , 384 f <sub>S</sub> , 512 f <sub>S</sub> , or 768 f <sub>S</sub> . (3)
S/M	8	I	Slave/master mode selection. See Table 4. (2)
V <sub>CC</sub>	22	_	Analog power supply
$V_{COM}L$	3	_	L-channel analog common-mode voltage (2.5 V)
$V_{COM}R$	26	_	R-channel analog common-mode voltage (2.5 V)
$V_{DD}$	14	_	Digital power supply
V <sub>IN</sub> L-	5	I	L-channel analog input, negative pin
V <sub>IN</sub> L+	4	I	L-channel analog input, positive pin
V <sub>IN</sub> R-	24	I	R-channel analog input, negative pin
V <sub>IN</sub> R+	25	I	R-channel analog input, positive pin
$V_{REF}L$	1	_	L-channel voltage reference output, requires capacitors for decoupling to AGND
V <sub>REF</sub> R	28	_	R-channel voltage reference output, requires capacitors for decoupling to AGND

- Schmitt-trigger input Schmitt-trigger input with internal pulldown (51 kµ typically), 5-V tolerant. Schmitt-trigger input, 5-V tolerant.



# **ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted) (1)

	Cumply voltage	V <sub>CC</sub>	-0.3 V to 6.5 V		
	Supply voltage	$V_{DD}$	–0.3 V to 4 V		
	Ground voltage differences	AGND, AGNDL, AGNDR, DGND	±0.1 V		
	Supply voltage difference	V <sub>CC</sub> , V <sub>DD</sub>	$V_{CC} - V_{DD} < 3 V$		
	Digital input valtage	FMT0, FMT1, S/M, OSR0, OSR1, OSR2, SCKI, RST	–0.3 V to 6.5 V		
	Digital input voltage	BYPAS, DATA/DSDR, BCK/DSDL, LRCK/DSDBCK, OVFL, OVFR	-0.3 V to (V <sub>DD</sub> + 0.3 V)		
	Analog input voltage	V <sub>REF</sub> L, V <sub>REF</sub> R, V <sub>COM</sub> L, V <sub>COM</sub> R, V <sub>IN</sub> L+, V <sub>IN</sub> R+, V <sub>IN</sub> L-, V <sub>IN</sub> R-	-0.3 V to (V <sub>CC</sub> + 0.3 V)		
	Input current (any pins except	supplies)	±10 mA		
T <sub>A</sub>	Ambient temperature under b	ias	-40°C to 125°C		
T <sub>stg</sub>	Storage temperature		−55°C to 150°C		
TJ	Junction temperature		150°C		
	Lead temperature (soldering)	Lead temperature (soldering)			
	Package temperature (IR refle	ow, peak)	260°C		

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# **RECOMMENDED OPERATING CONDITIONS**

over operating free-air temperature range

		MIN	NOM	MAX	UNIT	
Analog supply voltage, V <sub>CC</sub>		4.75	5	5.25	V	
Digital supply voltage, V <sub>DD</sub>		3	3.3	3.6	V	
Analog input voltage, full-scale (-0 dB), differential input			5		Vp-p	
Digital input logic family		TTL	compatible			
Digital input along from	System clock	8.192		36.864	MHz	
Digital input clock frequency	Sampling clock	32		36.864 MHz 192 kHz	kHz	
Digital output load capacitance				10	pF	
Operating free-air temperature, T <sub>A</sub>		-10		70	70 °C	



#### **ELECTRICAL CHARACTERISTICS**

All specifications at  $T_A = 25$ °C,  $V_{CC} = 5$  V,  $V_{DD} = 3.3$  V, master mode, single-speed mode,  $f_S = 48$  kHz, system clock = 256  $f_S$ , 24-bit data, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	PCM1804	UNIT		
	PARAMETER	TEST CONDITIONS	MIN TY	P MAX	UNIT	
	Resolution		2	4	Bits	
ATA	FORMAT					
	Audio data interface format		Standard, I <sup>2</sup> S, let	ft-justified		
	Audio data bit length		2	4	Bits	
	Audio data format		MSB firs 2s complemen			
DIGIT	AL INPUT/OUTPUT					
	Logic family		TTL compa	tible		
,	High-level input voltage	(1) (2)	2	5.5	Vdc	
√ <sub>IH</sub>	nigh-level input voltage	(3)	2	$V_{DD}$	Vac	
√ <sub>IL</sub>	Low-level input voltage	(1) (2) (3)		8.0	Vdc	
		$V_{IN} = V_{DD}$ <sup>(1)</sup>	6	5 100		
IH	High-level input current	$V_{IN} = V_{DD}$ (2)		±10	μΑ	
		$V_{IN} = V_{DD}$ (3)		±100		
	Low lovel input ourrent	V <sub>IN</sub> = 0 V <sup>(1)</sup> <sup>(2)</sup>		±10		
IL	Low-level input current	$V_{IN} = 0 \ V^{(3)}$		±50	μA	
V <sub>OH</sub>	High-level output voltage	$I_{OH} = -1 \text{ mA}^{(4)}$	2.4		Vdc	
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 1 mA <sup>(4)</sup>		0.4	Vdc	
CLOC	K FREQUENCY					
s	Sampling frequency		32	192	kHz	
		256 f <sub>S</sub> , single rate <sup>(5)</sup>	12.28	8		
		384 f <sub>S</sub> , single rate <sup>(5)</sup>	18.43	2		
		512 f <sub>S</sub> , single rate <sup>(5)</sup>	24.57	6		
	Cyatam alask fraguency	768 f <sub>S</sub> , single rate <sup>(5)</sup>	36.864			
	System clock frequency	256 f <sub>S</sub> , dual rate <sup>(6)</sup>	24.57	6	MHz	
		384 f <sub>S</sub> , dual rate <sup>(6)</sup>	36.86	4		
		128 f <sub>S</sub> , quad rate <sup>(7)</sup>	24.57	24.576		
		192 f <sub>S</sub> , quad rate <sup>(7)</sup>	36.86	4		
OC AC	CCURACY					
	Gain mismatch, channel- to-channel			±3	% of FS	
	Gain error (V <sub>IN</sub> = −0.5 dB)			±4	% of FS	
	Bipolar zero error	HPF bypass	±0.	2	% of FS	

<sup>(1)</sup> Pins 6–11, 19: FMT0, FMT1, S/M, OSR0, OSR1, OSR2, RST [Schmitt-trigger input with internal pulldown (51 kµ typically), 5-V tolerant]

Pin 18: SCKI (Schmitt-trigger input, 5-V tolerant)

Pins 12, 16–17: BYPAS, BCK/DSDL, LRCK/DSDBCK (in slave mode, Schmitt-trigger input)
Pins 15–17, 20, and 21: DATA/DSDR, BCK/DSDL, LRCK/DSDBCK (in master mode), OVFR, OVFL

<sup>(5)</sup> Single rate,  $f_S = 48 \text{ kHz}$ 

<sup>(6)</sup> Dual rate,  $f_S = 96 \text{ kHz}$ (7) Quad rate,  $f_S = 192 \text{ kHz}$ 



# **ELECTRICAL CHARACTERISTICS (continued)**

All specifications at  $T_A = 25^{\circ}C$ ,  $V_{CC} = 5$  V,  $V_{DD} = 3.3$  V, master mode, single-speed mode,  $f_S = 48$  kHz, system clock = 256  $f_S$ , 24-bit data, unless otherwise noted.

	PARAMETER		TEST CONDITIONS	PC	M1804DB	UNIT		
	FARAMETER		TEST CONDITIONS	MIN	TYP MAX	UNIT		
DYNAM	IC PERFORMANCE (8)							
		$V_{IN} = -0.5 \text{ dB}$	f 40 kd la gyatam alaak 256 f		-102 -95			
		$V_{IN} = -60 \text{ dB}$ $f_S = 48 \text{ kHz}$ , system clock = 256 $f_S$			-49			
		$V_{IN} = -0.5 \text{ dB}$	f <sub>S</sub> = 96 kHz, system clock = 256 f <sub>S</sub>		-101			
THD+N	Total harmonic distortion plus noise	$V_{IN} = -60 \text{ dB}$	IS = 90 KHZ, System clock = 230 IS		<b>-47</b>	dB		
	pide ileide	$V_{IN} = -0.5 \text{ dB}$	f _ 102 kHz avatam alaak _ 129 f		-101			
		$V_{IN} = -60 \text{ dB}$	$f_S = 192 \text{ kHz}$ , system clock = 128 $f_S$		-47			
		$V_{IN} = -0.5 \text{ dB}$	DSD mode		-100			
			f <sub>S</sub> = 48 kHz, system clock = 256 f <sub>S</sub>	106	112			
	Dynamic range	$V_{IN} = -60 \text{ dB}$	f <sub>S</sub> = 96 kHz, system clock = 256 f <sub>S</sub>		112	dB		
	(A-weighted)		$f_S = 192 \text{ kHz}$ , system clock = 128 $f_S$		112	uБ		
		DSD mode			112			
		$f_S = 48 \text{ kHz, s}$	ystem clock = 256 f <sub>S</sub>	105	111			
	SNR (A-weighted)	$f_S = 96 \text{ kHz, s}$	ystem clock = 256 f <sub>S</sub>		111	dB		
	SNR (A-weighted)	$f_S = 192 \text{ kHz},$	system clock = 128 f <sub>S</sub>		111	uБ		
		DSD mode			111			
		$f_S = 48 \text{ kHz, s}$	ystem clock = 256 f <sub>S</sub>	97	109			
	Channel separation	$f_S = 96 \text{ kHz, s}$	ystem clock = 256 f <sub>S</sub>		107	dB		
		$f_S = 192 \text{ kHz},$	system clock = 128 f <sub>S</sub>		107	<u> </u>		
ANALO	G INPUT							
	Input voltage	Differential inp	ut		±2.5	V		
	Center voltage				2.5	Vdc		
	Input impedance	Single-ended			10	kμ		
DIGITAL	FILTER PERFORMANCE							
	Pass-band edge	Single rate, du	al rate		0.453 f <sub>S</sub>	Hz		
	Stop-band edge	Single rate, du	al rate	0.547 f <sub>S</sub>		Hz		
	Pass-band ripple	Single rate, du	ial rate		±0.005	dB		
	Stop-band attenuation	Single rate, du	al rate	-100		dB		
	Pass-band edge (-0.005 dB)	Quad rate			0.375 f <sub>S</sub>	Hz		
	Pass-band edge (-3 dB)	Quad rate			0.49 f <sub>S</sub>	Hz		
	Stop-band edge	Quad rate		0.77 f <sub>S</sub>		Hz		
	Pass-band ripple	Quad rate			±0.005	dB		
	Stop-band attenuation	Quad rate		-135		dB		
	Group delay	Single rate, du	ial rate		37/f <sub>S</sub>	s		
	Group delay	Quad rate			9.5/f <sub>S</sub>	s		
	HPF frequency response	–3 dB			f <sub>S</sub> /48000	Hz		

<sup>(8)</sup> f<sub>IN</sub> = 1 kHz, using System Two™ audio measurement system by Audio Precision™ in RMS mode, with 20-kHz LPF and 400-Hz HPF in calculation for single rate, or with 40-kHz LPF in calculation for dual and quad rates.



# **ELECTRICAL CHARACTERISTICS (continued)**

All specifications at  $T_A = 25^{\circ}\text{C}$ ,  $V_{CC} = 5$  V,  $V_{DD} = 3.3$  V, master mode, single-speed mode,  $f_S = 48$  kHz, system clock = 256  $f_S$ , 24-bit data, unless otherwise noted.

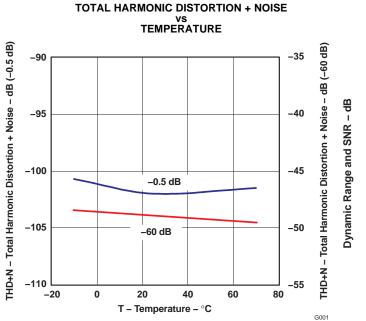
	DADAMETED	TEST CONDITIONS	PC	PCM1804DB		
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWE	R SUPPLY REQUIREMENT	S				
$V_{CC}$	Complete self-self-self-self-self-self-self-self-		4.75	5	5.25	\/- -
$V_{DD}$	Supply voltage range		3	3.3	3.6	Vdc
Icc		V <sub>CC</sub> = 5 V <sup>(9)</sup> (10) (11)		35	45	
	Supply current	$V_{DD} = 3.3 \text{ V}^{(9)(12)}$		15	20	A
$I_{DD}$		$V_{DD} = 3.3 \text{ V}^{(10)(12)}$		27		mA
		$V_{DD} = 3.3 \text{ V}^{(11)} (12)$		18		
	1	Operation, $V_{CC} = 5 \text{ V}$ , $V_{DD} = 3.3 \text{ V}^{(9) (12)}$		225	290	
<u> </u>	Davies dissination	Operation, $V_{CC} = 5 \text{ V}$ , $V_{DD} = 3.3 \text{ V}^{(10)}$ (12)		265		\^/
$P_D$	Power dissipation	Operation, $V_{CC} = 5 \text{ V}$ , $V_{DD} = 3.3 \text{ V}$ (11) (12)		235		mW
	Power down, $V_{CC} = 5 \text{ V}$ , $V_{DD} = 3.3 \text{ V}$		5			
TEMP	ERATURE RANGE					
	Operation temperature		-10		70	°C
$\theta_{JA}$	Thermal resistance			100		°C/W

 $<sup>\</sup>begin{array}{ll} \text{(9)} & \text{Single rate, } f_S = 48 \text{ kHz} \\ \text{(10)} & \text{Dual rate, } f_S = 96 \text{ kHz} \\ \text{(11)} & \text{Quad rate, } f_S = 192 \text{ kHz} \\ \text{(12)} & \text{Minimum load on DATA/DSDR (pin 15)} \end{array}$ 



# **TYPICAL PERFORMANCE CURVES - SINGLE RATE**

All specifications at  $T_A = 25^{\circ}C$ ,  $V_{CC} = 3.3 \text{ V}$ ,  $V_{DD} = 5 \text{ V}$ , master mode,  $f_S = 48 \text{ kHz}$ , system clock = 256  $f_S$ , 24-bit data, unless otherwise noted.



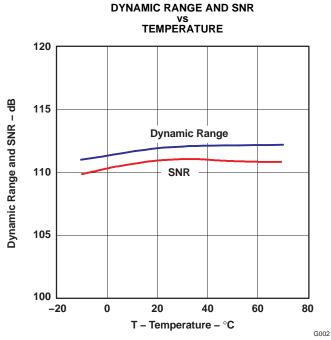
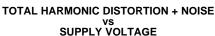


Figure 1.



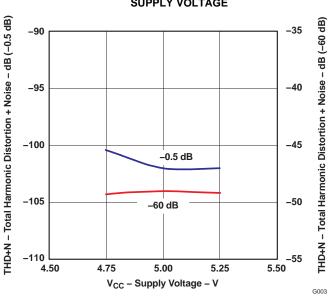


Figure 3.

# DYNAMIC RANGE AND SNR vs SUPPLY VOLTAGE

Figure 2.

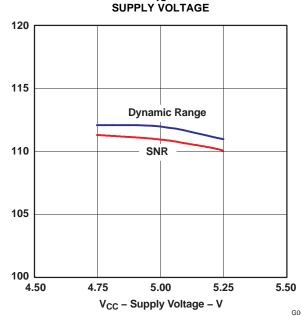


Figure 4.

Dynamic Range and SNR - dB



# **TYPICAL PERFORMANCE CURVES - SINGLE RATE (continued)**

All specifications at  $T_A = 25$ °C,  $V_{CC} = 3.3$  V,  $V_{DD} = 5$  V, master mode,  $f_S = 48$  kHz, system clock = 256  $f_S$ , 24-bit data, unless otherwise noted.

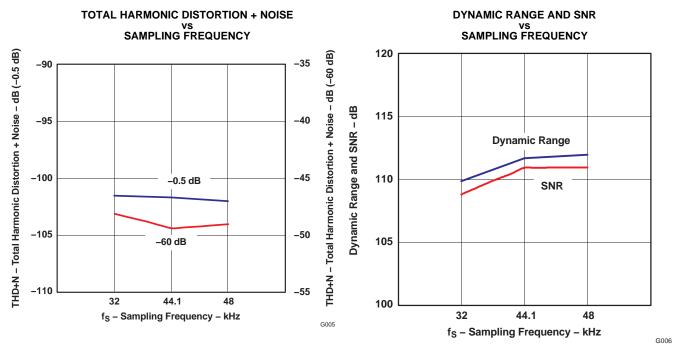
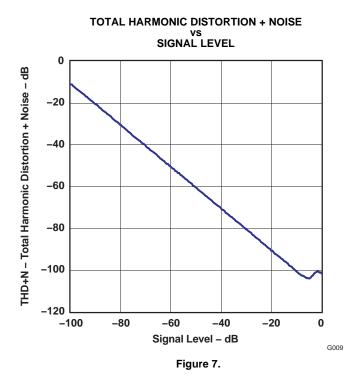


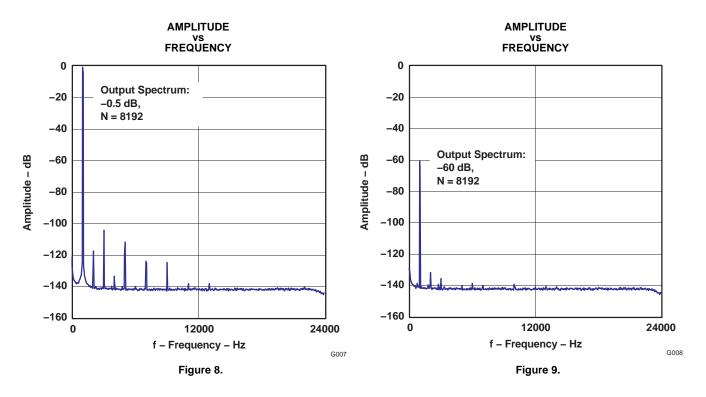
Figure 5. Figure 6.





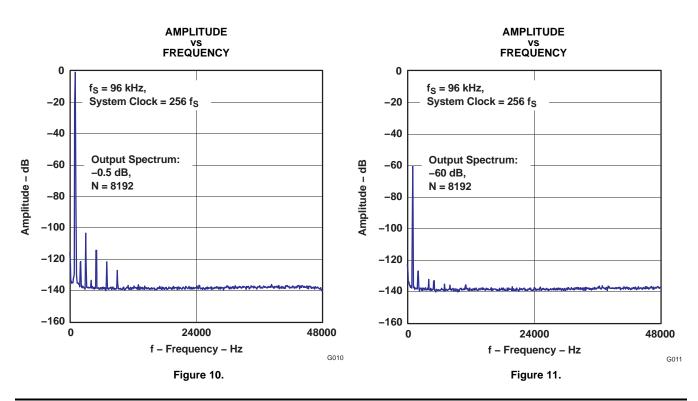
# TYPICAL PERFORMANCE CURVES - SINGLE RATE (continued)

All specifications at  $T_A = 25$ °C,  $V_{CC} = 3.3$  V,  $V_{DD} = 5$  V, master mode,  $f_S = 48$  kHz, system clock = 256  $f_S$ , 24-bit data, unless otherwise noted.



# **TYPICAL PERFORMANCE CURVES - DUAL RATE**

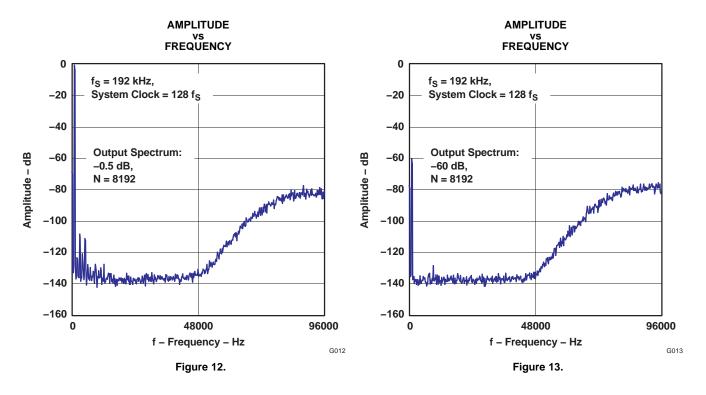
All specifications at  $T_A = 25^{\circ}C$ ,  $V_{CC} = 3.3 \text{ V}$ ,  $V_{DD} = 5 \text{ V}$ , master mode, and 24-bit data, unless otherwise noted.





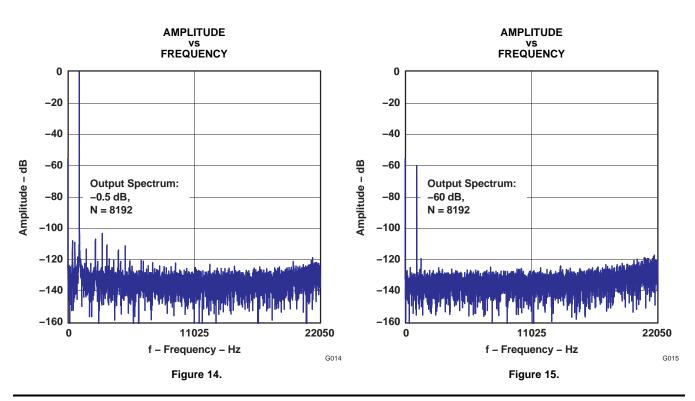
#### **TYPICAL PERFORMANCE CURVES - QUAD RATE**

All specifications at  $T_A = 25$ °C,  $V_{CC} = 3.3$  V,  $V_{DD} = 5$  V, master mode, 24-bit data, unless otherwise noted.



#### **TYPICAL PERFORMANCE CURVES - DSD MODE**

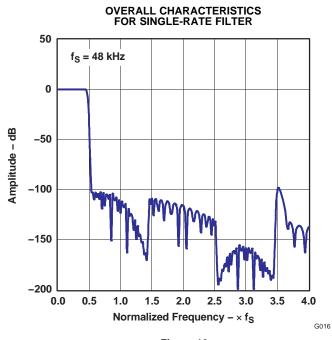
All specifications at  $T_A = 25$ °C,  $V_{CC} = 3.3$  V,  $V_{DD} = 5$  V, master mode,  $f_S = 44.1$  kHz, system clock = 16.9344 MHz, unless otherwise noted.





# TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER

# LINEAR PHASE ANTIALIAS DIGITAL FILTER FREQUENCY RESPONSE - Single-Rate



# STOP-BAND ATTENUATION CHARACTERISTICS FOR SINGLE-RATE FILTER

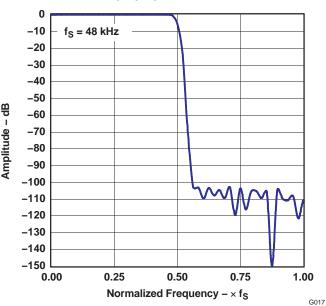


Figure 16.



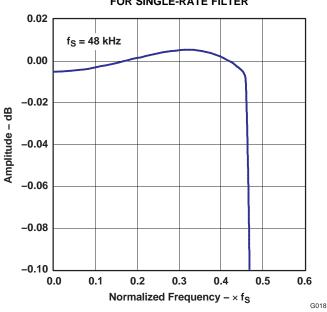


Figure 18.

# TRANSIENT BAND CHARACTERISTICS FOR SINGLE-RATE FILTER

Figure 17.

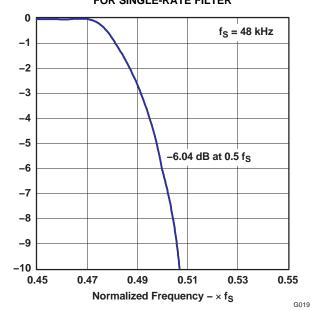
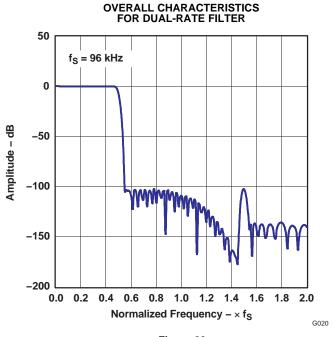


Figure 19.

Amplitude - dB



# TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (continued) LINEAR PHASE ANTIALIAS DIGITAL FILTER FREQUENCY RESPONSE - Dual-Rate





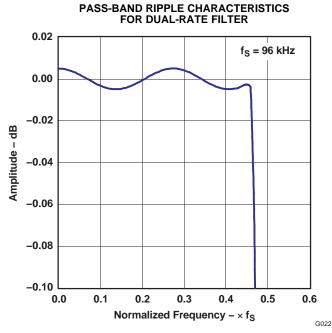


Figure 22.

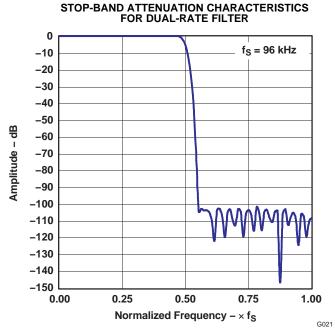


Figure 21.

# TRANSIENT BAND CHARACTERISTICS FOR DUAL-RATE FILTER

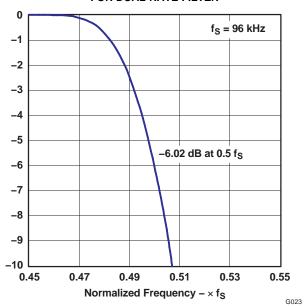


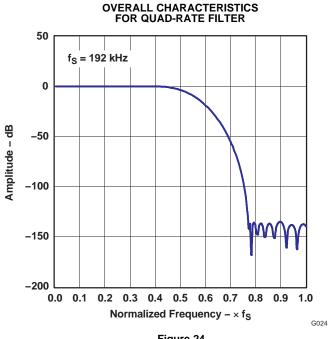
Figure 23.

Amplitude - dB

G025



# TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (continued) LINEAR PHASE ANTIALIAS DIGITAL FILTER FREQUENCY RESPONSE - Quad-Rate



#### Figure 24.

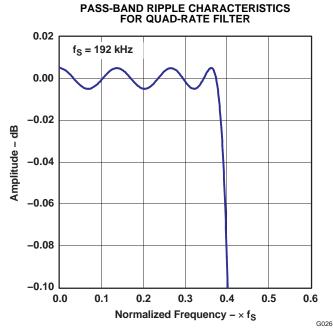
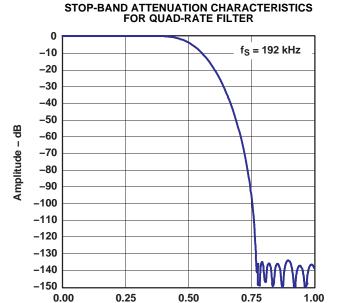


Figure 26.



Normalized Frequency –  $\times$   $f_S$ Figure 25.

# TRANSIENT BAND CHARACTERISTICS FOR QUAD-RATE FILTER

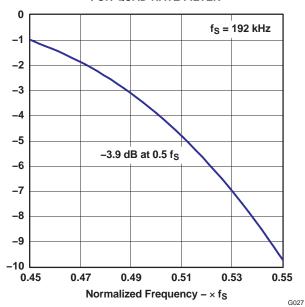
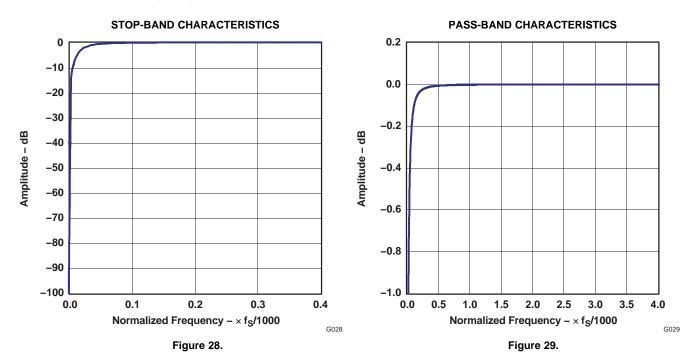


Figure 27.

Amplitude - dB



# TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (continued) HIGH-PASS FILTER (HPF) FREQUENCY RESPONSE



# PRINCIPLES OF OPERATION

#### THEORY OF OPERATION

The PCM1804 consists of a band-gap reference, a delta-sigma modulator with full-differential architecture for L-channel and R-channel, a decimation filter with a high-pass filter, and a serial interface circuit. Figure 30 illustrates the total architecture of the PCM1804. An on-chip, high-precision reference with  $10-\mu F$  external capacitor(s) provides all the reference voltage needed in the PCM1804, and it defines the full-scale voltage range of both channels. Full-differential architecture provides a wide dynamic range and excellent power-supply rejection performance. The input signal is sampled at  $\times 128$ ,  $\times 64$ , and  $\times 32$  oversampling rates according to the overasmpling ratio control, OSR[0:2]. The single rate, dual rate, and quad rate eliminate the external sample-hold amplifier. Figure 31 illustrates how for each oversampling ratio the PCM1804 decimates the modulator output down to PCM data when the modulator is running at 6.144 MHz. The delta-sigma modulation randomizes the modulator outputs and reduces the idle tone level. The oversampled data stream from the delta-sigma modulator is converted to a 1-f<sub>S</sub>, 24-bit digital signal, while removing high-frequency noise components using a decimation filter. The dc components of the signal are removed by the HPF, and the HPF output is converted to a time-multiplexed serial signal through the serial interface, which provides flexible serial formats and master/slave modes. The PCM1804 also has a DSD output mode. The PCM1804 can output the signal directly from the modulators to DSDL (pin 16) and DSDR (pin 15).



# PRINCIPLES OF OPERATION (continued)

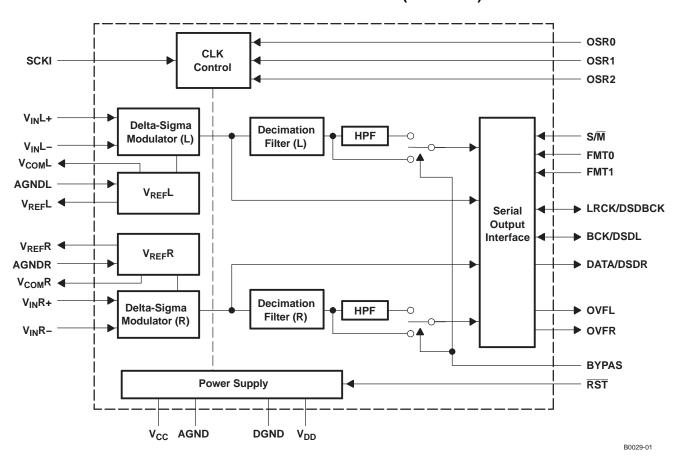


Figure 30. Total Block Diagram of PCM1804

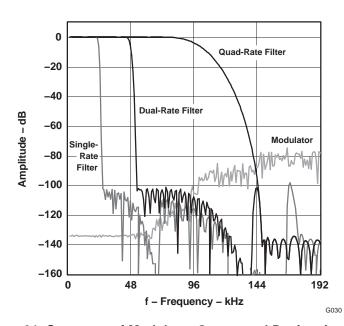


Figure 31. Spectrum of Modulator Output and Decimation Filter



# **PRINCIPLES OF OPERATION (continued)**

#### SYSTEM CLOCK INPUT

The PCM1804 supports  $128 \, f_S$ ,  $192 \, f_S$  (only in master mode at quad rate),  $256 \, f_S$ ,  $384 \, f_S$ ,  $512 \, f_S$ , and  $768 \, f_S$  as a system clock, where  $f_S$  is the audio sampling frequency. The system clock must be supplied on SCKI (pin 18). Table 3 shows the relationship of typical sampling frequency and the system clock frequency, and Figure 32 shows system clock timing. In master mode, the system clock rate is selected by OSR2 (pin 11), OSR1 (pin 10), and OSR0 (pin 9) as shown in Table 1. In slave mode, the system clock rate is automatically detected. In DSD mode, OSR2 (pin 11), OSR1 (pin 10), OSR0 (pin 9), and the system clock frequency are fixed as shown in Table 1 and Table 3.

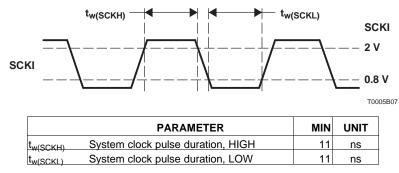


Figure 32. System Clock Input Timing

#### **POWER-ON AND RESET FUNCTIONS**

The PCM1804 has both an internal power-on-reset circuit and  $\overline{RST}$  (pin 19). For internal power-on reset, initialization (reset) is performed automatically at the time when the power supply  $V_{DD}$  exceeds 2 V (typical) and  $V_{CC}$  exceeds 4 V (typical).  $\overline{RST}$  accepts external forced reset, and a low level on  $\overline{RST}$  initiates the reset sequence. Because an internal pulldown resistor terminates  $\overline{RST}$ , no connection of  $\overline{RST}$  is equivalent to a low-level input. Because the system clock is used as a clock signal for the reset circuit, the system clock must be supplied as soon as power is supplied; more specifically, at least three system clocks are required prior to  $V_{DD} > 2$  V,  $V_{CC} > 4$  V, and  $\overline{RST} = \text{high}$ . While  $V_{DD} < 2$  V (typical),  $V_{CC} < 4$  V (typical), or  $\overline{RST} = \text{low}$ , and  $1/f_S$  (maximum) count after  $V_{DD} > 2$  V (typical),  $V_{CC} > 4$  V (typical) and  $\overline{RST} = \text{high}$ , the PCM1804 stays in the reset state and the digital output is forced to zero. The digital output is valid after the reset state is released and the time of 1116/ $f_S$  has passed. Figure 33 and Figure 34 illustrate the internal power-on-reset and external-reset timing, respectively. Figure 35 illustrates the digital output for power-on reset and  $\overline{RST}$  control. The PCM1804 needs  $\overline{RST} = \text{low}$  when control pins are changed or in slave mode when SCKI. LRCK, and BCK are changed.

#### **POWER-DOWN FUNCTION**

The PCM1804 has a power-down feature that is controlled by RST (pin 19). Entering the power-down mode is done by keeping the RST input level low for more than 65536/f<sub>S</sub>. In the master mode, the SCKI (pin 18) is used as the clock signal for the power-down counter. While in the slave mode, SCKI (pin 18) and LRCK (pin 17) are used as the clock signal. The clock(s) must be supplied until the power-down sequence completes. As soon as RST goes high, the PCM1804 starts the reset-release sequence described in the *Power-On and Reset Functions* section.

#### **OVERSAMPLING RATIO**

The oversampling ratio is selected by OSR2 (pin 11), OSR1 (pin 10), and OSR0 (pin 9) as shown in Table 1 and Table 2. The PCM1804 needs  $\overline{RST}$  = low when logic levels on the OSR2, OSR1, and OSR0 pins are changed.



Table 1. Oversampling Ratio in Master Mode

OSR2	OSR1	OSR0	OVERSAMPLING RATIO	SYSTEM CLOCK RATE
Low	Low	Low	Single rate (× 128 f <sub>S</sub> )	768 f <sub>S</sub>
Low	Low	High	Single rate (× 128 f <sub>S</sub> )	512 f <sub>S</sub>
Low	High	Low	Single rate (× 128 f <sub>S</sub> )	384 f <sub>S</sub>
Low	High	High	Single rate (× 128 f <sub>S</sub> )	256 f <sub>S</sub>
High	Low	Low	Dual rate (× 64 f <sub>S</sub> )	384 f <sub>S</sub>
High	Low	High	Dual rate (× 64 f <sub>S</sub> )	256 f <sub>S</sub>
High	High	Low	Quad rate (× 32 f <sub>S</sub> )	192 f <sub>S</sub>
High	High	High	Quad rate (× 32 f <sub>S</sub> )	128 f <sub>S</sub>
High	Low	Low	DSD mode (× 64 f <sub>S</sub> )	384 f <sub>S</sub>
High	Low	High	DSD mode (× 64 f <sub>S</sub> )	256 f <sub>S</sub>

**Table 2. Oversampling Ratio in Slave Mode** 

OSR2	OSR1	OSR0	OVERSAMPLING RATIO	SYSTEM CLOCK RATE
Low	Low	Low	Single rate (× 128 f <sub>S</sub> )	Automatically detected
Low	Low	High	Dual rate (× 64 f <sub>S</sub> )	Automatically detected
Low	High	Low	Quad rate (× 32 f <sub>S</sub> ) <sup>(1)</sup>	Automatically detected
Low	High	High	Reserved	-
High	Low	Low	Reserved	-
High	Low	High	Reserved	-
High	High	Low	Reserved	-
High	High	High	Reserved	-

<sup>(1)</sup> Only at the 128-f<sub>S</sub> system clock rate

**Table 3. Sampling Frequency and System Clock Frequency** 

OVERSAMPLING RATIO	SAMPLING	SYSTEM CLOCK FREQUENCY (MHz)						
OVERSAMPLING RATIO	FREQUENCY (kHz)	128 f <sub>S</sub>	192 f <sub>S</sub> <sup>(1)</sup>	256 f <sub>S</sub>	384 f <sub>S</sub>	512 f <sub>S</sub>	768 f <sub>S</sub>	
	32	_	-	8.192	12.288	16.384	24.576	
Single rate <sup>(2)</sup>	44.1	_	-	11.2896	16.9344	22.5792	33.8688	
	48	_	-	12.288	18.432	24.576	36.864	
Dual rate <sup>(3)</sup>	88.2	_	_	22.5792	33.8688	-	-	
Dual fale **/	96	-	_	24.576	36.864	-	_	
Quad rate <sup>(4)</sup>	176.4	22.5792	33.8688	-	-	-	-	
Quad rate V	192	24.576	36.864	-	-	-	-	
DSD mode <sup>(3)</sup>	44.1	_	_	11. 2896	16.9344	-	-	

- Only available in master mode at the quad rate
- Modulator is running at 128 f<sub>s</sub>. Modulator is running at 64 f<sub>s</sub>. Modulator is running at 32 f<sub>s</sub>.

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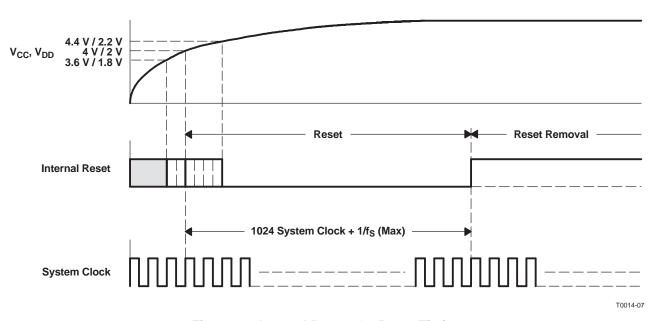


Figure 33. Internal Power-On-Reset Timing

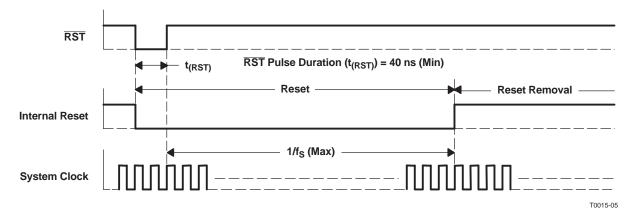
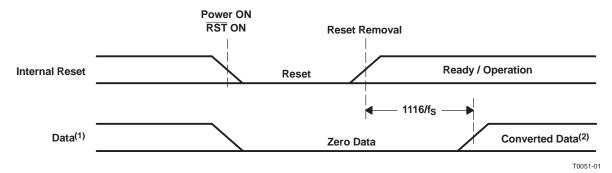


Figure 34. External Reset Timing



- (1) In the DSD mode, DSDL is also controlled like DSDR.
- (2) The HPF transient response appears initially.

Figure 35. ADC Digital Output for Power-On Reset and RST Control



#### **AUDIO DATA INTERFACE**

The PCM1804 interfaces the audio system through BCK/DSDL (pin 16), LRCK/DSDBCK (pin 17), and DATA/DSDR (pin 15). The PCM1804 needs  $\overline{RST}$  = low when in the interface mode and/or the data format are changed.

#### **INTERFACE MODE**

The PCM1804 supports master mode and slave mode as interface modes, which are selected by S/M (pin 8) as shown in Table 4. In master mode, the PCM1804 provides the timing of the serial audio data communications between the PCM1804 and the digital audio processor or external circuit. While in slave mode, the PCM1804 receives the timing for data transfer from an external controller. Slave mode is not available for DSD.

**Table 4. Interface Mode** 

S/M	MODE
Low	Master mode
High	Slave mode

#### **DATA FORMAT**

The PCM1804 supports four audio data formats in both master and slave modes, and these data formats are selected by FMT0 (pin 6) and FMT1 (pin 7) as shown in Table 5.

**Table 5. Data Format** 

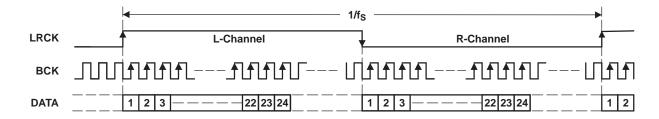
FMT1	FMT0	FORMAT	MASTER	SLAVE
Low	Low	PCM, left-justified, 24-bit	Yes	Yes
Low	High	PCM, I <sup>2</sup> S, 24-bit	Yes	Yes
High	Low	PCM, standard, 24-bit	Yes	Yes
High	High	DSD	Yes	ı



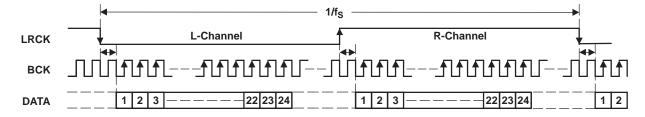
#### INTERFACE TIMING FOR PCM

Figure 36 through Figure 38 illustrate the interface timing for PCM.

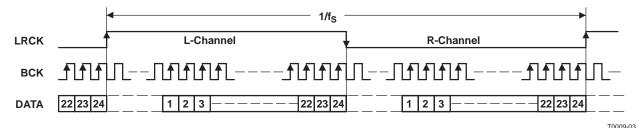
(1) Left-Justified Data Format; L-Channel = High, R-Channel = Low



(2) I<sup>2</sup>S Data Format; L-Channel = Low, R-Channel = High



(3) Standard Data Format; L-Channel = High, R-Channel = Low

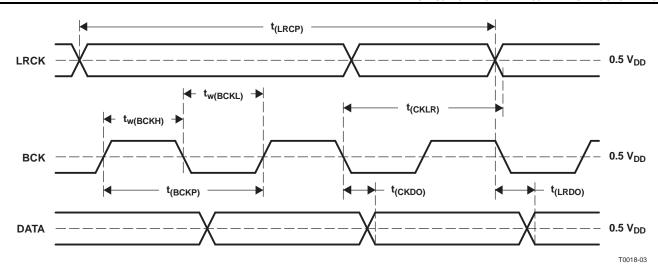


NOTE: LRCK and BCK work as outputs in master mode and as inputs in slave mode.

Figure 36. Audio Data Format for PCM

22



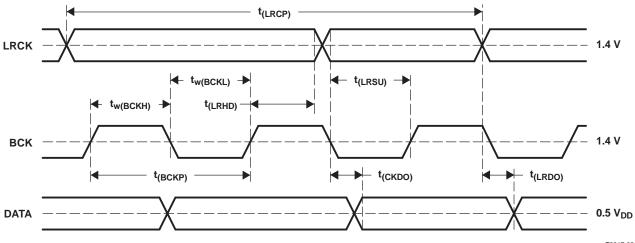


	PARAMETERS	MIN	TYP	MAX	UNIT
t <sub>(BCKP)</sub>	BCK period		1/(64 f <sub>S</sub> ) <sup>(3</sup>		
t <sub>w(BCKH)</sub>	BCK pulse duration, HIGH	32			ns
t <sub>w(BCKL)</sub>	BCK pulse duration, LOW	32			ns
t <sub>(CKLR)</sub>	Delay time, BCK falling edge to LRCK valid	-5		15	ns
t <sub>(LRCP)</sub>	LRCK period		1/f	: S	
t <sub>(CKDO)</sub>	Delay time, BCK falling edge to DATA valid	-5		15	ns
t <sub>(LRDO)</sub>	Delay time, LRCK edge to DATA valid	-5		15	ns
t <sub>r</sub>	Rising time of all signals <sup>(1)(2)</sup>			10	ns
t <sub>f</sub>	Falling time of all signals <sup>(1)(2)</sup>			10	ns

- (1) Rising and falling times are measured from 10% to 90% of IN/OUT signal swing.
- (2) Load capacitance of all signals is 10 pF.
- (3)  $t_{(BCKP)}$  is fixed at 1/(64  $f_S$ ) in case of master mode.

Figure 37. Audio Data Interface Timing for PCM (Master Mode: LRCK and BCK Work as Outputs)





T0017-03

	PARAMETERS	MIN	TYP	MAX	UNIT
t <sub>(BCKP)</sub>	BCK period	1/(64 f <sub>S</sub> )		1/(48 f <sub>S</sub> )	
t <sub>w(BCKH)</sub>	BCK pulse duration, HIGH	32			ns
t <sub>w(BCKL)</sub>	BCK pulse duration, LOW	32			ns
t <sub>(LRSU)</sub>	LRCK setup time to BCK rising edge	12			ns
t <sub>(LRHD)</sub>	LRCK hold time to BCK rising edge	12			ns
t <sub>(LRCP)</sub>	LRCK period		1/f <sub>S</sub>		
t <sub>(CKDO)</sub>	Delay time, BCK falling edge to DATA valid	5		25	ns
t <sub>(LRDO)</sub>	Delay time, LRCK edge to DATA valid	5		25	ns
t <sub>r</sub>	Rising time of all signals <sup>(1)(2)</sup>			10	ns
t <sub>f</sub>	Falling time of all signals <sup>(1)(2)</sup>			10	ns

- (1) Rising and falling times are measured from 10% to 90% of IN/OUT signals swing.
- (2) Load capacitance of DATA/DSDR signal is 10 pF.

Figure 38. Audio Data Interface Timing for PCM (Slave Mode: LRCK and BCK Work as Inputs)

# INTERFACE TIMING FOR DSD

Figure 39 and Figure 40 illustrate the interface timing for DSD.

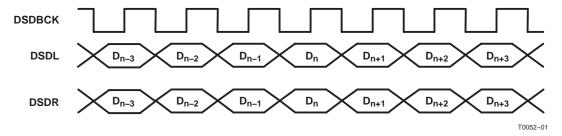
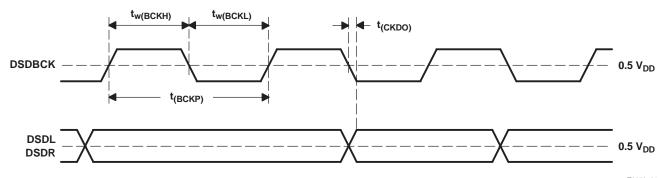


Figure 39. Audio Data Format





T0053-01

	PARAMETERS	MIN	TYP	MAX	UNIT
t <sub>(BCKP)</sub>	DSDBCK period		354		ns
t <sub>w(BCKH)</sub>	DSDBCK pulse duration, HIGH		177		ns
t <sub>w(BCKL)</sub>	DSDBCK pulse duration, LOW		177		ns
t <sub>(CKDO)</sub>	Delay time DSDBCK falling edge to DSDL, DSDR valid	<b>-</b> 5		15	ns
t <sub>r</sub>	Rising time of all signals <sup>(1)(2)</sup>			10	ns
t <sub>f</sub>	Falling time of all signals <sup>(1)(2)</sup>			10	ns

- (1) Rising and falling times are measured from 10% to 90% of IN/OUT signal swing.
- (2) Load capacitance of DSDBCK/DSDL/DSDR signal is 10 pF.

Figure 40. Audio Data Interface Timing for DSD (Master Mode Only)

#### SYNCHRONIZATION WITH DIGITAL AUDIO SYSTEM FOR PCM

In slave mode, the PCM1804 operates under LRCK synchronized with the system clock SCKI. The PCM1804 does not need a specific phase relationship between LRCK and SCKI, but does require the synchronization of LRCK and SCKI.

If the relationship between LRCK and SCKI changes more than ±6 BCK during one sample period due to LRCK or SCKI jitter, internal operation of the ADC halts within 1/f<sub>S</sub> and digital output is forced into BPZ code until resynchronization between LRCK and SCKI is completed.

In case of changes less than ±5 BCK, resynchronization does not occur and the previously described digital output control and discontinuity do not occur.

Figure 41 illustrates ADC digital output for loss of synchronization and resynchronization. During undefined data, the PCM1804 may generate some noise in the audio signal. Also, the transitions of normal to undefined data and undefined or zero data to normal cause a discontinuity of data on the digital output. This can generate noise in the audio signal. In master mode, synchronization loss never occurs.

#### HIGH-PASS FILTER (HPF) BYPASS CONTROL FOR PCM

The built-in function for dc component rejection can be bypassed by BYPAS (pin 12) control. In bypass mode, the dc component of the input analog signal and the internal dc offset are also converted and output in the digital output data.

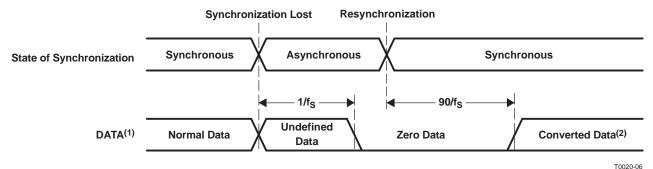
#### **HPF Bypass Control**

BYPAS PIN	HPF MODE
Low	Normal (high-pass) mode
High	Bypass (through) mode



#### **OVERFLOW FLAG FOR PCM**

The PCM1804 has two overflow flag pins, OVFR (pin 20) and OVFL (pin 21). The pins go to high as soon as the analog input goes across the full-scale range. The high level is held for 1.016 s at maximum, and returns to low if the analog input does not go across the full-scale range for the period.



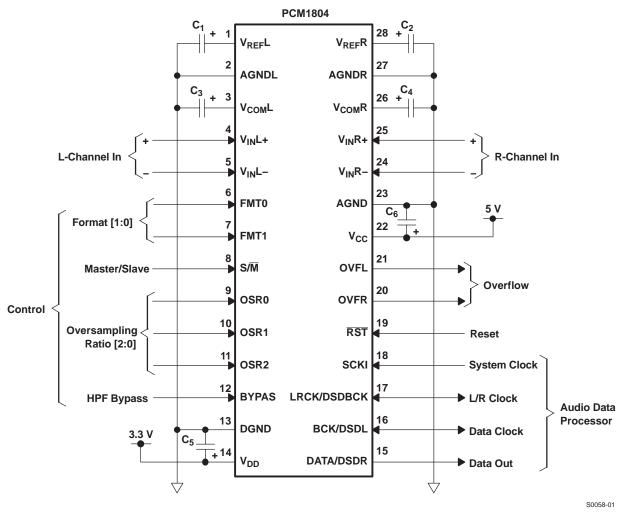
- (1) Applies only for slave mode; the loss of synchronization never occurs in master mode.
- (2) The HPF transient response appears initially.

Figure 41. ADC Digital Output for Loss of Synchronization and Resynchronization



# TYPICAL CIRCUIT CONNECTION DIAGRAM

Figure 42 illustrates a typical circuit connection diagram in the PCM data format operation.

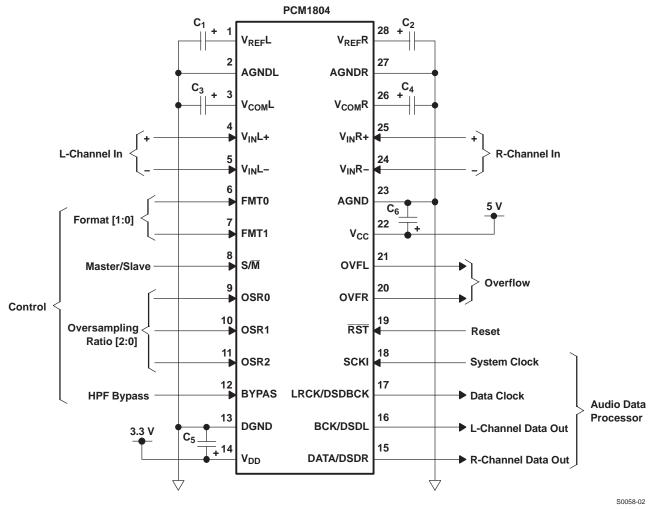


- A. C1, C2, C5, and C6: Bypass capacitors, 0.1-µF ceramic and 10-µF tantalum, depending on layout and power supply
- B. C3, C4: Bypass capacitor, 0.1-µF tantalum, depending on layout and power supply

Figure 42. Typical Circuit Connection Diagram for PCM



Figure 43 illustrates a typical circuit connection diagram in the DSD data format operation.



- A. C1, C2, C5, and C6: Bypass capacitors, 0.1-µF ceramic and 10-µF tantalum, depending on layout and power supply
- B. C3 and C4: Bypass capacitors, 0.1-µF tantalum, depending on layout and power supply

Figure 43. Typical Circuit Connection Diagram for DSD



#### **APPLICATION INFORMATION**

#### **BOARD DESIGN AND LAYOUT CONSIDERATIONS**

#### $V_{CC}$ , $V_{DD}$ Pins

The digital and analog power supply lines to the PCM1804 should be bypassed to the corresponding ground pins with 0.1-µF ceramic and 10-µF tantalum capacitors placed as close to the pins as possible to maximize the dynamic performance of the ADC. Although the PCM1804 has two power lines to maximize the potential of dynamic performance, using one common power supply is recommended to avoid unexpected power-supply trouble like latch-up or power-supply sequence.

# **VIN Pins**

Use of  $0.01-\mu F$  film capacitors between  $V_{IN}L+$  and  $V_{IN}L-$  and between  $V_{IN}R+$  and  $V_{IN}R-$  is strongly recommended to remove higher-frequency noise from the delta-sigma input section.

#### V<sub>REF</sub>X, V<sub>COM</sub>X Inputs

Use 0.1- $\mu$ F ceramic and 10- $\mu$ F tantalum capacitors between V<sub>REF</sub>L, V<sub>REF</sub>R, and corresponding AGNDx, to ensure low-source impedance at ADC references. Use 0.1- $\mu$ F tantalum capacitors between V<sub>COM</sub>L, V<sub>COM</sub>R and corresponding AGNDx to ensure low source impedance of common voltage. These capacitors should be located as close as possible to the V<sub>REF</sub>L, V<sub>REF</sub>R, V<sub>COM</sub>L, and V<sub>COM</sub>R pins to reduce dynamic errors on references and common voltage. The dc voltage level of these pins is 2.5 V.

#### DATA/DSDR, BCK/DSDL, and LRCK/DSDBCK Pins

The DATA/DSDR, BCK/DSDL, and LRCK/DSDBCK pins in master mode have large load drive capability. Locating the buffer near the PCM1804 and minimizing the load capacitance, minimizes the digital-analog crosstalk and maximizes the dynamic performance of the ADC.

#### **System Clock**

The quality of the system clock can influence dynamic performance, as the PCM1804 operates based on a system clock. Therefore, it might be necessary to consider the system clock duty, jitter, and the time difference between system clock transition and BCK/DSDL or LRCK/DSDBCK transition in slave mode.

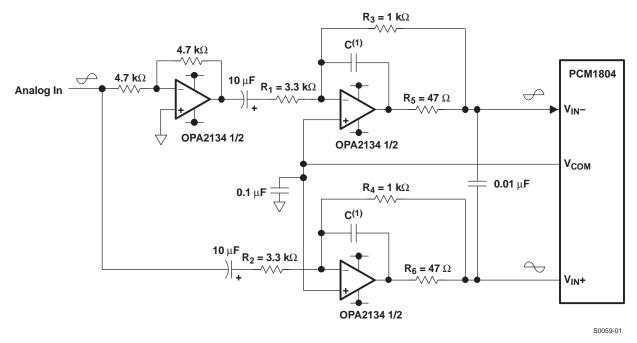
#### **Reset Control**

If capacitors larger than 10  $\mu$ F are used on  $V_{REF}L$  and  $V_{REF}R$ , an external reset control with a delay time corresponding to the  $V_{REF}L$  and  $V_{REF}R$  response is required. Also, it works as a power-down control.

#### APPLICATION CIRCUIT FOR SINGLE-ENDED INPUT

An application diagram for a single-ended input circuit is shown in Figure 44. The maximum signal input voltage and differential gain of this circuit is designed as Vinmax = 8.28 Vpp, Ad = 0.3. Differential gain (Ad) is given by R3/R1(R4/R2) in a circuit configured as a normal inverted-gain amplifier. Resistor R5(R6) in the feedback loop gives low-impedance drive operation and noise filtering for the analog input of the PCM1804. The circuit technique using R5(R6) is recommended.





(1) A capacitor value of 1800 pF is recommended, unless an input signal greater than -6 dBFS at 100 kHz or higher is applied in the DSD mode. In that case, 3300 pF is recommended.

Figure 44. Application Circuit for Single-Ended Input Circuit (PCM)

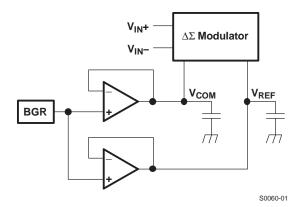


Figure 45. Equivalent Circuit of Internal Reference (V<sub>COM</sub>, V<sub>REF</sub>)





13-Apr-2012

#### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
PCM1804DB	ACTIVE	SSOP	DB	28	47	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
PCM1804DBG4	ACTIVE	SSOP	DB	28	47	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
PCM1804DBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
PCM1804DBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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# TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

# QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1804DBR	SSOP	DB	28	2000	330.0	17.4	8.5	10.8	2.4	12.0	16.0	Q1





#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1804DBR	SSOP	DB	28	2000	336.6	336.6	28.6

# DB (R-PDSO-G\*\*)

# PLASTIC SMALL-OUTLINE

#### **28 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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