SCAS174A - MAY 1991 - REVISED APRIL 1996

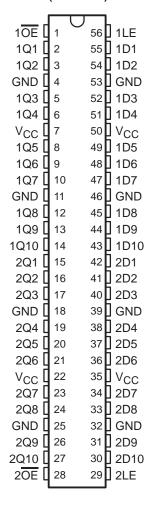
- Members of the Texas Instruments Widebus™ Family
- Inputs Are TTL-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Provide Extra Bus Driving/Latches
  Necessary for Wider Address/Data Paths or
  Buses With Parity
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Thin Shrink Small-Outline (DGG) Packages, 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings, and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings

#### description

These 20-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'ACT16841 can be used as two 10-bit latches or one 20-bit latch. The 20 latches are transparent D-type. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

54ACT16841 . . . WD PACKAGE 74ACT16841 . . . DGG OR DL PACKAGE (TOP VIEW)



A buffered output-enable ( $1\overline{OE}$  or  $2\overline{OE}$ ) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

OE does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.



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### description (continued)

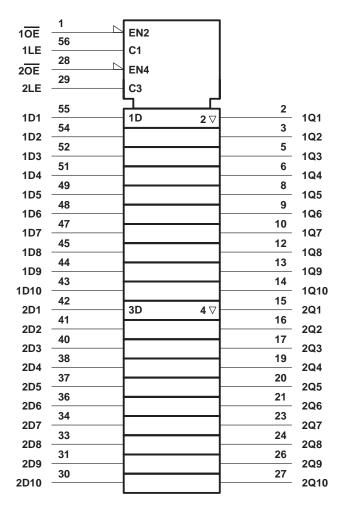
The 74ACT16841 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16841 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16841 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each 10-bit latch)

	INPUTS		OUTPUT
OE	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	Q <sub>0</sub>
Н	Χ	Χ	Z

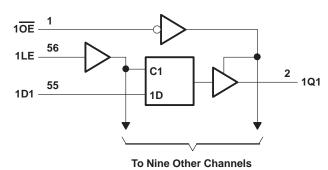
## logic symbol†

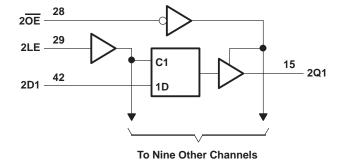


<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



### logic diagram (positive logic)





## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)–0.	5 V to $V_{CC}$ + 0.5 V
Output voltage range, V <sub>O</sub> (see Note 1)	5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through V <sub>CC</sub> or GND	±500 mA
Maximum package power dissipation at T <sub>A</sub> = 55°C (in still air) (see Note 2): DGG package	e 1 W
DL package	1.4 W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 3)

		54.	ACT1684	41	74	ACT1684	11	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2		4	2			V
V <sub>IL</sub>	Low-level input voltage		Š	0.8			0.8	V
VI	Input voltage	0	70 A	VCC	0		VCC	V
Vo	Output voltage	0	7	VCC	0		VCC	V
IOH	High-level output current		3	-24			-24	mA
loL	Low-level output current	, C	5	24			24	mA
Δt/Δν	Input transition rise or fall rate	0		10	0		10	ns/V
TA	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

 $<sup>2. \</sup>quad \text{The maximum package power dissipation is calculated using a junction temperature of } 150\,^{\circ}\text{C} \text{ and a board trace length of } 750\,\text{mils}.$ 

# 54ACT16841, 74ACT16841 20-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DARAMETER	TEST CONDITIONS	V	T,	Δ = 25°C		54ACT	16841	74ACT	16841	UNIT
PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
	10.1 - 50.11A	4.5 V	4.4			4.4		4.4		
	I <sub>OH</sub> =-50 μA	5.5 V	5.4			5.4		5.4		
Voн	I <sub>OH</sub> = -24 mA	4.5 V	3.94			3.8		3.8		V
	10H = -24 111A	5.5 V	4.94			4.8	_	4.8		
	I <sub>OH</sub> = -75 mA <sup>†</sup>	5.5 V				3.85	18	3.85		
	I <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1		0.1	
	ΙΟΣ = 30 μΑ	5.5 V			0.1	4	0.1		0.1	
VOL	I <sub>OL</sub> = 24 mA	4.5 V			0.36	Ό,	0.44		0.44	V
	IOL = 24 IIIA	5.5 V			0.36	90	0.44		0.44	
	I <sub>OL</sub> = 75 mA <sup>†</sup>	5.5 V				d'a	1.65		1.65	
lį	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1		±1	μΑ
loz	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5		±5	μΑ
<sup>I</sup> CC	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		80		80	μΑ
Δl <sub>CC</sub> ‡	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			0.9		1		1	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		3						pF
Co	VO = VCC or GND	5 V		11						pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

# timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

			T <sub>A</sub> = :	25°C	54ACT	16841	74ACT	16841	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	UNII
t <sub>W</sub>	Pulse duration, LE high		4		4	4	4		ns
t <sub>su</sub>	Setup time, data before LE↓		1.5		1.5	10.01	1.5		ns
٠.	Hold time data after LE	High	3		2-30	11.	3		20
t <sub>h</sub>	Hold time, data after LE↓	Low	4.5		4.5		4.5		ns

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	T,	<b>Վ = 25°</b> C	;	54ACT	16841	74ACT	16841	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
<sup>t</sup> PLH	D	Q	4	7.1	10.3	4	11.8	4	11.8	ns
<sup>t</sup> PHL	Ь	ά	3.2	6.9	11	3.2	12.2	3.2	12.2	115
<sup>t</sup> PLH	LE	Q	4.5	7.7	11.3	4.5	12.7	4.5	12.7	ns
t <sub>PHL</sub>	LE	Q	4.3	7.8	11.4	4.3	12.7	4.3	12.7	115
<sup>t</sup> PZH	ŌĒ	Q	3.1	6.4	10.1	3.1	11.3	3.1	11.3	no
t <sub>PZL</sub>	OE	σ	3.8	7.6	12.1	3.8	13.7	3.8	13.7	ns
<sup>t</sup> PHZ	ŌĒ	Q	4	7.3	9.5	4	10.2	4	10.2	no
<sup>t</sup> PLZ	OE	ά	4	6.8	8.9	4	9.6	4	9.6	ns

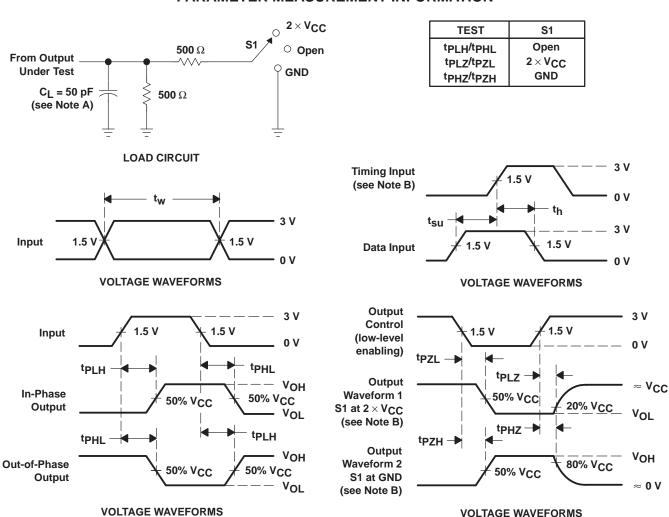


<sup>&</sup>lt;sup>‡</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

# operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

	PARAMETER	TEST CO	TYP	UNIT		
	Power dissipation capacitance	Outputs enabled	$C_1 = 50 pF$	f = 1 MHz	41	n.E
Cpd	rower dissipation capacitance	Outputs disabled	CL = 50 pr,	I = I IVIIIZ	10	pF

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_\Gamma = 3$  ns,  $t_f = 3$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms







28-Aug-2010

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
74ACT16841DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
74ACT16841DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
74ACT16841DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
74ACT16841DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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# PACKAGE MATERIALS INFORMATION

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## TAPE AND REEL INFORMATION





Α	0	Dimension designed to accommodate the component width
В	0	Dimension designed to accommodate the component length
		Dimension designed to accommodate the component thickness
٧	٧	Overall width of the carrier tape
ГР	1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ACT16841DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ACT16841DLR	SSOP	DL	56	1000	346.0	346.0	49.0

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