SCBS197D - FEBRUARY 1991 - REVISED MAY 1997

- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C
- High-Drive Outputs (-32-mA I_{OH}, 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (NT) and Ceramic (JT) DIPs

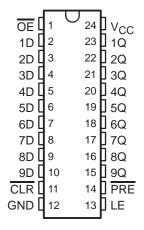
description

The 'ABT843 9-bit latches are designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

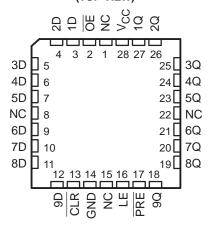
The nine transparent D-type latches provide true data at the outputs.

A buffered output-enable (\overline{OE}) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

SN54ABT843...JT OR W PACKAGE SN74ABT843...DB, DW, OR NT PACKAGE (TOP VIEW)



SN54ABT843 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

OE does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT843 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT843 is characterized for operation from –40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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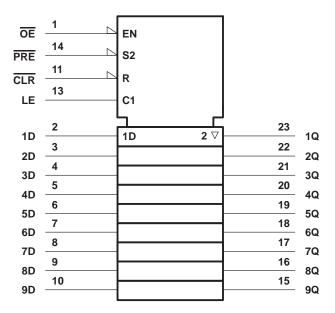
SN54ABT843, SN74ABT843 9-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS197D - FEBRUARY 1991 - REVISED MAY 1997

FUNCTION TABLE

	INPUTS									
PRE	CLR	OE	LE	D	Q					
L	Х	L	Χ	Χ	Н					
Н	L	L	X	X	L					
Н	Н	L	Н	L	L					
Н	Н	L	Н	Н	н					
Н	Н	L	L	Χ	Q ₀					
Х	X	Н	Χ	Χ	Z					

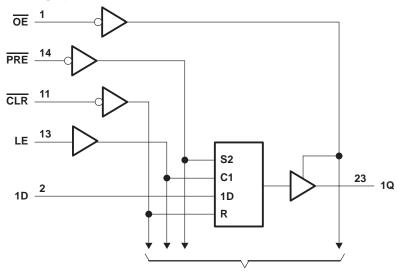
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, NT, and W packages.



logic diagram (positive logic)



To Eight Other Channels

Pin numbers shown are for the DB, DW, JT, NT, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		
Input voltage range, V _I (see Note 1)		–0.5 V to 7 V
Voltage range applied to any output in the high	or power-off state, VO	
Current into any output in the low state, IO: SNS	54ABT843	96 mA
SN7	74ABT843	128 mA
Input clamp current, I _{IK} (V _I < 0)		–18 mA
Output clamp current, I _{OK} (V _O < 0)		
Package thermal impedance, θ _{JA} (see Note 2):	DB package	104°C/W
	DW package	81°C/W
	NT package	67°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.



SN54ABT843, SN74ABT843 9-BIT BUS-INTERFACE D-TYPE LATCHES **WITH 3-STATE OUTPUTS**

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recommended operating conditions (see Note 3)

		SN54A	BT843	SN74A	BT843	UNIT
		MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2		2		V
VIL	Low-level input voltage		0.8		0.8	V
٧ _I	Input voltage	0	VCC	0	VCC	V
IOH	High-level output current		-24		-32	mA
loL	Low-level output current		48		64	mA
Δt/Δν	Input transition rise or fall rate		5		5	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		TEST CONDITION	10	Т	A = 25°0	;	SN54A	BT843	SN74A	BT843	
PARAMETER		TEST CONDITION	NS	MIN	TYP [†]	MAX	MIN	MAX	MIN	MAX	UNIT
VIK	$V_{CC} = 4.5 \text{ V},$	$I_{I} = -18 \text{ mA}$				-1.2		-1.2		-1.2	V
	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -3 mA					2.5		2.5		
Vou	$V_{CC} = 5 V$,	$I_{OH} = -3 \text{ mA}$		3			3		3		V
VOH	V _{CC} = 4.5 V						2				v
	VCC = 4.5 V	$I_{OH} = -32 \text{ mA}$		2*					2		
Va. Va	V _{CC} = 4.5 V	$I_{OL} = 48 \text{ mA}$						0.55			V
V _{OL} V _{CC} = 4.5 V		I _{OL} = 64 mA			0.55*				0.55		
V _{hys}					100						mV
Ι _Ι	$V_{CC} = 5.5 \text{ V},$	$V_I = V_{CC}$ or GND				±1		±1		±1	μΑ
lozh [‡]	$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.7 \text{ V}$				10		10		10	μΑ
l _{OZL} ‡	$V_{CC} = 5.5 \text{ V},$	V _O = 0.5 V				-10		-10		-10	μΑ
l _{off}	$V_{CC} = 0$,	V_I or $V_O \le 4.5 \text{ V}$				±100				±100	μΑ
ICEX	$V_{CC} = 5.5 \text{ V},$	$V_0 = 5.5 \text{ V}$	Outputs high			50		50		50	μΑ
I _O §	$V_{CC} = 5.5 \text{ V},$	V _O = 2.5 V		-50	-140	-180	-50	-180	-50	-180	mA
		0	Outputs high		1	250		250		250	μΑ
ICC	V _{CC} = 5.5 V, I _C V _I = V _{CC} or GI		Outputs low		24	34		34		34	mA
	V = VCC 01 GIAD		Outputs disabled		0.5	250		250		250	μΑ
ΔI _{CC} ¶	V _{CC} = 5.5 V, O Other inputs at	one input at 3.4 V, V _{CC} or GND				1.5		1.5		1.5	mA
Ci	V _I = 2.5 V or 0.5 V				4					·	pF
Co	$V_0 = 2.5 \text{ V or } 0$).5 V			7						pF

^{*} On products compliant to MIL-PRF-38535, this parameter does not apply.



[†] All typical values are at $V_{CC} = 5 \text{ V}$.

[‡] The parameters IOZH and IOZL include the input leakage current.

[§] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[¶] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 1 and 2)

				V _{CC} =	= 5 V, 25°C	SN54A	BT843	SN74A	BT843	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
		CLR low		5.5		5.5		5.5		
t _W Pulse duration	Pulse duration	PRE low	4.5		4.5		4.5		ns	
		LE low		3.3		3.3		3.4		
		Data before LE↓	Low	2.5		2.5		2.5		
١.	Setup time		High	3		3		3		
t _{su}	Setup time	PRE inactive	1.6		1.6		1.6		ns	
		CLR inactive		2		2		2		
.	Hold time, data after LE↓	High		1		1		1		no
t _h	⊓oiu time, uata arter LE↓	Low		1.5†		2.3†		1.5†		ns

[†]This data sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			SN54ABT843		SN74ABT843		UNIT
	(1141-01)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
^t PLH	D	Q	1.2†	3.8	5.2	1.2†	7.8	1.2†	6.7†	20
^t PHL	D	Q	1.5†	3.4	6.3	1.5†	7.3	1.5†	7.2	ns
^t PLH	LE	Q	1.7†	4.4	5.6	1.7†	8.3	1.7†	7.2†	ns
^t PHL	LE	Q	1.9†	4.1	6.3	1.3†	7.2	1.9†	6.9	115
^t PLH	PRE	Q	2.2	5	6.2	2.2	8.3	2.2	7.4	ns
^t PHL	PRE	Q	2.1†	4.1	6.5	2.1†	7.5	2.1†	7.2	113
^t PLH	<u> </u>	Q	2†	4.4	6.3	2†	7.6	2†	7.1	ns
^t PHL	CLR	Q	1.9†	4.5	6.8	1.9†	8.1	1.9†	8	115
^t PZH		0	1	3.4	4.5†	1	6.4	1	5.7	
tPZL	ŌĒ	Q	2	4.3	5.7†	2	6.6	2	6.5	ns
^t PHZ	ŌĒ	0	2.4†	4.9	6.2	2.4†	7.3	2.4†	6.8	no
tPLZ	OE .	Q	1.5†	4.2	6.3	1.5†	7	1.5†	5.9†	ns

[†] This data sheet limit may vary among suppliers.



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recovery-time waveform

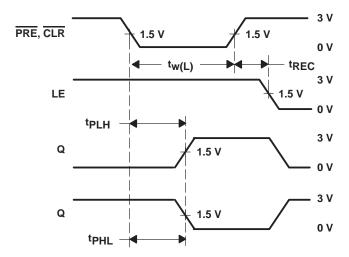
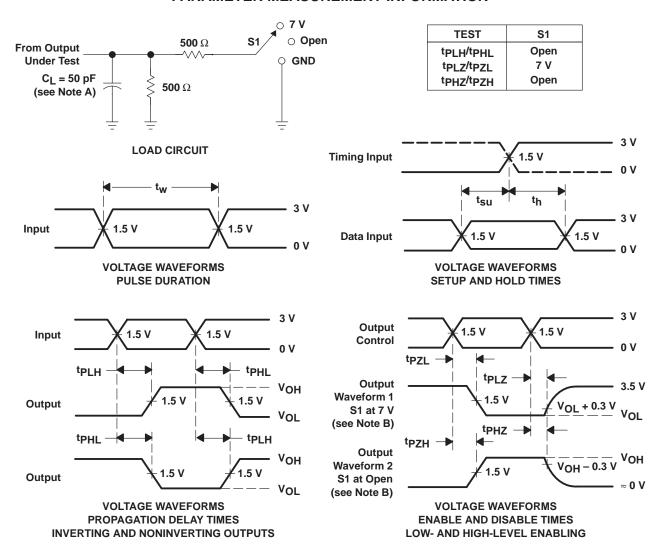


Figure 1. CLR and PRE Pulse Duration, CLR and PRE to Output Delay, and CLR and PRE to Latch-Enable Recovery Time



PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

16-Jan-2012

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-9571201Q3A	ACTIVE	LCCC	FK	28	1	TBD	Call TI	Call TI	
5962-9571201QKA	ACTIVE	CFP	W	24	1	TBD	Call TI	Call TI	
5962-9571201QLA	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Call TI	
SN74ABT843DBLE	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI	
SN74ABT843DBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT843DBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT843DBRG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT843DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT843DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT843DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT843DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT843DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT843DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT843NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ABT843NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SNJ54ABT843FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54ABT843JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	
SNJ54ABT843W	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.



PACKAGE OPTION ADDENDUM

16-Jan-2012

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54ABT843, SN74ABT843:

Catalog: SN74ABT843

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Military: SN54ABT843

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT843DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74ABT843DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT843DBR	SSOP	DB	24	2000	346.0	346.0	33.0
SN74ABT843DWR	SOIC	DW	24	2000	346.0	346.0	41.0

JT (R-GDIP-T**)

24 LEADS SHOWN

CERAMIC DUAL-IN-LINE

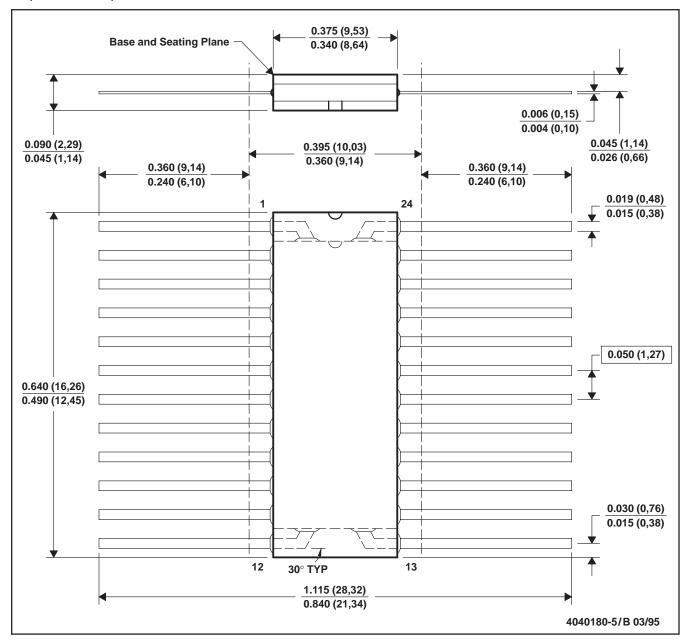


NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
 - E. Index point is provided on cap for terminal identification only.



FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

The 28 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



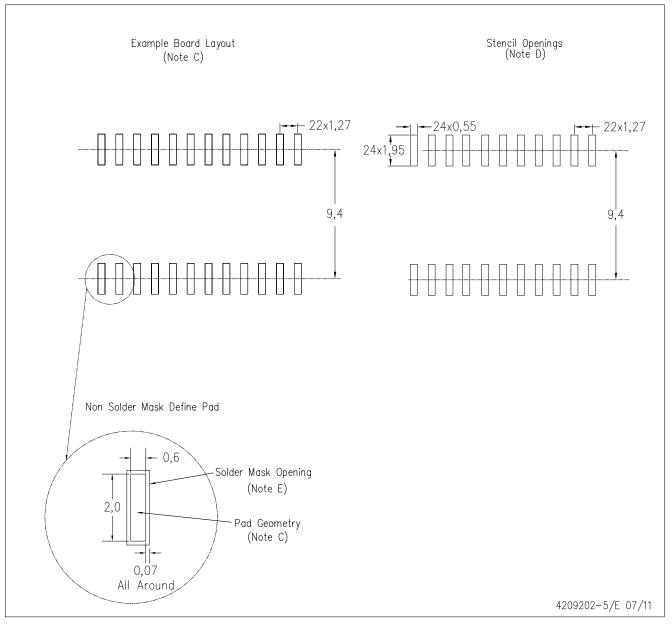
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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