

SINGLE-ENDED, ANALOG-INPUT 24-BIT, 96-kHz STEREO A/D CONVERTER

Check for Samples: [PCM1808-Q1](#)

FEATURES

- Qualified for Automotive Applications
- 24-Bit Delta-Sigma Stereo A/D Converter
- Single-Ended Voltage Input: 3 V_{p-p}
- High Performance:
 - THD + N: –93 dB (Typical)
 - SNR: 99 dB (Typical)
 - Dynamic Range: 99 dB (Typical)
- Oversampling Decimation Filter:
 - Oversampling Frequency: ×64
 - Pass-Band Ripple: ±0.05 dB
 - Stop-Band Attenuation: –65 dB
 - On-Chip High-Pass Filter: 0.91 Hz (48 kHz)
- Flexible PCM Audio Interface
 - Master/Slave Mode Selectable
 - Data Formats: 24-Bit I²S, 24-Bit Left-Justified
- Power Down and Reset by Halting System Clock
- Analog Antialias LPF Included
- Sampling Rate: 8 kHz–96 kHz
- System Clock: 256 f_S, 384 f_S, 512 f_S

- Dual Power Supplies:
 - 5-V for Analog
 - 3.3-V for Digital
- Package: 14-Pin TSSOP

DESCRIPTION

The PCM1808-Q1 is high-performance, low-cost, single-chip, stereo analog-to-digital converter with single-ended analog voltage input. The PCM1808-Q1 uses a delta-sigma modulator with 64-times oversampling and includes a digital decimation filter and high-pass filter that removes the dc component of the input signal. For various applications, the PCM1808-Q1 supports master and slave mode and two data formats in serial audio interface.

The PCM1808-Q1 supports the power-down and reset function by means of halting the system clock.

The PCM1808-Q1 is suitable for wide variety of cost-sensitive consumer applications where good performance and operation with a 5-V analog supply and 3.3-V digital supply is required. The PCM1808-Q1 is fabricated using a highly advanced CMOS process and is available in a small, 14-pin TSSOP package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

System Two, Audio Precision are trademarks of Audio Precision, Inc.
All other trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

	PCM1808-Q1
Analog supply voltage, V_{CC}	–0.3 V to 6.5 V
Digital supply voltage, V_{DD}	–0.3 V to 4 V
Ground voltage differences, AGND, DGND	±0.1 V
Digital input voltage, LRCK, BCK, DOUT	–0.3 V to ($V_{DD} + 0.3$ V) < 4 V
Digital input voltage, SCKI, MD0, MD1, FMT	–0.3 V to 6.5 V
Analog input voltage, V_{INL} , V_{INR} , V_{REF}	–0.3 V to ($V_{CC} + 0.3$ V) < 6.5 V
Input current (any pins except supplies)	±10 mA
Ambient temperature under bias, T_A	–40°C to 125°C
Storage temperature, T_{stg}	–55°C to 150°C
Junction temperature, T_J	150°C
Lead temperature (soldering)	260°C, 5 s
Package temperature (reflow, peak)	260°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Analog supply voltage, V_{CC}		4.5	5	5.5	V
Digital supply voltage, V_{DD}		2.7	3.3	3.6	V
Analog input voltage, full scale (–0 dB)	$V_{CC} = 5$ V		3		Vp-p
Digital input logic family		TTL compatible			
Digital input clock frequency, system clock		2.048		49.152	MHz
Digital input clock frequency, sampling clock		8		96	kHz
Digital output load capacitance				20	pF
Operating free-air temperature, T_A		–40		125	°C

ELECTRICAL CHARACTERISTICS

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, master mode, $f_S = 48\text{ kHz}$, system clock = $512 f_S$, 24-bit data, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			24		Bits
DATA FORMAT					
Audio data interface format		I ² S, left-justified			
Audio data bit length			24		Bits
Audio data format		MSB-first, 2s complement			
f_S Sampling frequency		8	48	96	kHz
System clock frequency ⁽¹⁾	256 f_S	2.048	12.288	24.576	MHz
	384 f_S	3.072	18.432	36.864	
	512 f_S	4.096	24.576	49.152	
INPUT LOGIC					
V_{IH} ⁽²⁾	Input logic level ⁽³⁾		2	V_{DD}	VDC
V_{IL} ⁽²⁾			0	0.8	
V_{IH} ^{(4) (5)}			2	5.5	
V_{IL} ^{(4) (5)}			0	0.8	
I_{IH} ⁽⁴⁾	Input logic current	$V_{IN} = V_{DD}$		± 10	μA
I_{IL} ⁽⁴⁾		$V_{IN} = 0\text{ V}$		± 10	
I_{IH} ^{(2) (5)}		$V_{IN} = V_{DD}$	65	100	
I_{IL} ^{(2) (5)}		$V_{IN} = 0\text{ V}$		± 10	
OUTPUT LOGIC					
V_{OH} ⁽⁶⁾	Output logic level ⁽³⁾	$I_{OUT} = -4\text{ mA}$	2.8		VDC
V_{OL} ⁽⁶⁾		$I_{OUT} = 4\text{ mA}$		0.5	
DC ACCURACY					
Gain mismatch, channel-to-channel			± 1	± 3	% of FSR
Gain error			± 3	± 6	% of FSR
DYNAMIC PERFORMANCE ⁽⁷⁾					
THD + N Total harmonic distortion + noise	$V_{IN} = -0.5\text{ dB}$, $f_S = 48\text{ kHz}$		-93	-87	dB
	$V_{IN} = -0.5\text{ dB}$, $f_S = 96\text{ kHz}$ ⁽⁸⁾		-87		
	$V_{IN} = -60\text{ dB}$, $f_S = 48\text{ kHz}$		-37		
	$V_{IN} = -60\text{ dB}$, $f_S = 96\text{ kHz}$ ⁽⁸⁾		-39		
Dynamic range	$f_S = 48\text{ kHz}$, A-weighted	95	99		dB
	$f_S = 96\text{ kHz}$, A-weighted ⁽⁸⁾		101		
S/N Signal-to-noise ratio	$f_S = 48\text{ kHz}$, A-weighted	95	99		dB
	$f_S = 96\text{ kHz}$, A-weighted ⁽⁸⁾		101		
Channel separation	$f_S = 48\text{ kHz}$	93	97		dB
	$f_S = 96\text{ kHz}$ ⁽⁸⁾		91		

(1) 384 f_S where $f_S = 96\text{ kHz}$, and 512 where $f_S = 48\text{ kHz}$ and 96 kHz are functionally tested. Other options are specified by design.

(2) Pins 7, 8: LRCK, BCK (Schmitt-trigger input, with 50-k Ω typical pulldown resistor, in slave mode)

(3) Specified by design

(4) Pin 6: SCKI (Schmitt-trigger input, 5-V tolerant)

(5) Pins 10–12: MD0, MD1, FMT (Schmitt-trigger input, with 50-k Ω typical pulldown resistor, 5-V tolerant)

(6) Pins 7–9: LRCK, BCK (in master mode), DOUT

(7) Analog performance specifications are tested using a System Two™ audio measurement system by Audio Precision™ with 400-Hz HPF and 20-kHz LPF in RMS mode.

(8) $f_S = 96\text{ kHz}$, system clock = $256 f_S$.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, master mode, $f_S = 48\text{ kHz}$, system clock = $512 f_S$, 24-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
Input voltage				0.6 V_{CC}		Vp-p
Center voltage (V_{REF})				0.5 V_{CC}		V
Input impedance				60		k Ω
Antialiasing filter frequency response		-3 dB		1.3		MHz
DIGITAL FILTER PERFORMANCE⁽⁹⁾						
Pass band					0.454 f_S	Hz
Stop band			0.583 f_S			Hz
Pass-band ripple					± 0.05	dB
Stop-band attenuation			-65			dB
Delay time				17.4/ f_S		
HPF frequency response		-3 dB		0.019 $f_S/1000$		
POWER SUPPLY REQUIREMENTS						
V_{CC}	Voltage range		4.5	5	5.5	VDC
V_{DD}			2.7	3.3	3.6	
I_{CC}	Supply current ⁽¹⁰⁾	$f_S = 48\text{ kHz}$, 96 kHz ⁽¹¹⁾		8.6	11	mA
		Powered down ⁽¹²⁾		1		μA
I_{DD}		$f_S = 48\text{ kHz}$		5.9	8	mA
		$f_S = 96\text{ kHz}$ ⁽¹¹⁾		10.2		mA
Power dissipation ⁽¹⁰⁾		Powered down ⁽¹²⁾		150		μA
		$f_S = 48\text{ kHz}$		62	81	mW
		$f_S = 96\text{ kHz}$ ⁽¹¹⁾		77		
		Powered down ⁽¹²⁾		500		μW
TEMPERATURE RANGE						
T_A	Operation temperature		-40		125	$^\circ\text{C}$
θ_{JA}	Thermal resistance			170		$^\circ\text{C/W}$

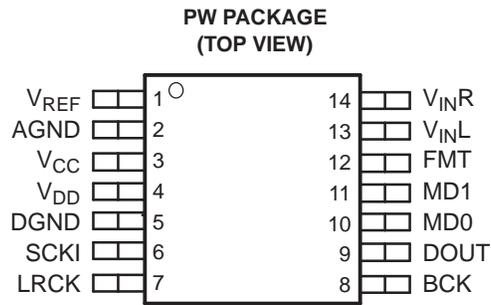
(9) Specified by design

(10) Minimum load on LRCK (pin 7), BCK (pin 8), DOUT (pin 9)

(11) $f_S = 96\text{ kHz}$, system clock = $256 f_S$.

(12) Power-down and reset functions enabled by halting SCKI, BCK, LRCK.

PIN ASSIGNMENTS



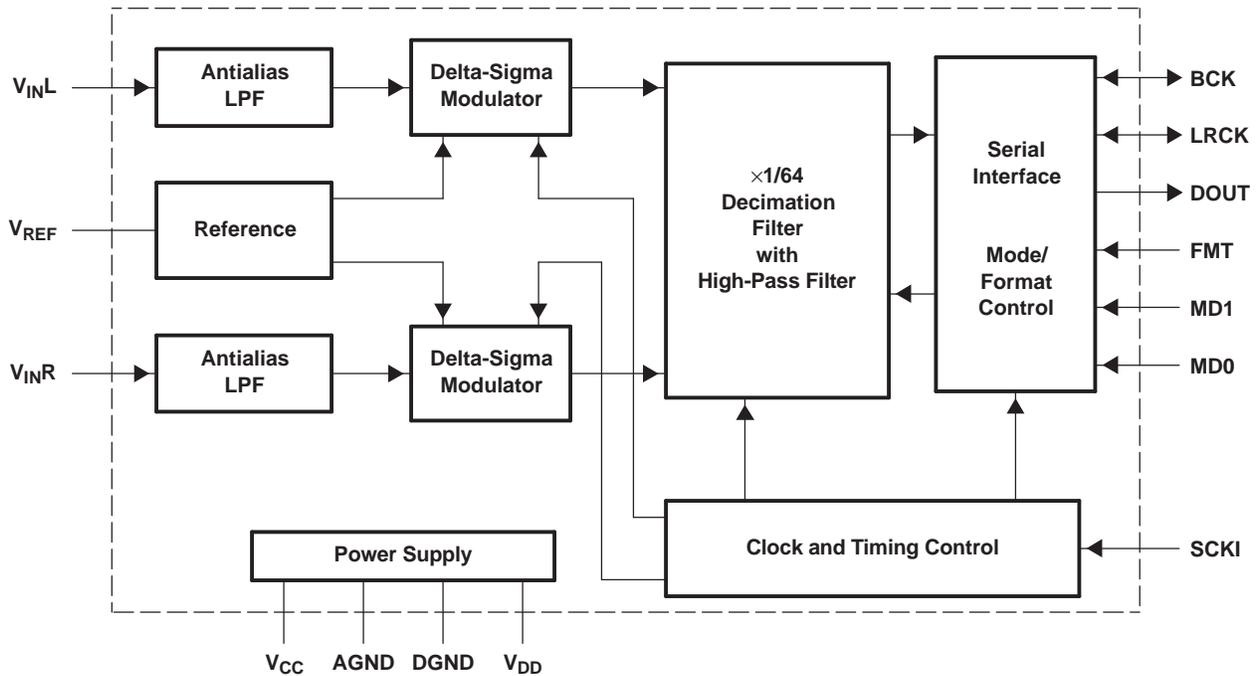
P0032-02

TERMINAL FUNCTIONS

TERMINAL NAME PIN		I/O	DESCRIPTION
AGND	2	–	Analog GND
BCK	8	I/O	Audio data bit clock input/output ⁽¹⁾
DGND	5	–	Digital GND
DOUT	9	O	Audio data digital output
FMT	12	I	Audio interface format select ⁽²⁾
LRCK	7	I/O	Audio data latch enable input/output ⁽¹⁾
MD0	10	I	Audio interface mode select 0 ⁽²⁾
MD1	11	I	Audio interface mode select 1 ⁽²⁾
SCKI	6	I	System clock input; 256 f _S , 384 f _S or 512 f _S ⁽³⁾
V _{CC}	3	–	Analog power supply, 5-V
V _{DD}	4	–	Digital power supply, 3.3-V
V _{IN} L	13	I	Analog input, L-channel
V _{IN} R	14	I	Analog input, R-channel
V _{REF}	1	–	Reference voltage decoupling (= 0.5 V _{CC})

- (1) Schmitt-trigger input with internal pulldown (50-kΩ, typical)
- (2) Schmitt-trigger input with internal pulldown (50-kΩ, typical), 5-V tolerant
- (3) Schmitt-trigger input, 5-V tolerant

Functional Block Diagram



B0004-10

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTERS

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, master mode, $f_S = 48\text{ kHz}$, system clock = $512 f_S$, 24-bit data, unless otherwise noted.

DECIMATION FILTER FREQUENCY RESPONSE

OVERALL CHARACTERISTICS

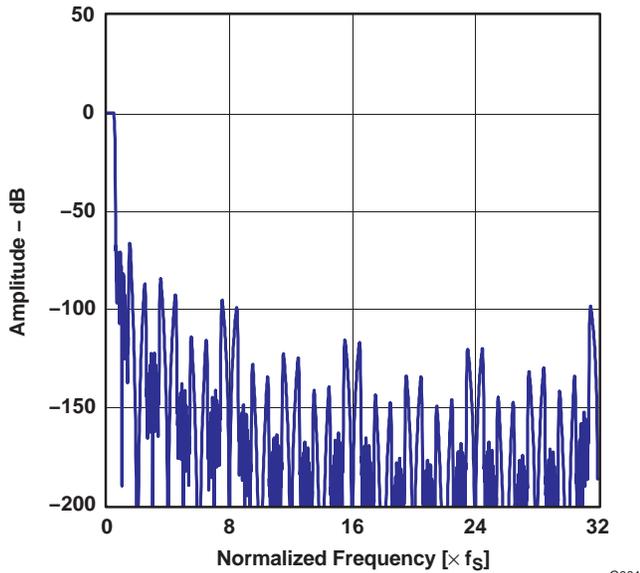


Figure 1.

G001

STOP-BAND ATTENUATION CHARACTERISTICS

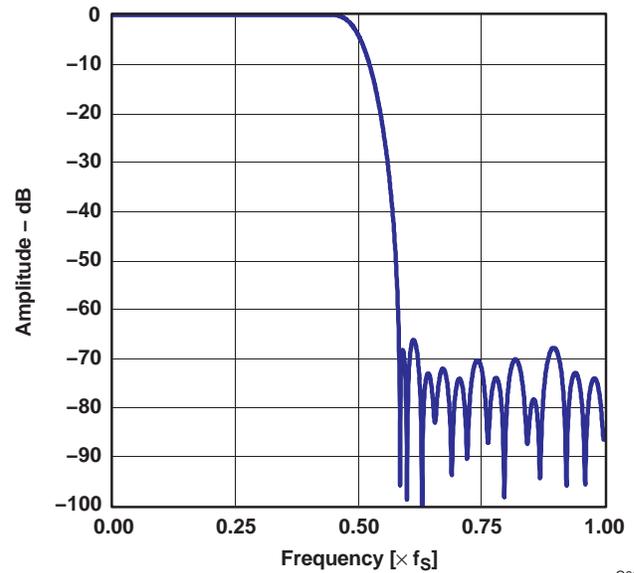


Figure 2.

G002

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTERS (Continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, master mode, $f_s = 48\text{ kHz}$, system clock = $512 f_s$, 24-bit data, unless otherwise noted.

DECIMATION FILTER FREQUENCY RESPONSE (Continued)

PASS-BAND RIPPLE CHARACTERISTICS

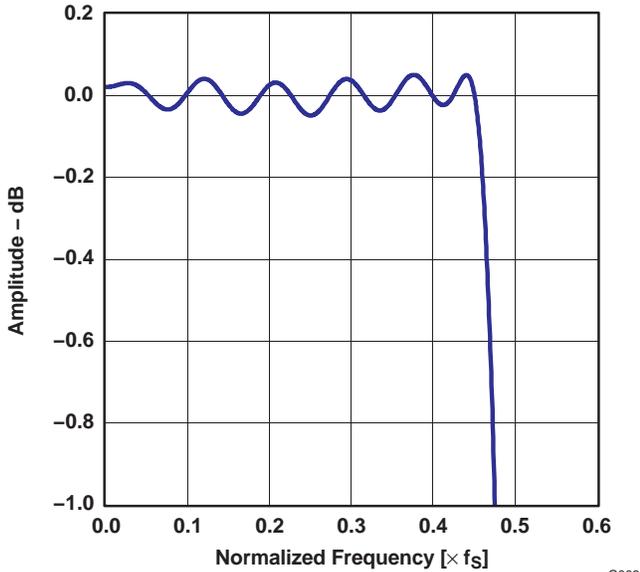


Figure 3.

G003

TRANSITION BAND CHARACTERISTICS

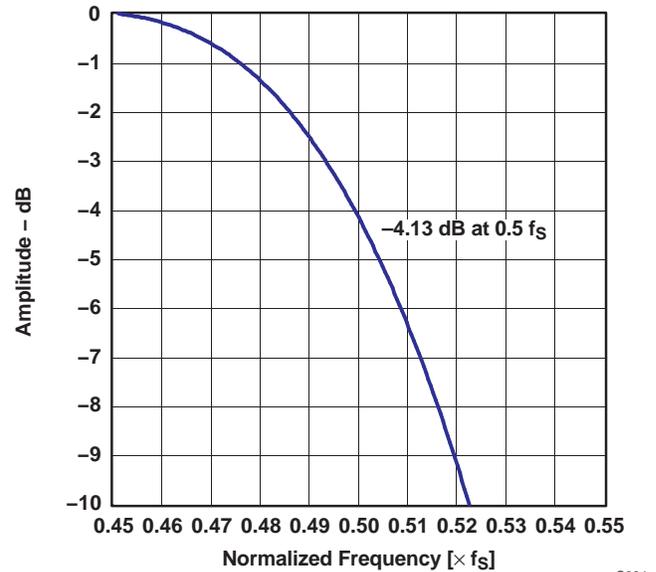


Figure 4.

G004

HIGH-PASS FILTER FREQUENCY RESPONSE

HPF STOP-BAND CHARACTERISTICS

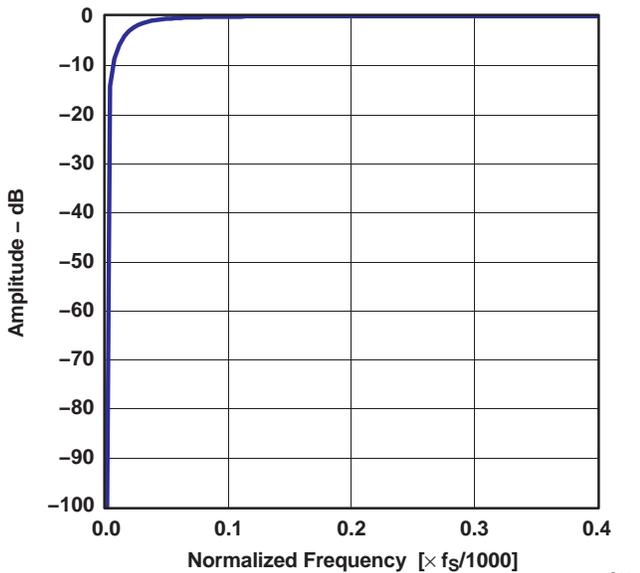


Figure 5.

G005

HPF PASS-BAND CHARACTERISTICS

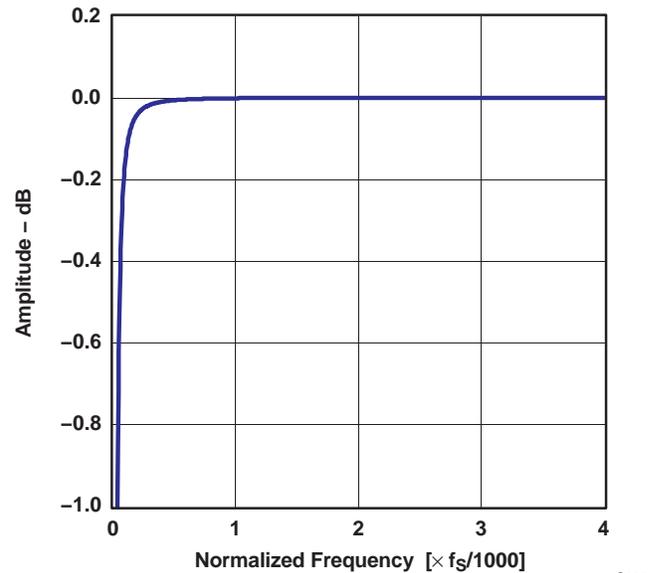


Figure 6.

G006

TYPICAL PERFORMANCE CURVES

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, master mode, $f_s = 48\text{ kHz}$, system clock = $512 f_s$, 24-bit data, unless otherwise noted.

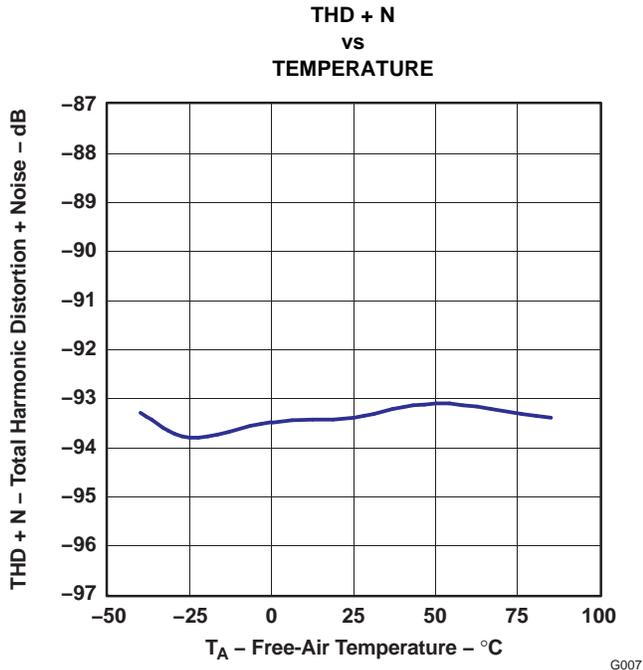


Figure 7.

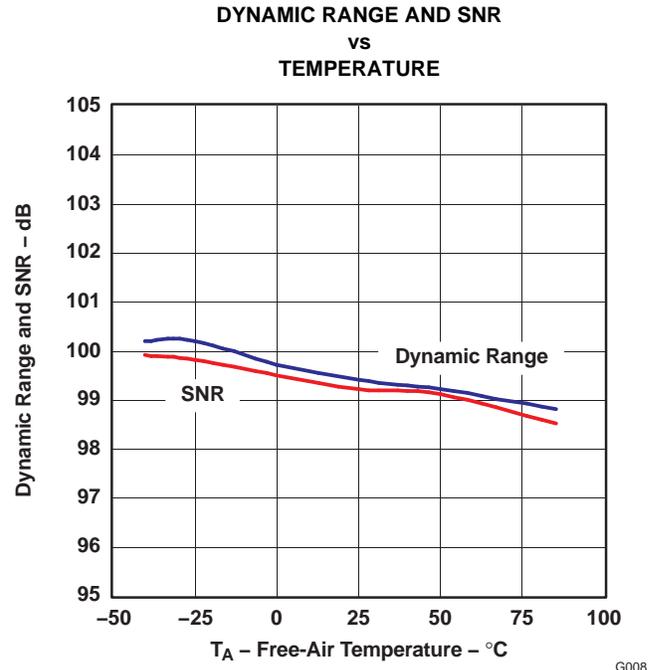


Figure 8.

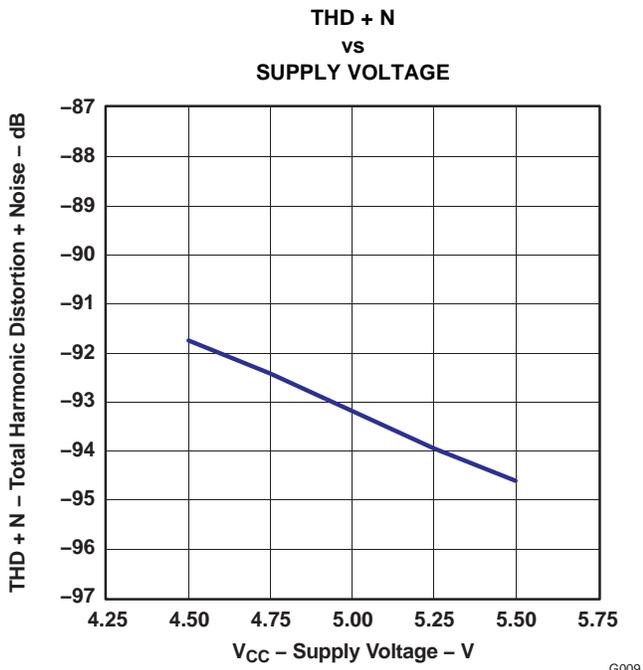


Figure 9.

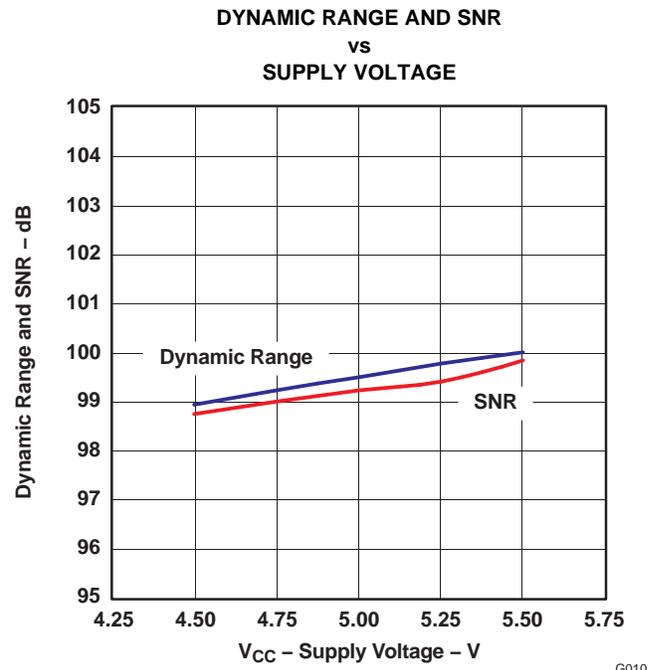


Figure 10.

TYPICAL PERFORMANCE CURVES (Continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, master mode, $f_S = 48\text{ kHz}$, system clock = $512 f_S$, 24-bit data, unless otherwise noted.

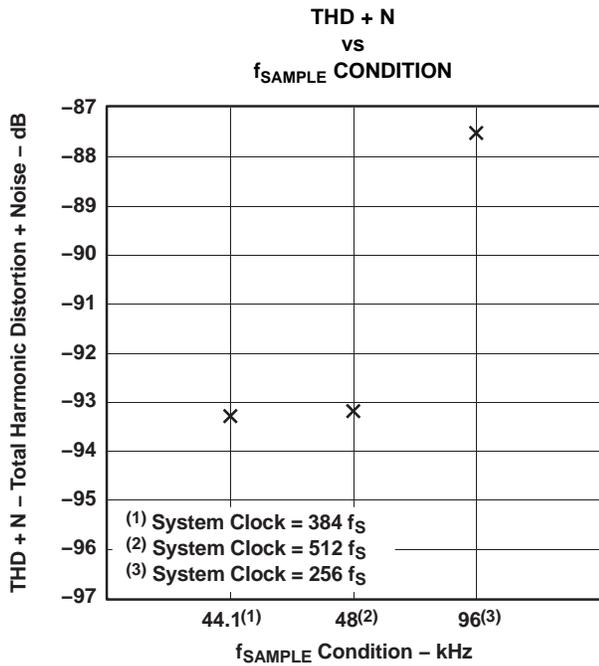


Figure 11.

G011

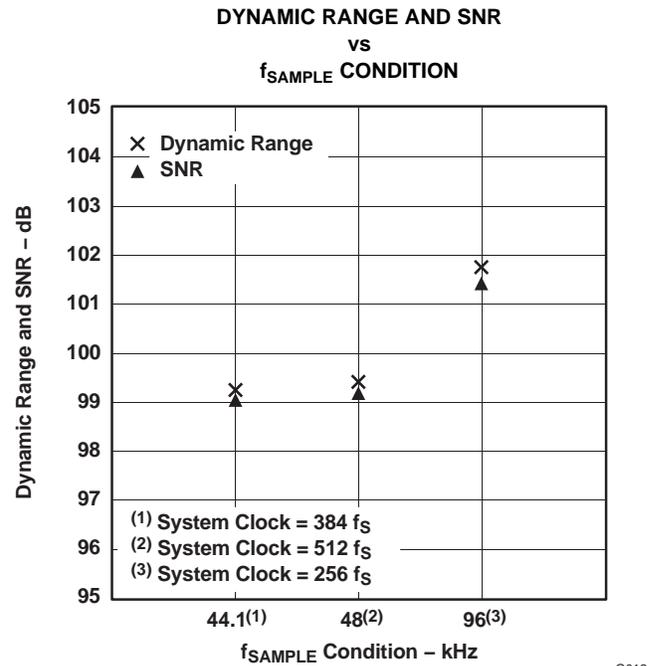


Figure 12.

G012

OUTPUT SPECTRUM

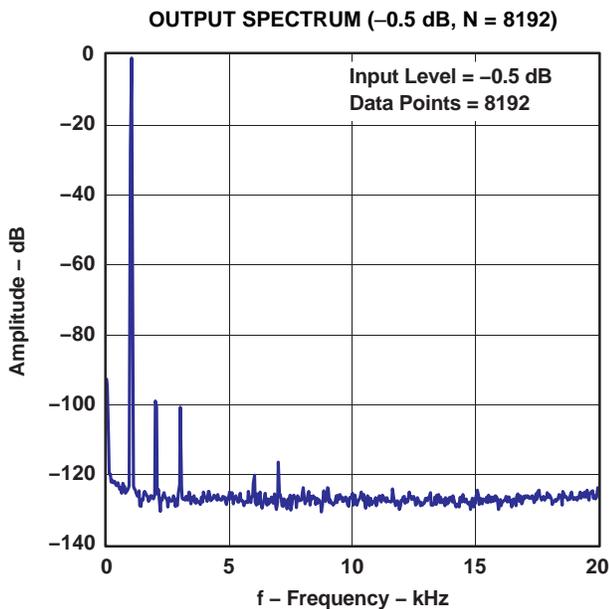


Figure 13.

G013

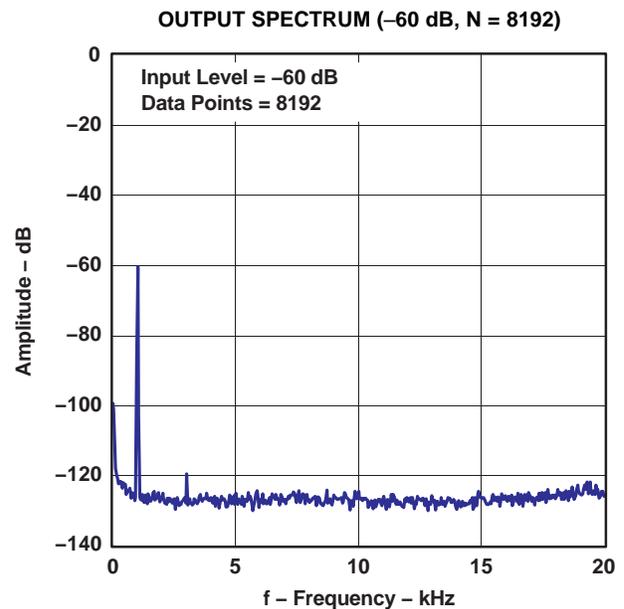


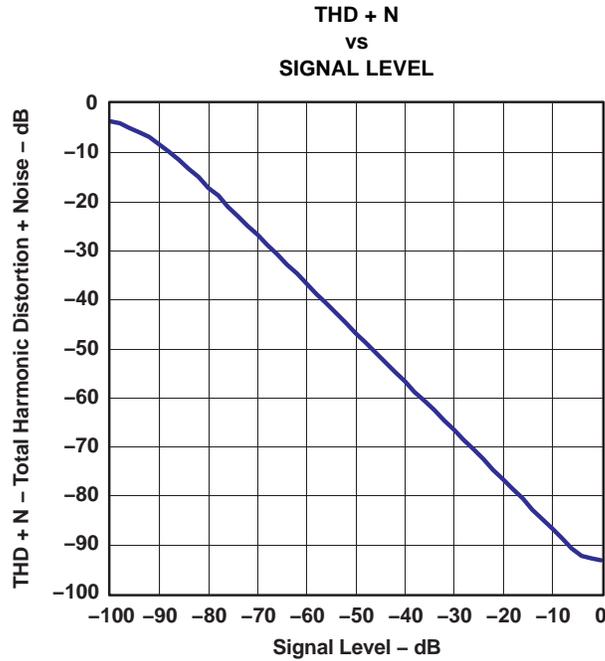
Figure 14.

G014

TYPICAL PERFORMANCE CURVES (Continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, master mode, $f_S = 48\text{ kHz}$, system clock = $512 f_S$, 24-bit data, unless otherwise noted.

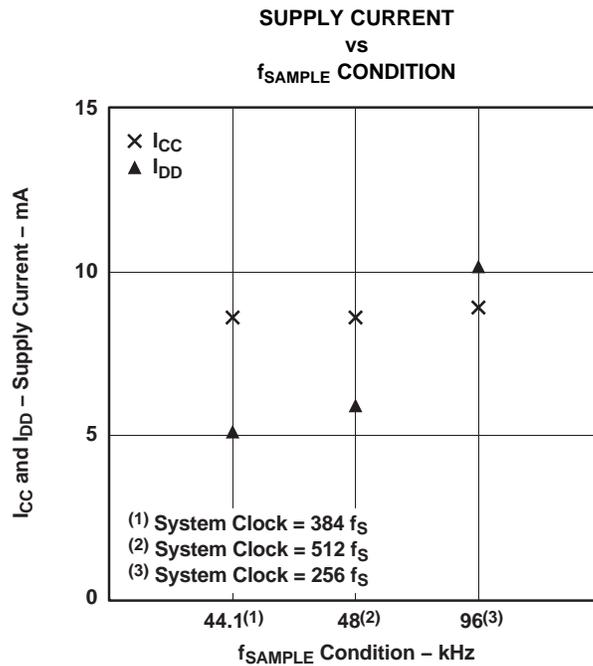
OUTPUT SPECTRUM (Continued)



G015

Figure 15.

SUPPLY CURRENT



G016

Figure 16.

SYSTEM CLOCK

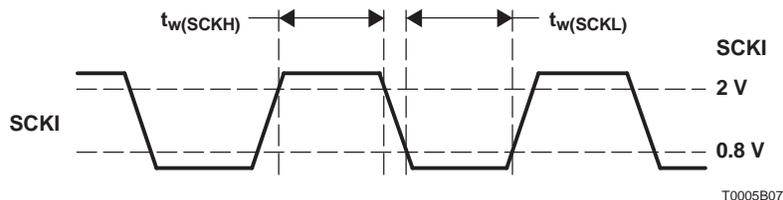
The PCM1808-Q1 supports $256 f_s$, $384 f_s$ and $512 f_s$ as system clock, where f_s is the audio sampling frequency. The system clock must be supplied on SCKI (pin 6).

The PCM1808-Q1 has a system clock detection circuit which automatically senses if the system clock is operating at $256 f_s$, $384 f_s$, or $512 f_s$ in slave mode. In master mode, the system clock frequency must be controlled through the serial control port, which uses MD1 (pin 111) and MD0 (pin 10). The system clock is divided down automatically to generate frequencies of $128 f_s$ and $64 f_s$, which are used to operate the digital filter and the delta-sigma modulator, respectively.

Table 1 shows some typical relationships between sampling frequency and system clock frequency, and Figure 17 shows system clock timing.

Table 1. Sampling Frequency and System Clock Frequency

SAMPLING FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (f_{SCLK}) (MHz)		
	$256 f_s$	$384 f_s$	$512 f_s$
8	2.048	3.072	4.096
16	4.096	6.144	8.192
32	8.192	12.288	16.384
44.1	11.2896	16.9344	22.5792
48	12.288	18.432	24.576
64	16.384	24.576	32.768
88.2	22.5792	33.8688	45.1584
96	24.576	36.864	49.152

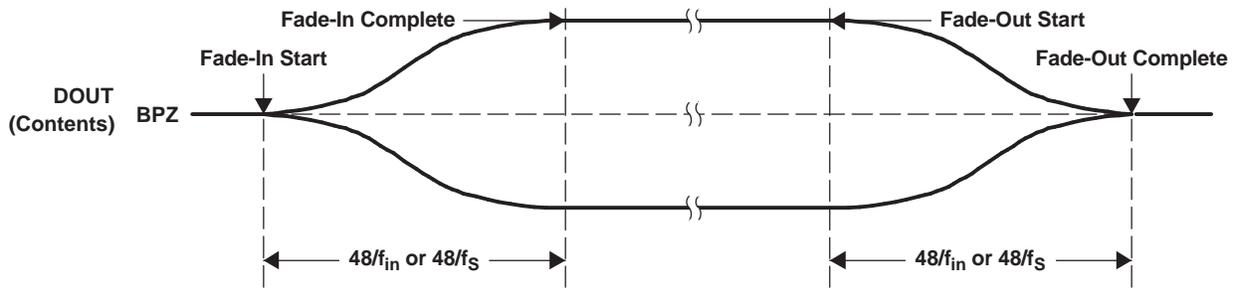


SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_w(SCKH)$	System clock pulse duration, HIGH	8		ns
$t_w(SCKL)$	System clock pulse duration, LOW	8		ns
	System clock duty cycle	40%	60%	

Figure 17. System Clock Timing

FADE-IN AND FADE-OUT FUNCTIONS

The PCM1808-Q1 has fade-in and fade-out functions on DOUT (pin 9) to avoid pop noise, and the functions come into operation in some cases as described in several following sections. The level changes from 0 dB to mute or mute to 0 dB are performed using calculated pseudo S-shaped characteristics with zero-cross detection. Because of the zero-cross detection, the time needed for the fade in and fade out depends on the analog input frequency (f_{in}). It takes $48/f_{in}$ until processing is completed. If there is no zero cross during $8192/f_s$, DOUT is faded in or out by force during $48/f_s$ (TIME OUT). Figure 18 illustrates the fade-in and fade-out operation processing.

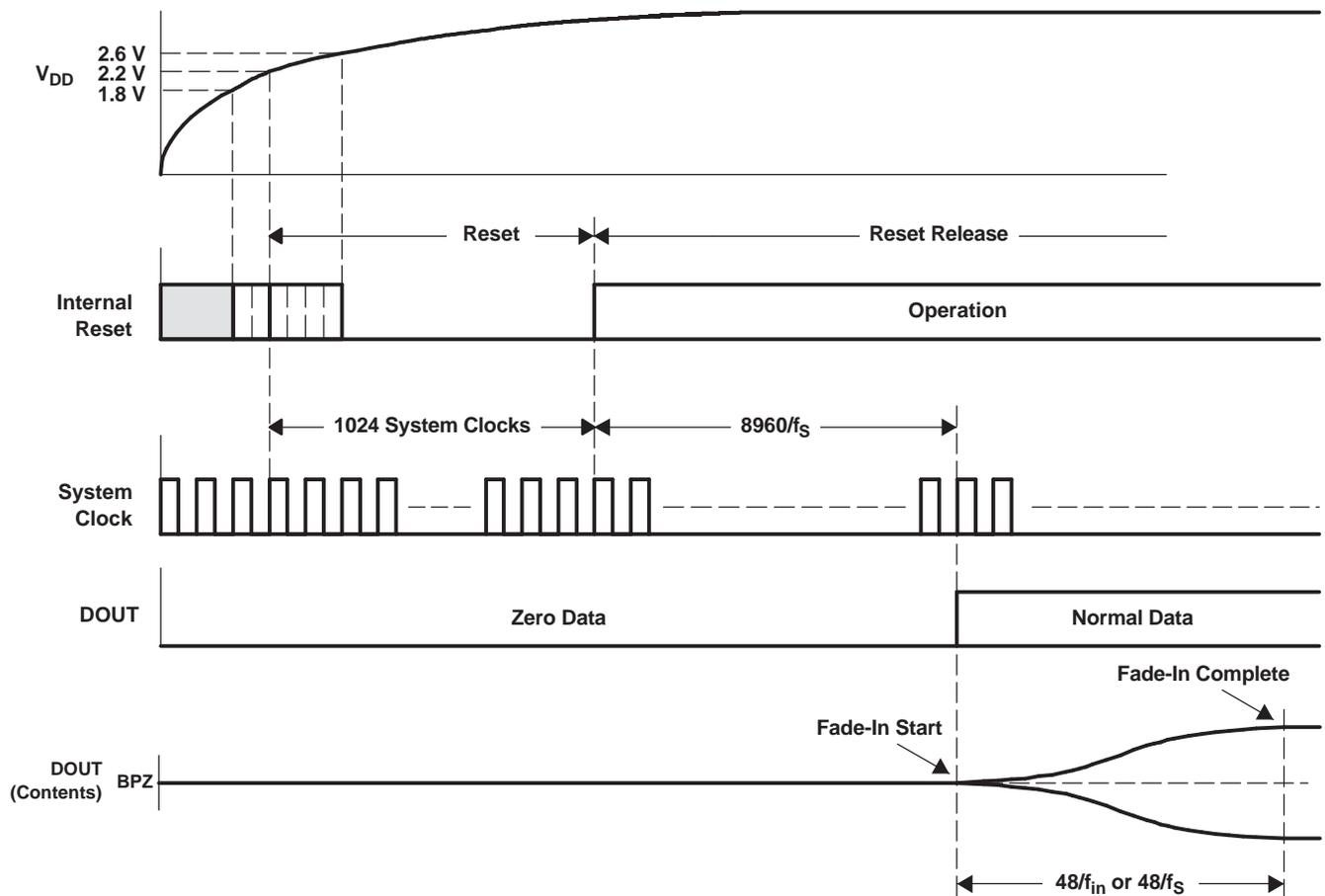


T0080-01

Figure 18. Fade-In and Fade-Out Operations

POWER ON

The PCM1808-Q1 has an internal power-on-reset circuit, and initialization (reset) is performed automatically when the power supply (V_{DD}) exceeds 2.2 V (typical). While $V_{DD} < 2.2$ V (typical), and for 1024 system-clock counts after $V_{DD} > 2.2$ V (typical), the PCM1808-Q1 stays in the reset state and the digital output is forced to zero. The digital output is valid after the reset state is released and the time of $8960/f_s$ has elapsed. Because the fade-in operation is performed, it takes additional time of $48/f_{in}$ or $48/f_s$ until the data corresponding to the analog input signal is obtained. Figure 19 illustrates the power-on timing and the digital output.



T0014-09

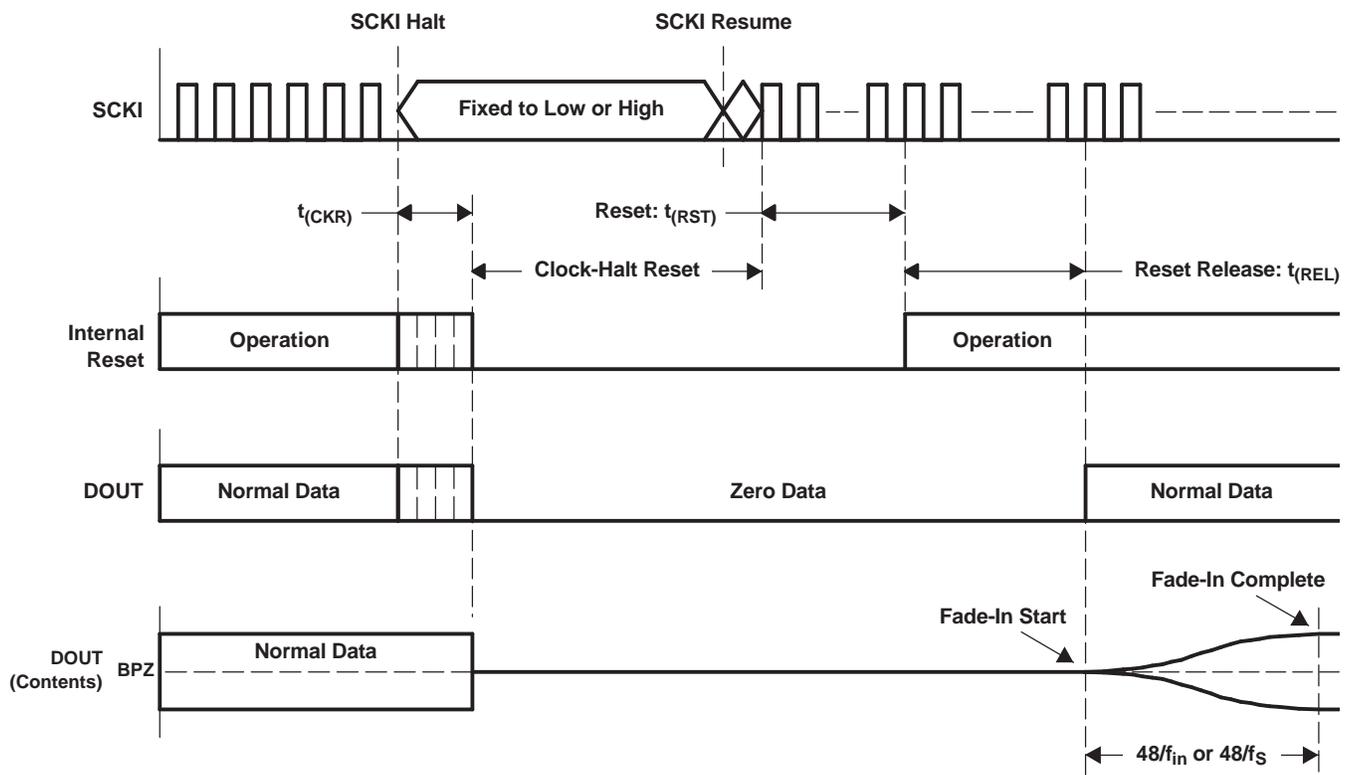
Figure 19. Power-On Timing

CLOCK-HALT POWER-DOWN AND RESET FUNCTION

The PCM1808-Q1 has a power-down and reset function, which is triggered by halting SCKI (pin 6) in both master and slave modes. The function is available anytime after power on. Reset and power down are performed automatically 4 μ s (minimum) after SCKI is halted. While the clock-halt reset is asserted, the PCM1808-Q1 stays in the reset and power-down mode, and DOUT (pin 9) is forced to zero. SCKI must be supplied to release the reset and power-down mode. The digital output is valid after the reset state is released and the time of 1024 SCKI + 8960/ f_s has elapsed. Because the fade-in operation is performed, it takes additional time of 48/ f_{in} or 48/ f_s until the level corresponding to the analog input signal is obtained. Figure 20 illustrates the clock-halt reset timing.

To avoid ADC performance degradation, BCK (pin 8) and LRCK (pin 7) are required to synchronize with SCKI within 4480/ f_s after SCKI is resumed. If it takes more than 4480/ f_s for BCK and LRCK to synchronize with SCKI, SCKI should be masked until the synchronization is achieved again, taking care of glitch and jitter. See the typical circuit connection diagram, Figure 26.

To avoid ADC performance degradation, the clock-halt reset also should be asserted when system clock SCKI or the audio interface clocks BCK and LRCK (sampling rate f_s) are changed on the fly.



T0081-01

SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{(CKR)}$	Delay time from SCKI halt to internal reset	4		μ s
$t_{(RST)}$	Delay time from SCKI resume to reset release		1024 SCKI	μ s
$t_{(REL)}$	Delay time from reset release to DOUT output		8960/ f_s	μ s

Figure 20. Clock-Halt Power-Down and Reset Timing

SERIAL AUDIO DATA INTERFACE

The PCM1808-Q1 interfaces the audio system through LRCK (pin 7), BCK (pin 8), and DOUT (pin 9).

INTERFACE MODE

The PCM1808-Q1 supports master mode and slave mode as interface modes, which are selected by MD1 (pin 11) and MD0 (pin 10), as shown in [Table 2](#). MD1 and MD0 must be set prior to power on.

In master mode, the PCM1808-Q1 provides the timing of serial audio data communications between the PCM1808-Q1 and the digital audio processor or external circuit. While in slave mode, the PCM1808-Q1 receives the timing for data transfer from an external controller.

Table 2. Interface Modes

MD1 (Pin 11)	MD0 (Pin 10)	INTERFACE MODE
Low	Low	Slave mode (256 f _S , 384 f _S , 512 f _S autodetection)
Low	High	Master mode (512 f _S)
High	Low	Master mode (384 f _S)
High	High	Master mode (256 f _S)

Master mode

In master mode, BCK and LRCK work as output pins, and these pins are controlled by timing which is generated in the clock circuit of the PCM1808-Q1. The frequency of BCK is fixed at 64 BCK/frame.

Slave mode

In slave mode, BCK and LRCK work as input pins. The PCM1808-Q1 accepts 64-BCK/frame or 48-BCK/frame format (only for a 384-f_S system clock), not 32-BCK/frame format.

DATA FORMAT

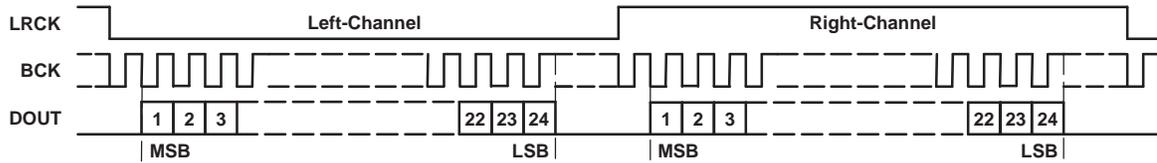
The PCM1808-Q1 supports two audio data formats in both master and slave modes. The data formats are selected by FMT (pin 12), as shown in [Table 3](#). [Figure 21](#) illustrates the data formats in slave mode and master mode.

Table 3. Data Format

FORMAT NO.	FMT (Pin 12)	FORMAT
0	Low	I ² S, 24-bit
1	High	Left-justified, 24-bit

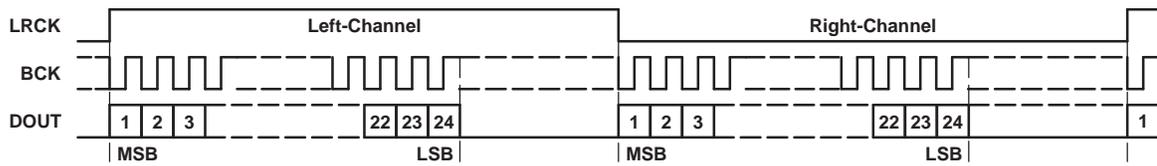
FORMAT 0: FMT = LOW

24-Bit, MSB-First, I²S



FORMAT 1: FMT = HIGH

24-Bit, MSB-First, Left-Justified

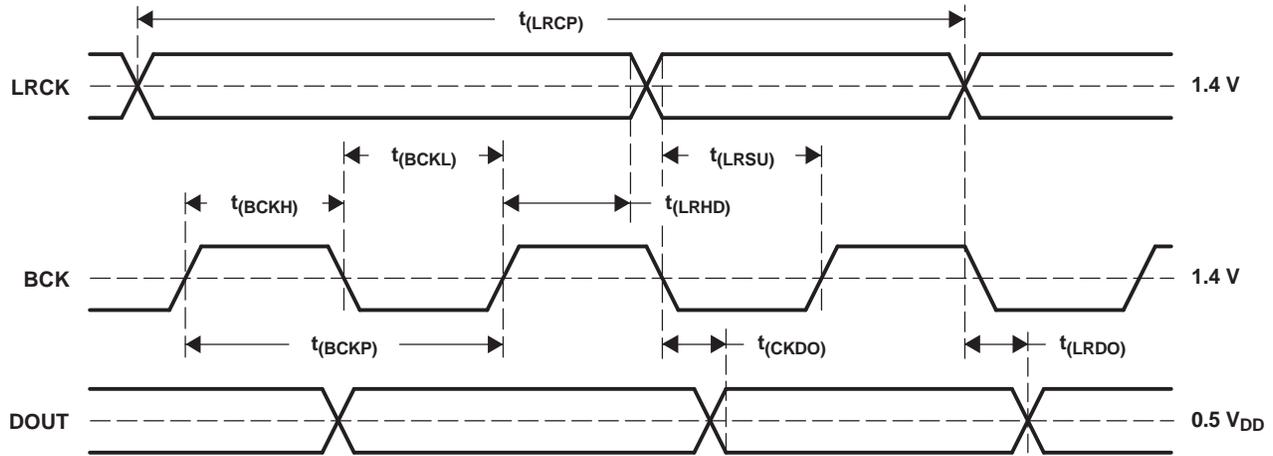


T0016-17

Figure 21. Audio Data Format (LRCK and BCK Work as Inputs in Slave Mode and as Outputs in Master Mode)

INTERFACE TIMING

Figure 22 and Figure 23 illustrate the interface timing in slave mode and master mode, respectively.

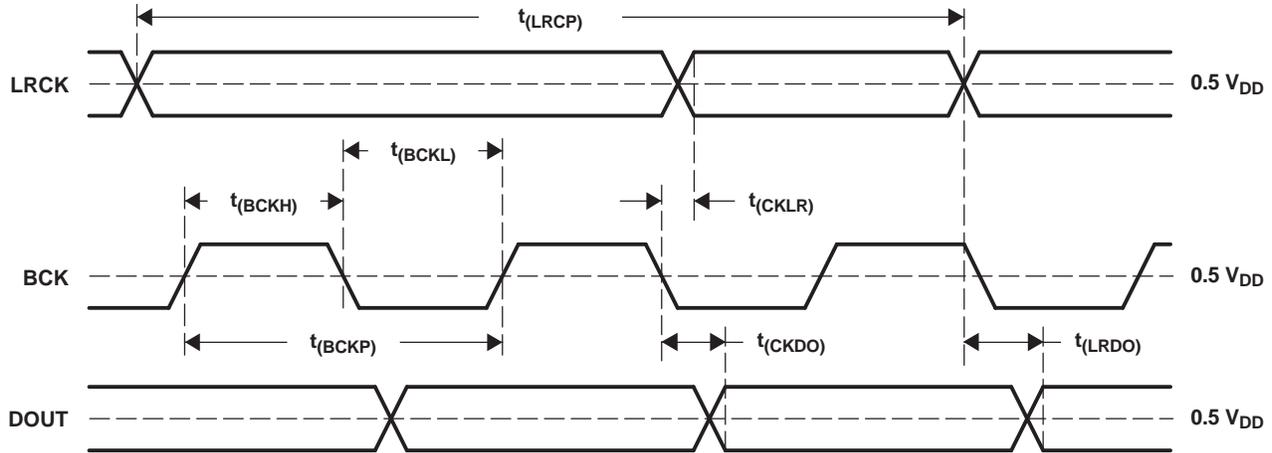


T0017-02

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$t_{(BCKP)}$	BCK period	$1/(64 f_S)$			ns
$t_{(BCKH)}$	BCK pulse duration, HIGH	$1.5 \times t_{(SCKI)}$			ns
$t_{(BCKL)}$	BCK pulse duration, LOW	$1.5 \times t_{(SCKI)}$			ns
$t_{(LRSU)}$	LRCK setup time to BCK rising edge	50			ns
$t_{(LRHD)}$	LRCK hold time to BCK rising edge	10			ns
$t_{(LRCP)}$	LRCK period	10			μ s
$t_{(CKDO)}$	Delay time, BCK falling edge to DOUT valid	-10		40	ns
$t_{(LRDO)}$	Delay time, LRCK edge to DOUT valid	-10		40	ns
t_r	Rise time of all signals			20	ns
t_f	Fall time of all signals			20	ns

NOTE: Timing measurement reference level is 1.4 V for input and 0.5 V_{DD} for output. Rise and fall times are from 10% to 90% of the input/output signal swing. Load capacitance of DOUT is 20 pF. $t_{(SCKI)}$ is the SCKI period.

Figure 22. Audio Data Interface Timing (Slave Mode: LRCK and BCK Work as Inputs)

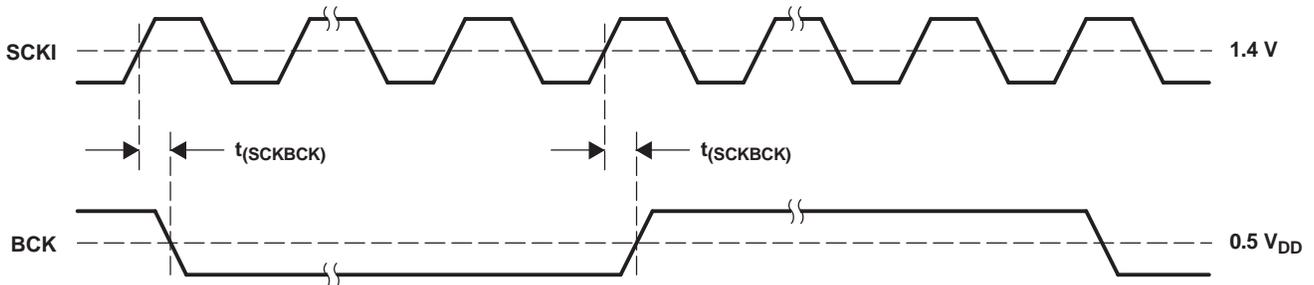


T0018-02

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$t_{(BCKP)}$	BCK period	150	$1/(64 f_s)$	2000	ns
$t_{(BCKH)}$	BCK pulse duration, HIGH	65		1200	ns
$t_{(BCKL)}$	BCK pulse duration, LOW	65		1200	ns
$t_{(CKLR)}$	Delay time, BCK falling edge to LRPC valid	-10		20	ns
$t_{(LRCP)}$	LRCK period	10	$1/f_s$	125	μs
$t_{(CKDO)}$	Delay time, BCK falling edge to DOUT valid	-10		20	ns
$t_{(LRDO)}$	Delay time, LRCK edge to DOUT valid	-10		20	ns
t_r	Rise time of all signals			20	ns
t_f	Fall time of all signals			20	ns

NOTE: Timing measurement reference level is $0.5 V_{DD}$. Rise and fall times are from 10% to 90% of the input/output signal swing. Load capacitance of all signals is 20 pF.

Figure 23. Audio Data Interface Timing (Master Mode: LRCK and BCK Work as Outputs)



T0074-01

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$t_{(SCKBCK)}$	Delay time, SCKI rising edge to BCK edge	5		30	ns

NOTE: Timing measurement reference level is 1.4 V for input and $0.5 V_{DD}$ for output. Load capacitance of BCK is 20 pF. This timing is applied when SCKI frequency is less than 25 MHz.

Figure 24. Audio Clock Interface Timing (Master Mode: BCK Works as Output)

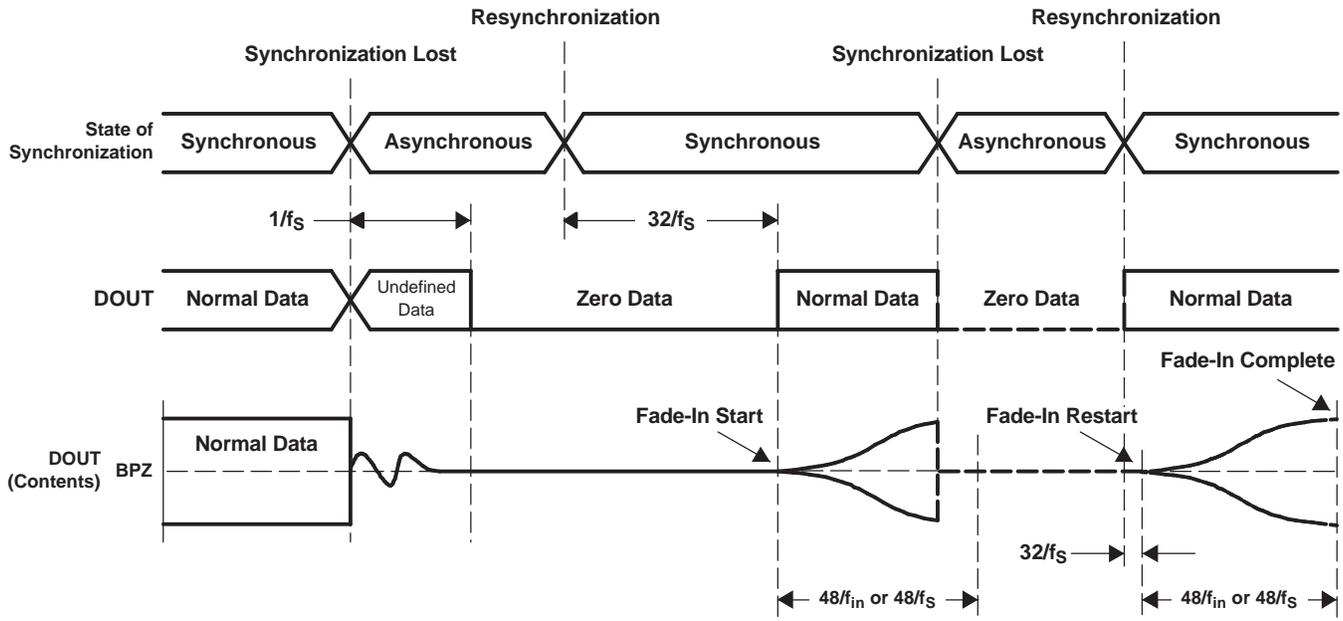
SYNCHRONIZATION WITH DIGITAL AUDIO SYSTEM

In slave mode, the PCM1808-Q1 operates under LRCK (pin 7), synchronized with system clock SCKI (pin 6). The PCM1808-Q1 does not require a specific phase relationship between LRCK and SCKI, but does require the synchronization of LRCK and SCKI.

If the relationship between LRCK and SCKI changes more than ± 6 BCKs for 64 BCK/frame (± 5 BCKs for 48 BCK/frame) during one sample period due to LRCK or SCKI jitter, internal operation of the ADC halts within $1/f_s$ and digital output is forced to zero data (BPZ code) until resynchronization between LRCK and SCKI is established.

In the case of changes less than ± 5 BCKs for 64 BCK/frame (± 4 BCKs for 48 BCK/frame), resynchronization does not occur and the previously described digital output control and discontinuity do not occur.

Figure 25 illustrates the digital output response for loss of synchronization and resynchronization. During undefined data, the PCM1808-Q1 can generate some noise in the audio signal. Also, the transition of normal data to undefined data creates a discontinuity in the digital output data, which can generate some noise in the audio signal. The digital output is valid after resynchronization completes and the time of $32/f_s$ has elapsed. Because the fade-in operation is performed, it takes additional time of $48/f_{in}$ or $48/f_s$ until the level corresponding to the analog input signal is obtained. If synchronization is lost during the fade-in or fade-out operation, the operation stops and DOUT (pin 9) is forced to zero data immediately. The fade-in operation resumes from mute after the time of $32/f_s$ following resynchronization.



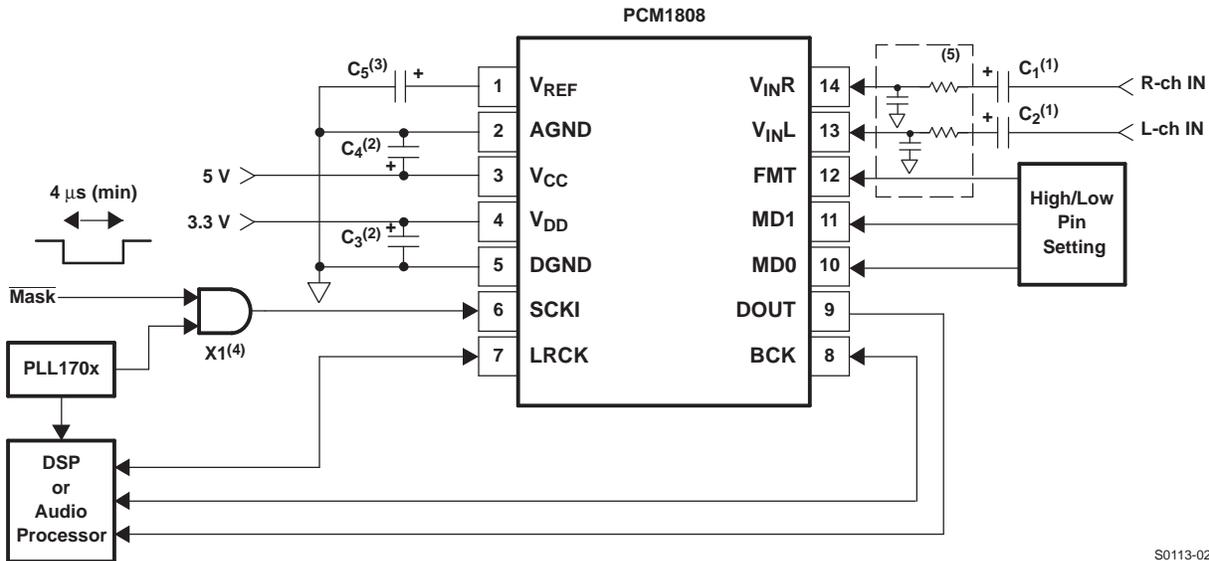
T0082-01

Figure 25. ADC Digital Output for Loss of Synchronization and Resynchronization

APPLICATION INFORMATION

TYPICAL CIRCUIT CONNECTION DIAGRAM

Figure 26 is a typical circuit connection diagram. The antialiasing low-pass filters are integrated on the analog inputs, V_{INL} and V_{INR} . If the performance of these filters is not adequate for an application, appropriate external antialiasing filters are needed. A passive RC filter (100 Ω and 0.01 μF to 1 k Ω and 1000 pF) generally is used.



S0113-02

- (1) C1, C2: A 1- μF electrolytic capacitor gives 2.7 Hz ($\tau = 1 \mu\text{F} \times 60 \text{ k}\Omega$) cutoff frequency for the input HPF in normal operation and requires a power-on settling time with a 60-ms time constant in the power-on initialization period.
- (2) C3, C4: Bypass capacitors, 0.1- μF ceramic and 10- μF electrolytic, depending on layout and power supply
- (3) C5: 0.1- μF ceramic and 10- μF electrolytic capacitors are recommended.
- (4) X1: X1 masks the system clock input when using the clock-halt reset function with external control.
- (5) Optional external antialiasing filter could be required, depending on the application.

Figure 26. Typical Circuit Connection Diagram

BOARD DESIGN AND LAYOUT CONSIDERATIONS

V_{CC} , V_{DD} PINS

The digital and analog power supply lines to the PCM1808-Q1 should be bypassed to the corresponding ground pins with both 0.1- μF ceramic and 10- μF electrolytic capacitors as close to the pins as possible to maximize the dynamic performance of the ADC.

AGND, DGND PINS

To maximize the dynamic performance of the PCM1808-Q1, the analog and digital grounds are not internally connected. These grounds should have low impedance to avoid digital noise feedback into the analog ground. They should be connected directly to each other under the PCM1808-Q1 package to reduce potential noise problems.

V_{INL} , V_{INR} PINS

V_{INL} and V_{INR} are single-ended inputs. The antialias low-pass filters are integrated on these inputs to remove the high-frequency noise outside the audio band. If the performance of these filters is not adequate for an application, appropriate external antialiasing filters are required. A passive RC filter (100 Ω and 0.01 μF to 1 k Ω and 1000 pF) is generally used.

V_{REF} PIN

To ensure low source impedance of the ADC references, 0.1- μ F ceramic and 10- μ F electrolytic capacitors are recommended between V_{REF} and AGND. These capacitors should be located as close as possible to the V_{REF} pin to reduce dynamic errors on the ADC references.

DOUT PIN

The DOUT pin has a large load-drive capability, but if the DOUT line is long, locating a buffer near the PCM1808-Q1 and minimizing load capacitance is recommended to minimize the digital-analog crosstalk and maximize the dynamic performance of the ADC.

SYSTEM CLOCK

The quality of the system clock can influence dynamic performance, as the PCM1808-Q1 operates based on a system clock. Therefore, it may be necessary to consider the system clock duty, jitter, and the time difference between system clock transition and BCK or LRCK transition in slave mode.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
PCM1808QPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

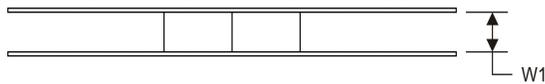
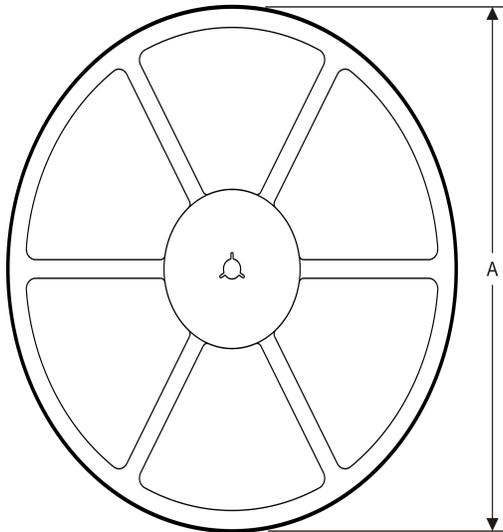
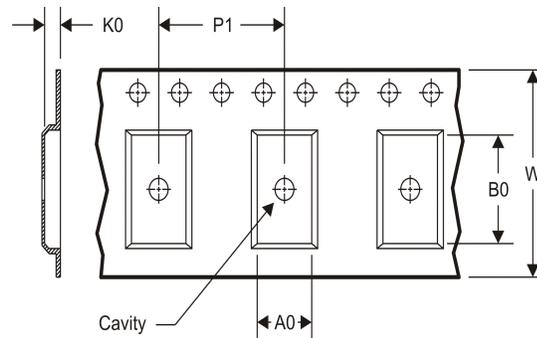
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF PCM1808-Q1 :

- Catalog: [PCM1808](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


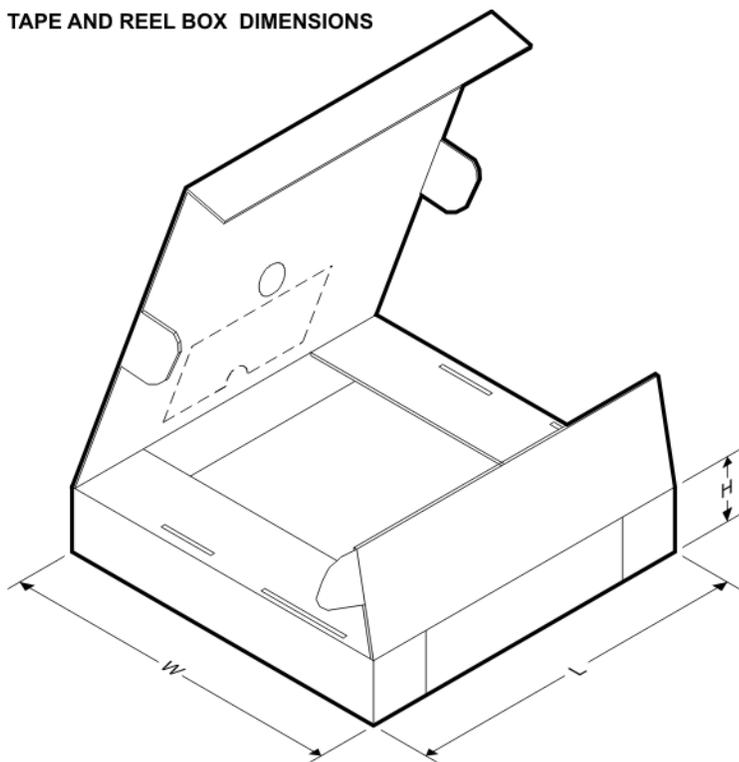
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1808QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

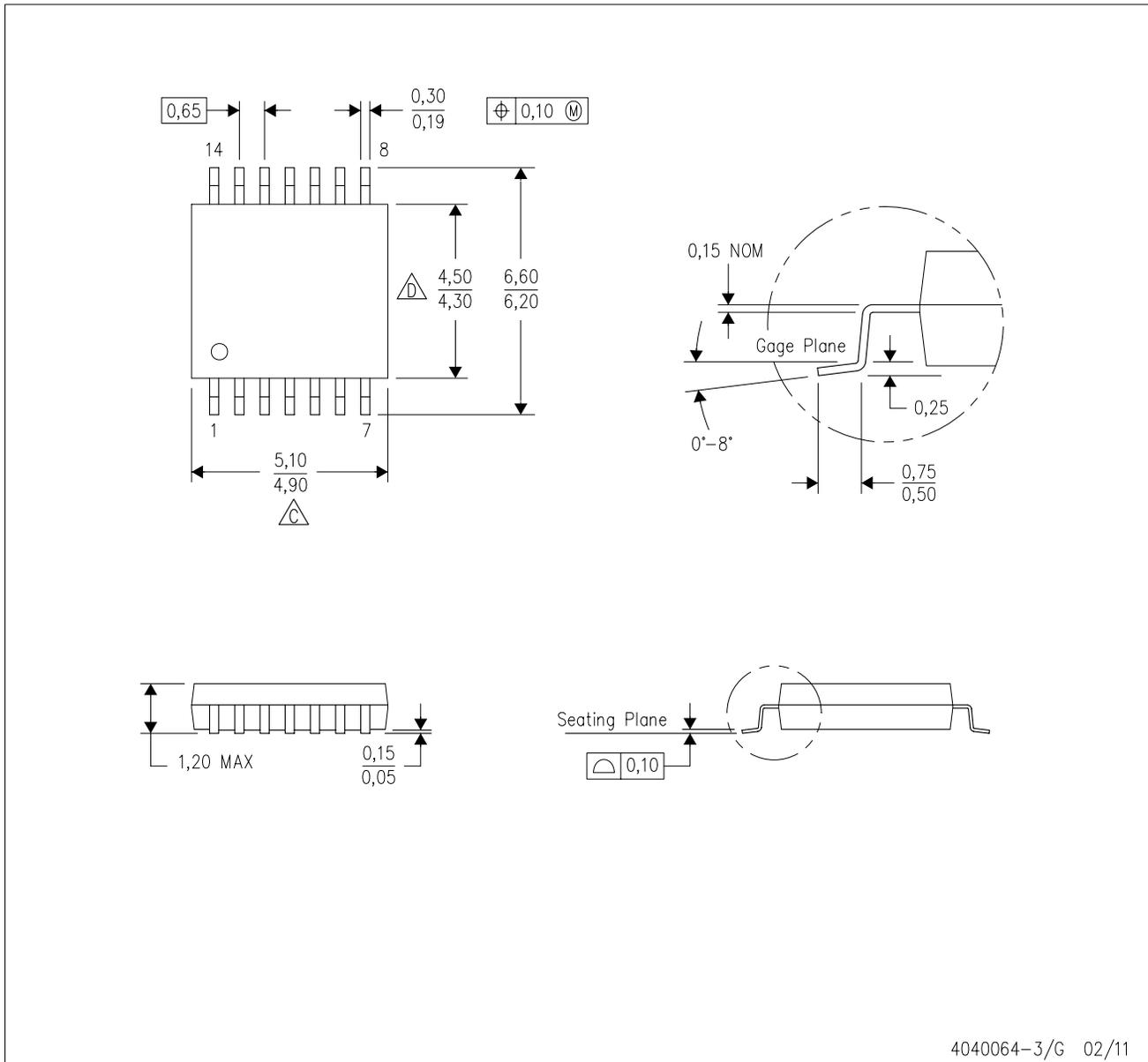


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1808QPWRQ1	TSSOP	PW	14	2000	346.0	346.0	29.0

PW (R-PDSO-G14)

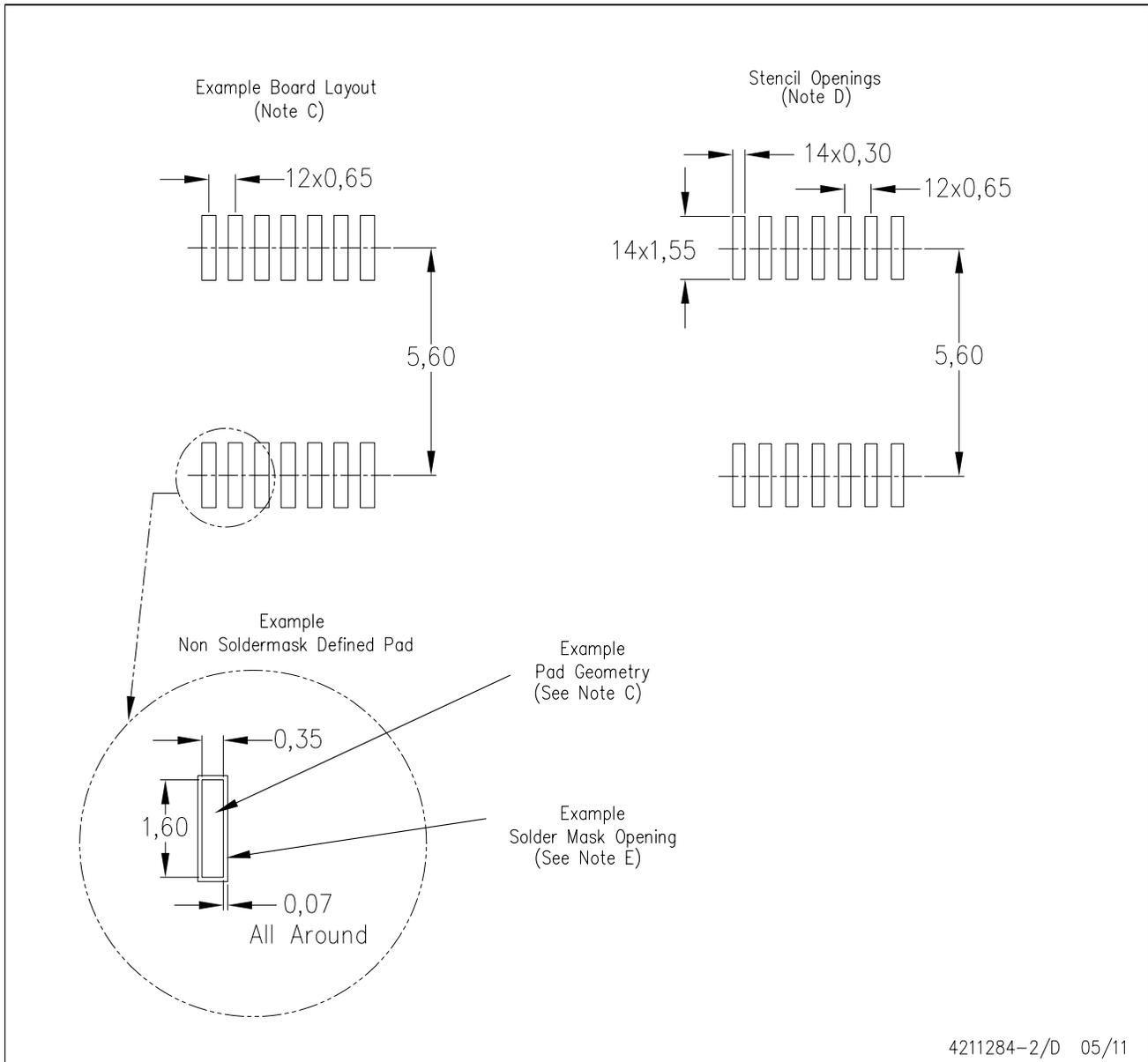
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/D 05/11

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Mobile Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2012, Texas Instruments Incorporated