

FEATURES

- Controlled Baseline
 - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of -40°C to 125°C and -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree (1)
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Operates From 2 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 7.5 ns at 3.3 V
- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25° C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 >2 V at V_{CC} = 3.3 V, T_A = 25°C
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})

DR DW OR DW DACKAGE

 I_{off} Supports Partial-Power-Down Mode Operation

DB, DV		RPW	/ PA	CRAGE
	(TC	OP VI	EW)
		\mathbf{T}		
OE [1	\cup	20	Vcc
1Q [2		19] 8Q
1D [3		18] 8D
2D [4		17]7D
2Q [5		16] 7Q
3Q [6		15] 6Q
3D [7		14]6D
4D [8		13] 5D
4Q [9		12] 5Q
GND [10		11	LE
				,

DESCRIPTION/ORDERING INFORMATION

The SN74LVC373A octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC373A is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

T _A	PAC	KAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC – DW	Reel of 2000	SN74LVC373AQDWREP	C373AEP
-40 C to 125 C	TSSOP – PW	Reel of 2000	SN74LVC373AQPWREP	C373AEP
–55°C to 125°C	SSOP – DB	Reel of 2000	SN74LVC373AMDBREP	C373AEP

ORDERING INFORMATION⁽¹⁾

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74LVC373A-EP OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS737C-NOVEMBER 2003-REVISED MARCH 2007

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

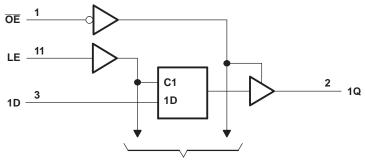
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

FUNCTION TABLE (each latch)

	-	-	
	INPUTS		OUTPUT
OE	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Х	Q ₀
н	Х	Х	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



To Seven Other Channels

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
V_{CC}	Supply voltage range		-0.5	6.5	V	
VI	Input voltage range ⁽²⁾		-0.5	6.5	V	
Vo	Voltage range applied to any output in the high-ir	mpedance or power-off state ⁽²⁾	-0.5	6.5	V	
Vo	Voltage range applied to any output in the high o	r low state ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V ₁ < 0		-50	mA	
I _{OK}	Output clamp current	tput clamp current V _O < 0		-50	mA	
I _O	Continuous output current			±50	mA	
	Continuous current through V _{CC} or GND			±100	mA	
		DB package		120		
θ_{JA}	Package thermal impedance ⁽⁴⁾	DW package	58		°C/W	
		PW package		83		
T _{stg}	Storage temperature range ⁽⁵⁾		-65	150	°C	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the recommended operating conditions table.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

(5) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V	Supply voltage	Operating	2	3.6	V
V _{CC}	Supply voltage	Data retention only	1.5		v
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
VI	Input voltage		0	5.5	V
V	/ _O Output voltage	High or low state	0	V _{CC}	V
۷O		3-state	0	5.5	v
	Ligh lovel output outport	$V_{CC} = 2.7 V$		-12	~^^
I _{OH}	High-level output current	V _{CC} = 3 V		-24	mA
		V _{CC} = 2.7 V		12	~^^
I _{OL}	Low-level output current	V _{CC} = 3 V		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
-		Q suffix	-40	125	°C
T _A	Operating free-air temperature	M suffix	-55	125	Ĵ

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVC373A-EP **OCTAL TRANSPARENT D-TYPE LATCH** WITH 3-STATE OUTPUTS SCAS737C-NOVEMBER 2003-REVISED MARCH 2007

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾	MAX	UNIT
	I _{OH} = -100 μA	2.7 V to 3.6 V	$V_{CC} - 0.2$			
N/	40	2.7 V	2.2			V
V _{OH}	$I_{OH} = -12 \text{ mA}$	3 V	2.4			V
	$I_{OH} = -24 \text{ mA}$	3 V	2.2			
	I _{OL} = 100 μA	2.7 V to 3.6 V			0.2	
V _{OL}	$I_{OL} = 12 \text{ mA}$	2.7 V			0.4	V
	$I_{OL} = 24 \text{ mA}$	3 V			0.55	
l _l	$V_1 = 0$ to 5.5 V	3.6 V			±5	μA
I _{OZ}	$V_0 = 0$ to 5.5 V	3.6 V			±15	μA
I	$V_1 = V_{CC} \text{ or } GND, \qquad I_O = 0$	3.6 V			10	۸
I _{CC}	$3.6 \ V \le V_1 \ \le 5.5 \ V^{(2)}, \qquad I_0 = 0$	3.0 V			10	μA
ΔI_{CC}	One input at $V_{CC} - 0.6 V$, Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500	μA
C _i	$V_{I} = V_{CC}$ or GND	3.3 V		4	12	pF
Co	$V_0 = V_{CC} \text{ or } GND$	3.3 V		5.5	12	pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C. (2) This applies in the disabled state only.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC} =	$V_{CC} = 2.7 V$		V _{CC} = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX		
tw	Pulse duration, LE high	3.3		3.3		ns	
t _{su}	Setup time, data before LE \downarrow	2		2		ns	
t _h	Hold time, data after LE \downarrow	2		2		ns	

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.7 V		V _{CC} = 3 ± 0.3	3.3 V V	UNIT
			MIN	MAX	MIN	MAX	
+	D	0		8.5	1	7.5	20
t _{pd}	LE	Q		9.5	1	8.5	ns
t _{en}	ŌĒ	Q		8.7	1	7.7	ns
t _{dis}	ŌĒ	Q		8	0.5	7	ns

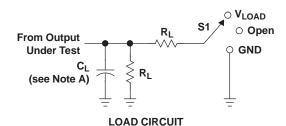
Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER		TEST CONDITIONS	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT
<u> </u>	Dower discinction conscitutes nor latch	Outputs enabled	f = 10 MHz	(1)	46	ρF
C _{pd}	Power dissipation capacitance per latch	Outputs disabled		(1)	3	рг

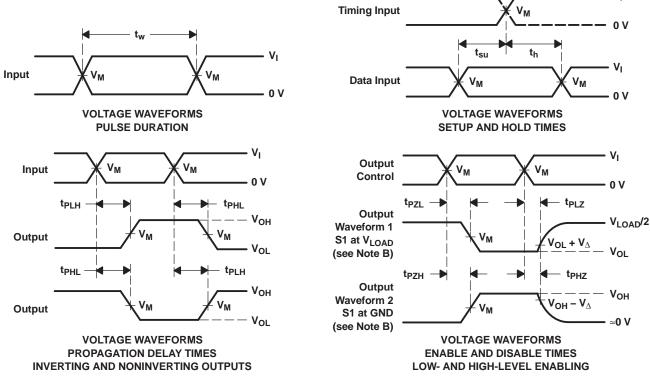
(1) This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

	INPUTS		N/	N	•		N
V _{CC}	VI	t _r /t _f	t _f V _M V _{LOAD}		CL	RL	V_{Δ}
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
$\textbf{3.3 V} \pm \textbf{0.3 V}$	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



NOTES: A. C₁ includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z₀ = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

Vı

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVC373AMDBREP	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC373AQDWREP	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC373AQPWREP	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04662-01XE	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04662-01YE	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04662-02ZE	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVC373A-EP :

Catalog: SN74LVC373A

- Automotive: SN74LVC373A-Q1
- Military: SN54LVC373A

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military QML certified for Military and Defense Applications

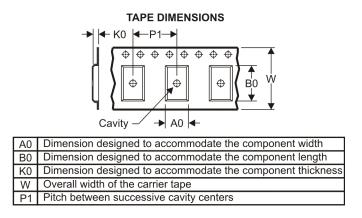
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Раскаде Туре	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC373AMDBREP	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVC373AQDWREP	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LVC373AQPWREP	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TEXAS INSTRUMENTS

www.ti.com

PACKAGE MATERIALS INFORMATION

5-May-2011



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC373AMDBREP	SSOP	DB	20	2000	346.0	346.0	33.0
SN74LVC373AQDWREP	SOIC	DW	20	2000	346.0	346.0	41.0
SN74LVC373AQPWREP	TSSOP	PW	20	2000	346.0	346.0	33.0

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

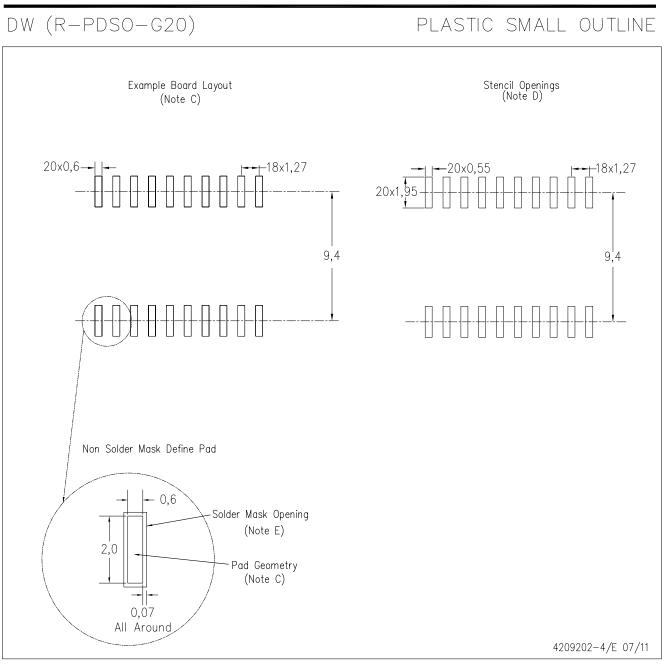
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AC.



LAND PATTERN DATA



NOTES:

A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. β . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



MECHANICAL DATA

MSSO002E - JANUARY 1995 - REVISED DECEMBER 2001

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150



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