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300-W STEREO / 400-W MONO PurePath™ HD ANALOG-INPUT POWER STAGE

Check for Samples: TAS5630B

FEATURES

- PurePath[™] HD Enabled Integrated Feedback Provides:
 - Signal Bandwidth up to 80 kHz for **High-Frequency Content From HD Sources**
 - Ultralow 0.03% THD at 1 W into 4 Ω
 - Flat THD at all Frequencies for Natural Sound
 - 80-dB PSRR (BTL, No Input Signal)
 - >100-dB (A-weighted) SNR
 - Click- and Pop-Free Start-Up
- **Multiple Configurations Possible on the Same** PCB With Stuffing Options:
 - Mono Parallel Bridge-Tied Load (PBTL)
 - Stereo Bridge-Tied Load (BTL)
 - 2.1 Single-Ended Stereo Pair and **Bridge-Tied Load Subwoofer**
 - Quad Single-Ended Outputs
- Total Output Power at 10% THD+N
 - 400 W in Mono PBTL Configuration
 - 300 W per Channel in Stereo BTL Configuration
 - 145 W per Channel in Quad Single-Ended Configuration
- High-Efficiency Power Stage (>88%) With . 60-mΩ Output MOSFETs
- **Two Thermally Enhanced Package Options:**
 - PHD (64-Pin QFP)
 - DKD (44-Pin PSOP3)
- Self-Protection Design (Including Undervoltage, Overtemperature, Clipping, and Short-Circuit Protection) With Error Reporting
- **EMI Compliant When Used With** Recommended System Design

APPLICATIONS

- Mini Combo System
- **AV Receivers**
- **DVD Receivers**
- **Active Speakers**

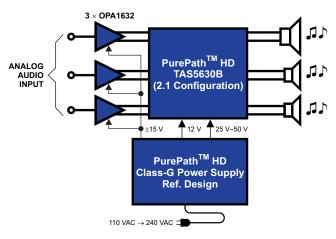
DESCRIPTION

The TAS5630B is a high-performance analog-input amplifier with integrated closed-loop class-D feedback technology (known as PurePath HD technology) with the ability to drive up to 300 W⁽¹⁾ stereo into $4-\Omega$ to $8-\Omega$ speakers from a single 50-V supply.

PurePath HD technology enables traditional AB-amplifier performance (<0.03% THD) levels while providing the power efficiency of traditional class-D amplifiers.

Unlike traditional class-D amplifiers, the distortion curve does not increase until the output levels move into clipping.

PurePath HD technology enables lower idle losses, making the device even more efficient. Coupled with TI's class-G power-supply reference design for TAS563x, industry-leading levels of efficiency can be achieved.



(1) Achievable output power levels are dependent on the thermal configuration of the target application. A high-performance thermal interface material between the exposed package heat slug and the heat sink should be used to achieve high output power levels.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

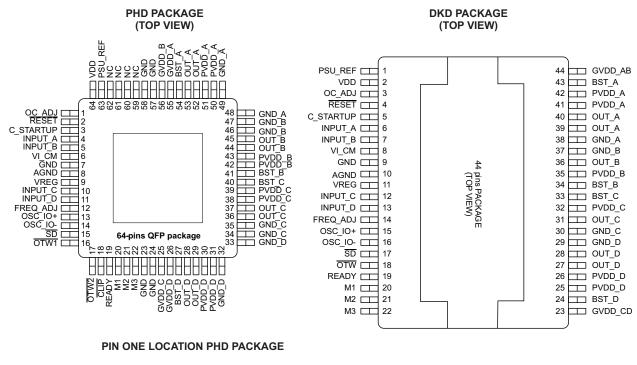
DEVICE INFORMATION

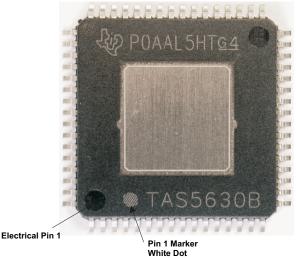
Terminal Assignment

The TAS5630B is available in two thermally enhanced packages:

- 64-Pin QFP (PHD) power package
- 44-Pin PSOP3 package (DKD)

The package types contain heat slugs that are located on the top side of the device for convenient thermal coupling to the heat sink.







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MODE SELECTION PINS

M	ODE PI	NS				DECODIDION			
M3	M2	M1	ANALOG INPUT	CONFIGURATION	DESCRIPTION				
0	0	0	Differential	2 × BTL	AD mode				
0	0	1	_	—	Reserved				
0	1	0	Differential	2 × BTL	BD mode	BD mode			
0	1	1	Differential single-ended	1 × BTL +2 ×SE	BD mode, BTL differential				
1	0	0	Single-ended	4 × SE	AD mode				
					INPUT_C ⁽¹⁾	INPUT_D ⁽¹⁾			
1	0	1	Differential	1 × PBTL	0	0	AD mode		
			1	0	BD mode				
1	1	0			Decembed				
1	1	1		Reserved					

(1) INPUT_C and D are used to select between a subset of AD and BD mode operations in PBTL mode (1=VREG and 0=AGND).

THERMAL INFORMATION

	THERMAL METRIC ⁽¹⁾⁽²⁾	TAS5	630B	
		PHD (64 Pins)	DKD (44 Pins)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	8.5	9.3	
θ_{JCtop}	Junction-to-case (top) thermal resistance	0.2	0.6	
θ_{JB}	Junction-to-board thermal resistance	20.6	3.7	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.2	1.3	C/VV
ψ_{JB}	Junction-to-board characterization parameter	0.73	3.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	8.2	19.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

(2) Thermal model data was performed using a 40 x 40 x 90mm heat-sink

Table 1. ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE	DESCRIPTION
0°C–70°C	TAS5630BPHD	64-pin HTQFP
0°C–70°C	TAS5630BDKD	44-pin PSOP3

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted ⁽¹⁾

		VALUE	UNIT
VDD to AGND		-0.3 to 13.2	V
GVDD to AGND		-0.3 to 13.2	V
PVDD_X to GND_X ⁽²⁾		-0.3 to 69	V
OUT_X to GND_X ⁽²⁾		-0.3 to 69	V
BST_X to GND_X ⁽²⁾		-0.3 to 82.2	V
BST_X to GVDD_X ⁽²⁾		-0.3 to 69	V
VREG to AGND		-0.3 to 4.2	V
GND_X to GND		-0.3 to 0.3	V
GND_X to AGND		-0.3 to 0.3	V
OC_ADJ, M1, M2, M3, OSC_IO+, OSC_IO	O–, FREQ_ADJ, VI_CM, C_STARTUP, PSU_REF to AGND	-0.3 to 4.2	V
INPUT_X		-0.3 to 7	V
RESET, SD, OTW1, OTW2, CLIP, READ	Y to AGND	-0.3 to 7	V
Continuous sink current (SD, OTW1, OTW	V2, CLIP, READY)	9	mA
Operating junction temperature range, T_{J}		0 to 150	°C
Storage temperature, T _{stg}		-40 to 150	°C
	Human-body model ⁽³⁾ (all pins)	±2	kV
Electrostatic discharge	Charged-device model ⁽³⁾ (all pins)	±500	V

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) These voltages represents the dc voltage + peak ac waveform measured at the terminal of the device in all conditions.
(3) Failure to follow good anti-static ESD handling during manufacture and rework contributes to device malfunction. Ensure operators handling the device are adequately grounded through the use of ground straps or alternative ESD protection.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
PVDD_x	Half-bridge supply	DC supply voltage	25	50	52.5	V
GVDD_x	Supply for logic regulators and gate-drive circuitry	DC supply voltage	10.8	12	13.2	V
VDD	Digital regulator supply voltage	DC supply voltage	10.8	12	13.2	V
R _L (BTL)			3.5	4		
R _L (SE) ⁽²⁾	Load impedance ⁽¹⁾	Output filter according to schematics in the application information section	1.8	2		Ω
R _L (PBTL) ⁽²⁾			25 50 52.5 10.8 12 13.2 10.8 12 13.2 3.5 4			
L _{OUTPUT} (BTL)			7	10		
L _{OUTPUT} (SE) ⁽²⁾	Output filter inductance (1)	Minimum output inductance at I _{OC}	7	15		μH
L _{OUTPUT} (PBTL) ⁽²⁾			7	10		
		Nominal	385	400	400 415	
f _{PWM}	PWM frame rate selectable for AM interference avoidance; 1% resistor tolerance.	AM1	315	333	350	kHz
		AM2	260	300	52.5 13.2 13.2 13.2 13.2 13.2 13.2 13.2 13.2	
		Nominal; master mode	9.9	10	10.1	
R _{FREQ_ADJ}	PWM frame-rate-programming resistor	AM1; master mode	19.8	20	20.2	kΩ
		AM2; master mode	29.7	30	30.3	
V _{FREQ_ADJ}	Voltage on FREQ_ADJ pin for slave mode operation	Slave mode		3.3		V
	Overcurrent-protection-programming resistor,	64-pin QFP package (PHD)	22		33	
R _{OCP}	cycle-by-cycle mode	44-Pin PSOP3 package (DKD)	24		33	kΩ
· · · · · · · · · · · · · · · · · · ·	Overcurrent-protection-programming resistor, latching mode	PHD or DKD	47		68	1122
TJ	Junction temperature		0		125	°C

(1) Values are for actual measured impedance over all combinations of tolerance, current and temperature and not simply the component rating.

(2) See additional details for SE and PBTL in the System Design Considerations section.

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PIN FUNCTIONS							
	PIN		Function ⁽¹⁾	DESCRIPTION			
NAME	PHD NO.	DKD NO.					
AGND	8	10	Р	Analog ground			
BST_A	54	43	Р	HS bootstrap supply (BST), external 0.033-µF capacitor to OUT_A required.			
BST_B	41	34	Р	HS bootstrap supply (BST), external 0.033-µF capacitor to OUT_B required.			
BST_C	40	33	Р	HS bootstrap supply (BST), external 0.033-µF capacitor to OUT_C required.			
BST_D	27	24	Р	HS bootstrap supply (BST), external 0.033-µF capacitor to OUT_D required.			
CLIP	18	—	0	Clipping warning; open drain; active-low			
C_STARTUP	3	5	0	Start-up ramp requires a charging capacitor of 4.7 nF to AGND in BTL mode			
FREQ_ADJ	12	14	I	PWM frame-rate-programming pin requires resistor to AGND			
GND	7, 23, 24, 57, 58	9	Р	Ground			
GND_A	48, 49	38	Р	Power ground for half-bridge A			
GND_B	46, 47	37	Р	Power ground for half-bridge B			
GND_C	34, 35	30	Р	Power ground for half-bridge C			
GND_D	32, 33	29	Р	Power ground for half-bridge D			
GVDD_A	55	—	Р	Gate-drive voltage supply requires 0.1-µF capacitor to GND_A			
GVDD_B	56	—	Р	Gate drive voltage supply requires 0.1-µF capacitor to GND_B			
GVDD_C	25	_	Р	Gate drive voltage supply requires 0.1-µF capacitor to GND_C			
GVDD_D	26	-	Р	Gate drive voltage supply requires 0.1-µF capacitor to GND_D			
GVDD_AB	_	44	Р	Gate drive voltage supply requires 0.22-µF capacitor to GND_A/GND_B			
GVDD_CD	_	23	Р	Gate drive voltage supply requires 0.22-µF capacitor to GND_C/GND_D			
INPUT_A	4	6	I	Input signal for half-bridge A			
INPUT_B	5	7	I	Input signal for half-bridge B			
INPUT_C	10	12	I	Input signal for half-bridge C			
INPUT_D	11	13	I	Input signal for half-bridge D			
M1	20	20	Ι	Mode selection			
M2	21	21	Ι	Mode selection			
M3	22	22	Ι	Mode selection			
NC	59–62	_	_	No connect; pins may be grounded.			
OC_ADJ	1	3	0	Analog overcurrent-programming pin requires resistor to AGND. 64-pin package (PHD) = 22 k Ω . 44-pin PSOP3 (DKD) = 24 k Ω			
OSC_IO+	13	15	I/O	Oscillator master/slave output/input			
OSC_IO-	14	16	I/O	Oscillator master/slave output/input			
OTW	_	18	0	Overtemperature warning signal, open-drain, active-low			
OTW1	16	_	0	Overtemperature warning signal, open-drain, active-low			
OTW2	17	_	0	Overtemperature warning signal, open-drain, active-low			
OUT_A	52, 53	39, 40	0	Output, half-bridge A			
OUT_B	44, 45	36	0	Output, half-bridge B			
OUT_C	36, 37	31	0	Output, half-bridge C			
OUT_D	28, 29	27, 28	0	Output, half-bridge D			
PSU_REF	63	1	P	PSU reference requires close decoupling of 330 pF to AGND.			
PVDD_A	50, 51	41, 42	P	Power-supply input for half-bridge A requires close decoupling of $0.01-\mu$ F capacitor in parallel with 2.2- μ F capacitor to GND_A.			
PVDD_B	42, 43	35	Р	Power-supply input for half-bridge B requires close decoupling of $0.01-\mu$ F capacitor in parallel with 2.2- μ F capacitor to GND_B.			
PVDD_C	38, 39	32	Р	Power-supply input for half-bridge C requires close decoupling of 0.0- μ F capacitor in parallel with 2.2- μ F capacitor to GND_C.			

(1) I = Input, O = Output, P = Power



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PIN FUNCTIONS (continued)

PIN			Function ⁽¹⁾	
NAME	PHD NO.	DKD NO.	Function	DESCRIPTION
PVDD_D	30, 31	25, 26	Р	Power-supply input for half-bridge D requires close decoupling of 0.01 - μ F capacitor in parallel with 2.2 - μ F capacitor to GND_D.
READY	19	19	0	Normal operation; open-drain; active-high
RESET	2	4	Ι	Device reset input; active-low
SD	15	17	0	Shutdown signal, open-drain, active-low
VDD	64	2	Р	Power supply for digital voltage regulator requires a $10-\mu F$ capacitor in parallel with a $0.1-\mu F$ capacitor to GND for decoupling.
VI_CM	6	8	0	Analog comparator reference node requires close decoupling of 1 nF to AGND.
VREG	9	11	Р	Digital regulator supply filter pin requires 0.1-µF capacitor to AGND.

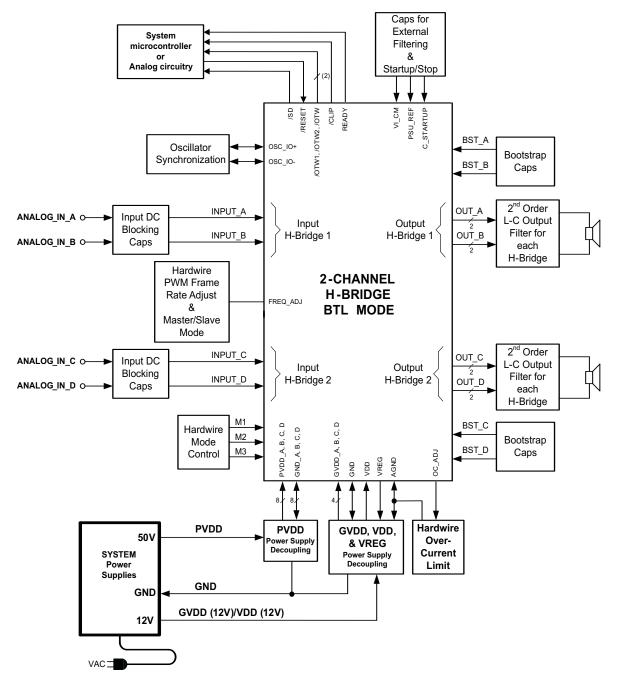
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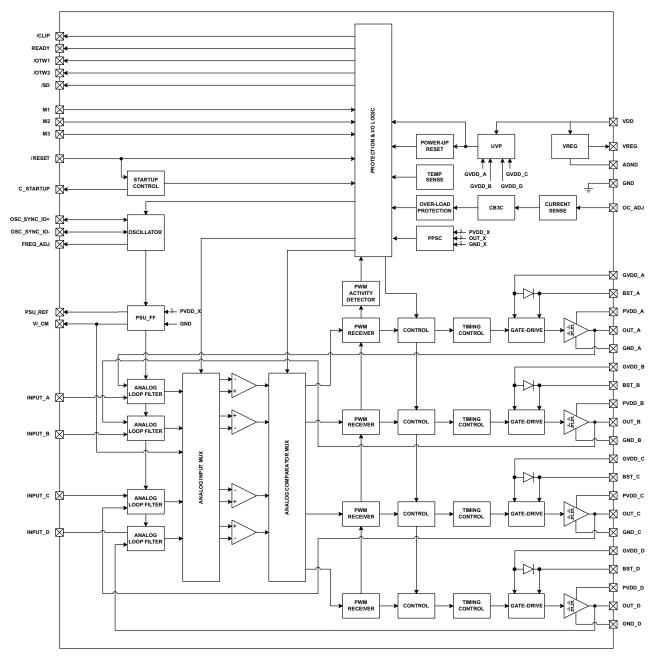
TYPICAL SYSTEM BLOCK DIAGRAM



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TEXAS INSTRUMENTS

FUNCTIONAL BLOCK DIAGRAM



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AUDIO CHARACTERISTICS (BTL)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 50 V, GVDD_X = 12 V, R_L = 4 Ω , f_S = 400 kHz, R_{OC} = 22 k Ω , T_C = 75°C; output filter: L_{DEM} = 7 μ H, C_{DEM} = 680 nF, MODE = 010, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
		$R_L = 4 \Omega$, 10% THD+N, clipped output signal	300		
		$R_L = 6 \Omega$, 10% THD+N, clipped output signal	signal 300 signal 210 signal 160 t signal 240 t signal 160 t signal 125 0.03%		
Po Power output per channel	$R_L = 8 \Omega$, 10% THD+N, clipped output signal	160		W	
Po	Power output per channel	$R_L = 4 \Omega$, 1% THD+N, unclipped output signal	240	300 210 160 240 160 220 03% 270 20 50 100 100	vv
		$R_L = 6 \Omega$, 1% THD+N, unclipped output signal	160		
		$R_L = 8 \Omega$, 1% THD+N, unclipped output signal	125))))))))))))))))))	
THD+N	Total harmonic distortion + noise	1 W	0.03%		
V _n	Output integrated noise	A-weighted, AES17 filter, input capacitor grounded	270		μV
V _{OS}	Output offset voltage	Inputs ac-coupled to AGND	20	50	mV
SNR	Signal-to-noise ratio ⁽¹⁾	A-weighted, AES17 filter	100		dB
DNR	Dynamic range	A-weighted, AES17 filter	100		dB
P _{idle}	Power dissipation due to idle losses (I _{PVDD_X})	$P_O = 0$, four channels switching ⁽²⁾	2.7		W

(1) SNR is calculated relative to 1% THD+N output level.

(2) Actual system idle losses also are affected by core losses of output inductors.

AUDIO SPECIFICATION (Single-Ended Output)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1kHz, PVDD_X = 50 V, GVDD_X = 12 V, R_L = 4 Ω , f_S = 400 kHz, R_{OC} = 22 k Ω , T_C = 75°C; output filter: L_{DEM} = 15 μ H, C_{DEM} = 470 μ F, MODE = 100, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
		$R_L = 2 \Omega$, 10% THD+N, clipped output signal	145	145 100 75 110 75 55	
		$R_L = 3 \Omega$, 10% THD+N, clipped output signal	145 100 75 110 75 0.07% ed 340 93 93		
		$R_L = 4 \Omega$, 10% THD+N, clipped output signal	75	145 100 75 110 75 55 .07% 340 93 93	
Po	Power output per channel	$R_L = 2 \Omega$, 1% THD+N, unclipped output signal	110		W
		$R_L = 3 \Omega$, 1% THD+N, unclipped output signal	75		
		$R_L = 4 \Omega$, 1% THD+N, unclipped output signal	55	MAX	
THD+N	Total harmonic distortion + noise	1 W	0.07%		
Vn	Output integrated noise	A-weighted, AES17 filter, input capacitor grounded	340		μV
SNR	Signal-to-noise ratio ⁽¹⁾	A-weighted, AES17 filter	93		dB
DNR	Dynamic range	A-weighted, AES17 filter	93		dB
P _{idle}	Power dissipation due to idle losses $(I_{PVDD X})$	$P_O = 0$, four channels switching ⁽²⁾	2		W

(1) SNR is calculated relative to 1% THD+N output level.

(2) Actual system idle losses are affected by core losses of output inductors.



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AUDIO SPECIFICATION (PBTL)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 50 V, GVDD_X = 12 V, R_L = 3 Ω , f_S = 400 kHz, R_{OC} = 22 k Ω , T_C = 75°C; output filter: L_{DEM} = 7 μ H, C_{DEM} = 1.5 μ F, MODE = 101-10, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
		$R_L = 3 \Omega$, 10% THD+N, clipped output signal	400		
		$ \begin{array}{c} R_L = 3 \ \Omega, 10\% \ \text{THD+N}, \text{clipped output signal} & 400 \\ R_L = 4 \ \Omega, 10\% \ \text{THD+N}, \text{clipped output signal} & 300 \\ R_L = 2 \ \Omega, 1\% \ \text{THD+N}, \text{unclipped output signal} & 480 \\ R_L = 3 \ \Omega, 1\% \ \text{THD+N}, \text{unclipped output signal} & 310 \\ R_L = 4 \ \Omega, 1\% \ \text{THD+N}, \text{unclipped output signal} & 230 \\ \end{array} $			
Po	Power output per channel	$R_L = 2 \Omega$, 1% THD+N, unclipped output signal	480	400 300 480 310 230 0.05% 260 100 100	W
		$R_L = 3 \Omega$, 1% THD+N, unclipped output signal	310		
		$R_L = 4 \Omega$, 1% THD+N, unclipped output signal	230		
THD+N	Total harmonic distortion + noise	1 W	0.05%		
V _n	Output integrated noise	A-weighted	260		μV
SNR	Signal to noise ratio ⁽¹⁾	A-weighted	100		dB
DNR	Dynamic range	A-weighted	100		dB
P _{idle}	Power dissipation due to idle losses (IPVDD_X)	$P_O = 0$, four channels switching ⁽²⁾	2.7		W

(1) SNR is calculated relative to 1% THD-N output level.

(2) Actual system idle losses are affected by core losses of output inductors.

ELECTRICAL CHARACTERISTICS

PVDD_X = 50 V, GVDD_X = 12 V, VDD = 12 V, T _c (Case temperature) = 75°C, f _s = 400 kHz, unless otherwise s	specified.
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	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL \	OLTAGE REGULATOR AND CURRENT CONSU	IMPTION	I.			
VREG	Voltage regulator, only used as reference node, VREG	VDD = 12 V	3	3.3	3.6	V
VI_CM	Analog comparator reference node, VI_CM		1.5	1.75	1.9	V
		Operating, 50% duty cycle		22.5		A
I _{VDD}	VDD supply current	Idle, reset mode		22.5		mA
		50% duty cycle		12.5		A
I _{GVDD_X}	GVDD_x gate-supply current per half-bridge	Reset mode		1.5		mA
I _{PVDD X} Half-bridge supply current		50% duty cycle with recommended output filter	13.3			mA
		Reset mode, No switching		870		μA
ANALOG IN	PUTS					
R _{IN}	Input resistance	READY = HIGH		33		kΩ
V _{IN}	Maximum input voltage swing			3.5		V_{PP}
I _{IN}	Maximum input current			342		μA
G	Voltage gain (V _{OUT} /V _{IN})			23		dB
OSCILLATO	R					
	Nominal, master mode		3.85	4	4.15	
f _{OSC_IO+}	AM1, master mode	F _{PWM} × 10	3.15	3.33	3.5	MHz
	AM2, master mode		2.6	3	3.35	
V _{IH}	High level input voltage		1.86			V
V _{IL}	Low level input voltage				1.45	V
OUTPUT-ST	AGE MOSFETs	·				
2	Drain-to-source resistance, low side (LS)	$T_1 = 25^{\circ}C$, excludes metallization		60	100	mΩ
R _{DS(on)}	Drain-to-source resistance, high side (HS)	resistance, GVDD = 12 V		60	100	mΩ



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ELECTRICAL CHARACTERISTICS (continued)

PVDD_X = 50 V, GVDD_X = 12 V, VDD = 12 V, T_C (Case temperature) = 75°C, f_S = 400 kHz, unless otherwise specified.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I/O PROTECT	ION					
V _{uvp,G}	Undervoltage protection limit, GVDD_x and VDD			9.5		V
V _{uvp,hyst} ⁽¹⁾				0.6		V
OTW1 ⁽¹⁾	Overtemperature warning 1		95	100	105	°C
OTW2 ⁽¹⁾	Overtemperature warning 2		115	125	135	°C
OTW _{hyst} ⁽¹⁾	Temperature drop needed below OTW temperature for OTW to be inactive after OTW event			25		°C
OTE ⁽¹⁾	Overtemperature error		145	155	165	°C
OTE	OTE-OTW differential			30		°C
OTE _{hyst} ⁽¹⁾	A reset must occur for SD to be released following an OTE event.			25		°C
OLPC	Overload protection counter	f _{PWM} = 400 kHz		2.6		ms
	Overeurrent limit protection	Resistor – programmable, nominal peak current in 1- Ω load, 64-pin QFP package (PHD) R _{OCP} = 22 k Ω		15		A
l _{oc}	Overcurrent limit protection	Resistor – programmable, nominal peak current in 1- Ω load, 44-Pin PSOP3 package (DKD), R _{OCP} = 24 k Ω		15		A
	Overcurrent limit protection, latched	Resistor – programmable, nominal peak current in 1- Ω load, R _{OCP} = 47 k Ω		15		А
I _{OCT}	Overcurrent response time	Time from switching transition to flip-state induced by overcurrent		150		ns
I _{PD}	Internal pulldown resistor at output of each half-bridge	Connected when RESET is active to provide bootstrap charge. Not used in SE mode		3		mA
STATIC DIGIT	TAL SPECIFICATIONS		1			1
V _{IH}	High-level input voltage		2			V
V _{IL}	Low-level input voltage	- INPUT_X, M1, M2, M3, RESET			0.8	V
l _{lkg}	Input leakage current				100	μA
OTW/SHUTDO	OWN (SD)	•				
R _{INT_PU}	Internal pullup resistance, OTW, OTW1, OTW2, CLIP, READY, SD to VREG		20	26	32	kΩ
		Internal pullup resistor	3	3.3	3.6	
V _{OH}	High-level output voltage	External pullup of 4.7 k Ω to 5 V	4.5 5			V
V _{OL}	Low-level output voltage	$I_{O} = 4 \text{ mA}$		200	500	mV
FANOUT	Device fanout OTW, OTW1, OTW2, SD, CLIP, READY	No external pullup		30		devices

(1) Specified by design.

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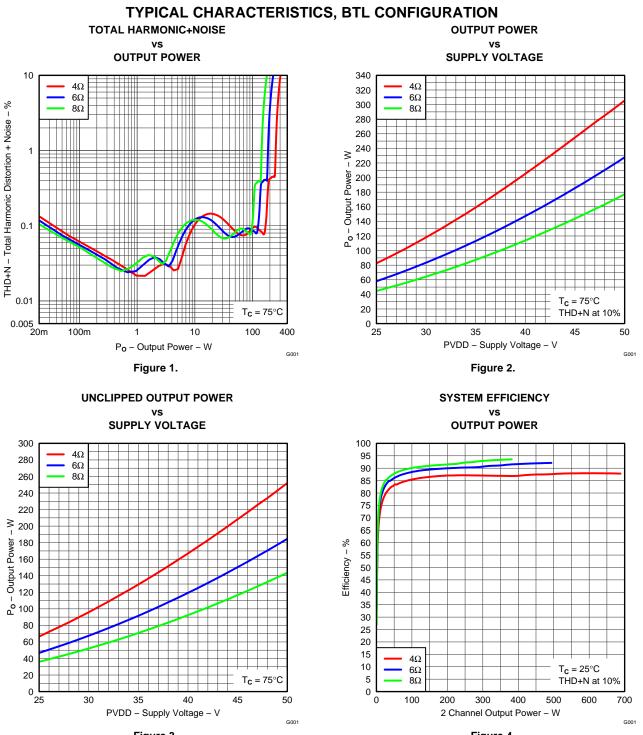
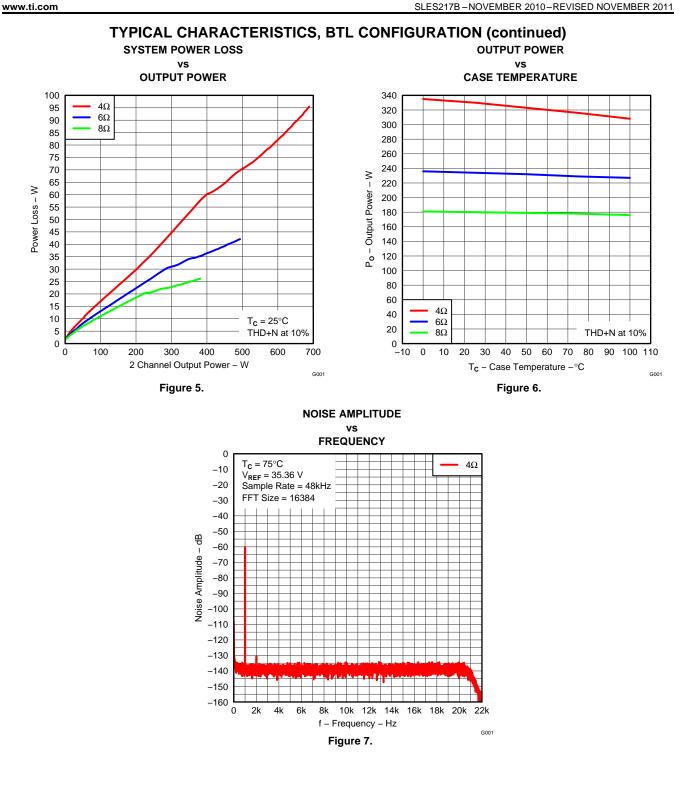




Figure 4.





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THD+N – Total Harmonic Distortion + Noise – %

2Ω

30

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TOTAL HARMONIC DISTORTION + NOISE

vs

OUTPUT POWER

OUTPUT POWER vs

SUPPLY VOLTAGE

150 4Ω 4Ω 140 130 120 Po - Output Power - W 110 - Output Power - W 100 - Output Power - W 50 40 30 20 10 $T_c = 75^{\circ}C$ 0 L 25 100m 10 100 200 30 35 40 1 PVDD – Supply Voltage – V Po - Output Power - W G001 Figure 8. Figure 9. OUTPUT POWER vs CASE TEMPERATURE 180 170 160 150 140 130 Po – Output Power – W 120 110 100 90 80 70 60 50 40 30 2Ω 20 3Ω 10 THD+N at 10% 4Ω

TYPICAL CHARACTERISTICS, SE CONFIGURATION 1 Channel Driven

170

160

2Ω

3Ω

30 40 50 60

70

80

90 100 110

G001

0 _10 0

10 20

T_c = 75°C

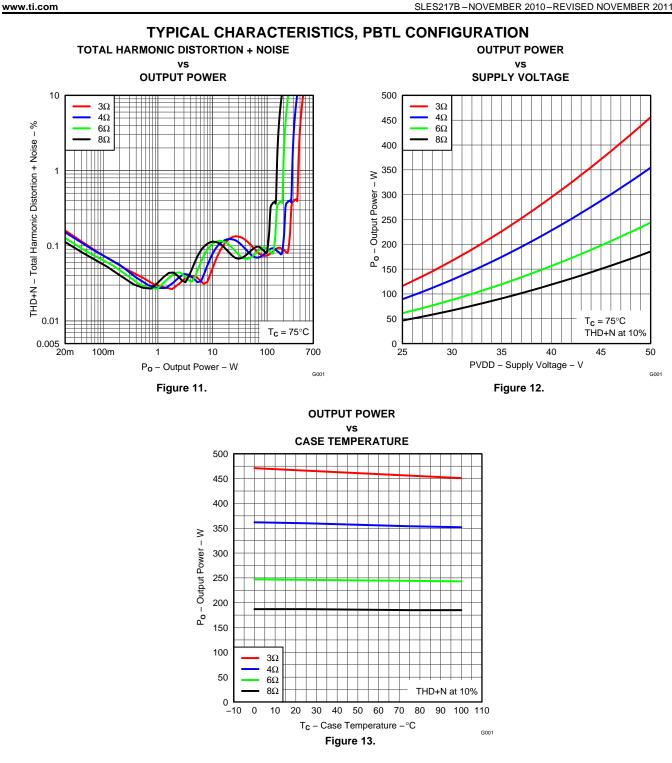
45

THD+N at 10%

50

G001

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NSTRUMENTS



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APPLICATION INFORMATION

PCB MATERIAL RECOMMENDATION

FR-4 2-oz. (70-µm) glass epoxy material is recommended for use with the TAS5630B. The use of this material can provide for higher power output, improved thermal performance, and better EMI margin (due to lower PCB trace resistance).

PVDD CAPACITOR RECOMMENDATION

The large capacitors used in conjunction with each full bridge are referred to as the PVDD capacitors. These capacitors should be selected for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well-designed system power supply, 1000 μ F, 63-V supports more applications. The PVDD capacitors should be the low-ESR type, because they are used in a circuit associated with high-speed switching.

DECOUPLING CAPACITOR RECOMMENDATIONS

To design an amplifier that has robust performance, passes regulatory requirements, and exhibits good audio performance, quality decoupling capacitors should be used. In practice, X7R should be used in this application.

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. This fact is particularly true in the selection of the 2.2- μ F capacitor that is placed on the power supply to each half-bridge. It must withstand the voltage overshoot of the PWM switching, the heat generated by the amplifier during high power output, and the ripple current created by high power output. A minimum voltage rating of 63 V is required for use with a 50-V power supply.

SYSTEM DESIGN RECOMMENDATIONS

The following schematics and PCB layouts illustrate best practices used for the TAS5630B.

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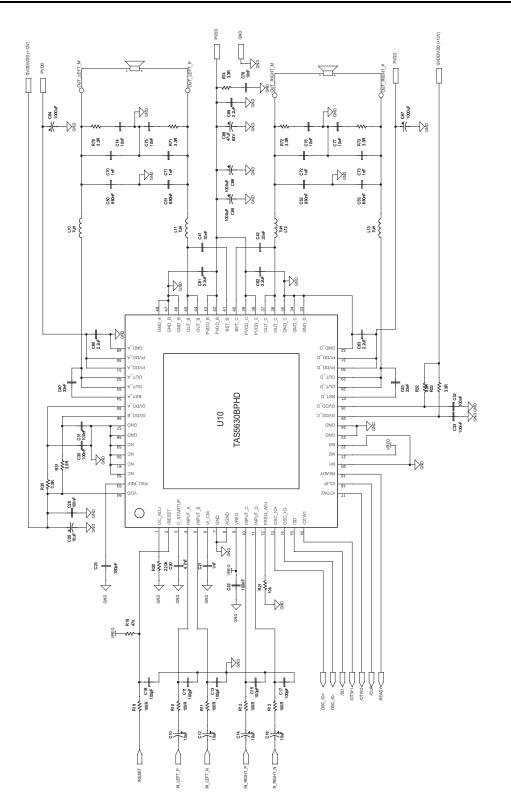


Figure 14. Typical Differential-Input BTL Application With BD Modulation Filters



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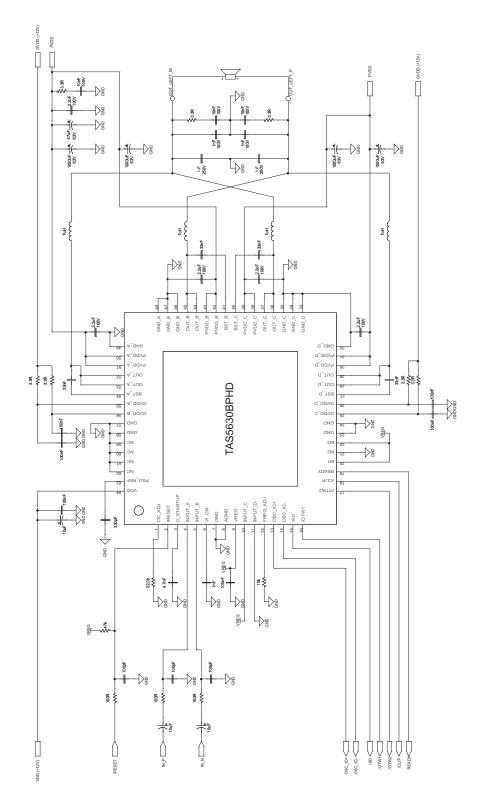


Figure 15. Typical Differential (2N) PBTL Application With BD Modulation Filters

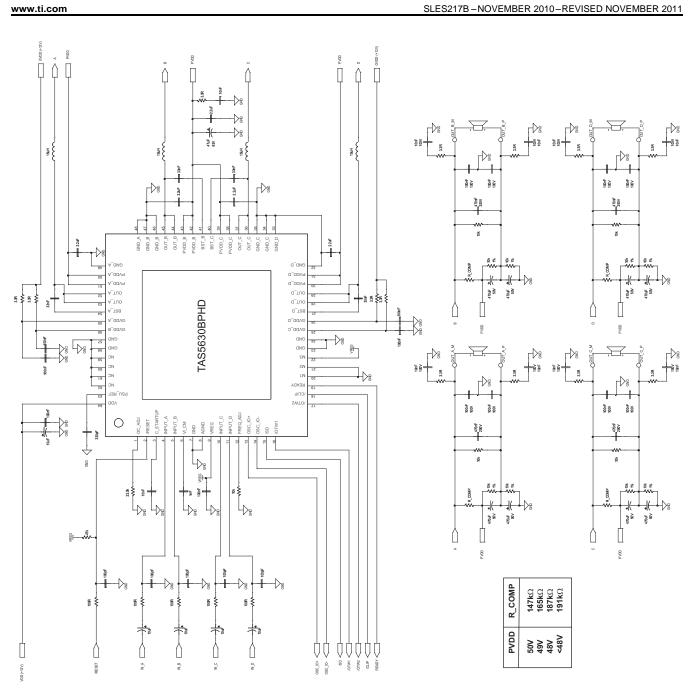


Figure 16. Typical SE Application





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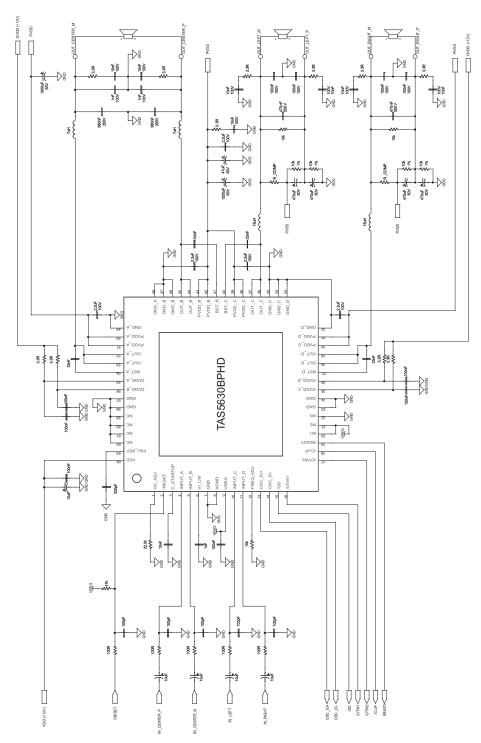
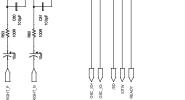


Figure 17. Typical 2.1 System Differential-Input BTL and Unbalanced-Input SE Application

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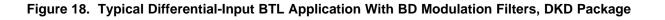
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THEORY OF OPERATION

POWER SUPPLIES

To facilitate system design, the TAS5630B needs only a 12-V supply in addition to the (typical) 50-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only an external capacitor for each half-bridge.

To provide outstanding electrical and acoustical characteristics, the PWM signal path, including gate drive and output stage, is designed as identical, independent half-bridges. For this reason, each half-bridge has separate gate drive supply pins (GVDD_X), bootstrap pins (BST_X), and power-stage supply pins (PVDD_X). Furthermore, an additional pin (VDD) is provided as supply for all common circuits. Although supplied from the same 12-V source, it is highly recommended to separate GVDD_A, GVDD_B, GVDD_C, GVDD_D, and VDD on the printed-circuit board (PCB) by RC filters (see application diagram for details). These RC filters provide the recommended high-frequency isolation. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided. (See reference board documentation for additional information.)

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 300 kHz to 400 kHz, it is recommended to use 33-nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X pin is decoupled with a 2.2-µF ceramic capacitor placed as close as possible to each supply pin. It is recommended to follow the PCB layout of the TAS5630B reference design. For additional information on recommended power supply and required components, see the application diagrams in this data sheet.

The 12-V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 50-V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit. Moreover, the TAS5630B is fully protected against erroneous power-stage turnon due to parasitic gate charging. Thus, voltage-supply ramp rates (dV/dt) are non-critical within the specified range (see the Recommended Operating Conditions table of this data sheet).

SYSTEM POWER-UP/POWER-DOWN SEQUENCE

Powering Up

The TAS5630B does not require a power-up sequence. The outputs of the H-bridges remain in a high-impedance state until the gate-drive supply voltage (GVDD_X) and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* table of this data sheet). Although not specifically required, it is recommended to hold RESET in a low state while powering up the device. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output.

Powering Down

The TAS5630B does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* table of this data sheet). Although not specifically required, it is a good practice to hold RESET low during power down, thus preventing audible artifacts including pops or clicks.

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ERROR REPORTING

The SD, OTW, OTW1 and OTW2 pins are active-low, open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown is signaled by the \overline{SD} pin going low. Likewise, \overline{OTW} and $\overline{OTW2}$ go low when the device junction temperature exceeds 125°C and $\overline{OTW1}$ goes low when the junction temperature exceeds 100°C (see the following table).

SD	OTW1	OTW2, OTW	DESCRIPTION
0	0	0	Overtemperature (OTE) or overload (OLP) or undervoltage (UVP)
0	0	1	Overload (OLP) or undervoltage (UVP). Junction temperature higher than 100°C (overtemperature warning)
0	1	1	Overload (OLP) or undervoltage (UVP)
1	0	0	Junction temperature higher than 125°C (overtemperature warning)
1	0	1	Junction temperature higher than 100°C (overtemperature warning)
1	1	1	Junction temperature lower than 100°C and no OLP or UVP faults (normal operation)

Note that asserting either $\overrightarrow{\text{RESET}}$ low forces the $\overrightarrow{\text{SD}}$ signal high, independent of faults being present. TI recommends monitoring the OTW signal using the system microcontroller and responding to an overtemperature warning signal by, e.g., turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

To reduce external component count, an internal pullup resistor to 3.3 V is provided on both \overline{SD} and \overline{OTW} outputs. Level compliance for 5-V logic can be obtained by adding external pullup resistors to 5 V (see the *Electrical Characteristics* table of this data sheet for further specifications).

DEVICE PROTECTION SYSTEM

The TAS5630B contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overload, overtemperature, and undervoltage. The TAS5630B responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the SD pin low. In situations other than overload and overtemperature error (OTE), the device automatically recovers when the fault condition has been removed, i.e., the supply voltage has increased.

BTL	Mode	PBTL	. Mode	SE Mode		
Local error in	Turns Off or in	Local error in	Turns Off or in	Local error in	Turns Off or in	
А	A . D	A		A		
В	A + B	В		В	A + B	
С	0.0	С	A + B + C + D	С	0.5	
D	C + D	D	_	D	C + D	

The device functions on errors, as shown in the following table.

Bootstrap UVP does not shut down according to the table; it shuts down the respective half-bridge.

PIN-TO-PIN SHORT-CIRCUIT PROTECTION (PPSC)

The PPSC detection system protects the device from permanent damage if a power output pin (OUT_X) is shorted to GND_X or PVDD_X. For comparison, the OC protection system detects an overcurrent after the demodulation filter, whereas PPSC detects shorts directly at the pin before the filter. PPSC detection is performed at startup, i.e., when VDD is supplied; consequently, a short to either GND_X or PVDD_X after system startup does not activate the PPSC detection system. When PPSC detection is activated by a short on the output, all half-bridges are kept in a Hi-Z state until the short is removed; the device then continues the startup sequence and starts switching. The detection is controlled globally by a two-step sequence. The first step ensures that there are no shorts from OUT_X to GND_X; the second step tests that there are no shorts from OUT_X to PVDD_X.



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filter. The typical duration is <15 ms/ μ F. While the PPSC detection is in progress, \overline{SD} is kept low, and the device does not react to changes applied to the RESET pins. If no shorts are present the PPSC detection passes, and SD is released, a device reset does not start a new PPSC detection. PPSC detection is enabled in BTL and PBTL output configurations; the detection is not performed in SE mode. To make sure the PPSC detection system is not tripped, it is recommended not to insert resistive load between OUT_X and GND_X or PVDD_X.

OVERTEMPERATURE PROTECTION

The two different package options have individual overtemperature protection schemes.

PHD Package:

The TAS5630B PHD package option has a three-level temperature-protection system that asserts an active-low warning signal (OTW1) when the device junction temperature exceeds 100°C (typical), (OTW2) when the device junction temperature exceeds 155°C (typical) and, if the device junction temperature exceeds 155°C (typical), the device is <u>put</u> into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and SD being asserted low. OTE is latched in this case. To clear the OTE latch, RESET must be asserted. Thereafter, the device resumes normal operation. For highest reliability, the RESET should not be asserted until OTW1 has cleared.

DKD Package:

The TAS5630B <u>DKD</u> package option has a two-level temperature-protection system that asserts an active-low warning signal (OTW) when the device junction temperature exceeds 125°C (typical) and, if the device junction temperature exceeds 155°C (typical), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and SD being asserted low. OTE is latched in this case. To clear the OTE latch, RESET must be asserted. It is recommended to wait until OTW has cleared before asserting RESET. Thereafter, the device resumes normal operation.

UNDERVOLTAGE PROTECTION (UVP) AND POWER-ON RESET (POR)

The UVP and POR circuits of the TAS5630B fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach the levels stated in the *Electrical Characteristics* table. Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or <u>GVDD_X</u> pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and SD being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

DEVICE RESET

When RESET is asserted low, all power-stage FETs in the four half-bridges are forced into a high-impedance (Hi-Z) state.

In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the reset input low enables weak pulldown of the half-bridge outputs. In the SE mode, the output is forced into a high-impedance state when asserting the reset input low. Asserting reset input low removes any fault information to be signaled on the SD output; i.e., SD is forced high. A rising-edge transition on reset input allows the device to resume operation after an overload fault. To ensure thermal reliability, the rising edge of reset must occur no sooner than 4 ms after the falling edge of SD.

SYSTEM DESIGN CONSIDERATIONS

A rising-edge transition on the reset input allows the device to execute the startup sequence and starts switching.

Apply audio only when the state of READY is high; that starts and stops the amplifier without having audible artifacts that are heard in the output transducers. If an overcurrent protection event is introduced, the READY signal goes low; hence, filtering is needed if the signal is intended for audio muting in non-microcontroller systems.

The CLIP signal indicates that the output is approaching clipping. The signal can be used either to activate a volume decrease or to signal an intelligent power supply to increase the rail voltage from low to high for optimum efficiency.

The device inverts the audio signal from input to output.



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The VREG pin is not recommended to be used as a voltage source for external circuitry.

Click and Pop in SE-Mode

The BTL startup has low click and pop due to the trimmed output dc offset, see the AUDIO CHARACTERISTICS (BTL) table.

The startup of the BTL+2 x SE system (Figure 17) or 4xSE (Figure 16) is more difficult to get click and pop free, than the pure BTL solution; therefore, evaluating the resulting click and pop before designing in the device is recommended.

PBTL Overload and Short Circuit

The TAS5630B has extensive overload and short circuit protection. In BTL and SE mode, it is fully protected against speaker terminal overloads, terminal-to-terminal short circuit, and short circuit to GND or PVDD. The protection works by limiting the current, by flipping the state of the output MOSFET's; thereby, ramping currents down in the inductor. This only works when the inductor is NOT saturated, the recommended minimum inductor values are listed in RECOMMENDED OPERATING CONDITIONS table. In BTL mode, the short circuit currents can reach more than 15A, so when connecting the device in PBTL mode (Mono), the currents double – that is more than 30A, and with these high currents, the protection system will limit PBTL speaker overloads, terminal-to-terminal shorts, and terminal-to-GND shorts. PBTL mode short circuit to PVDD is not recommended.

OSCILLATOR

The oscillator frequency can be trimmed by external control of the FREQ_ADJ pin.

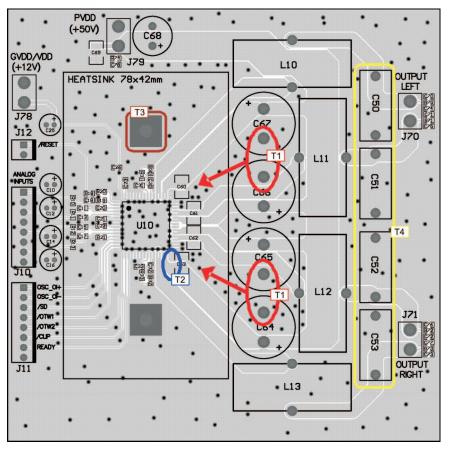
To reduce interference problems while using a radio receiver tuned within the AM band, the switching frequency can be changed from nominal to lower values. These values should be chosen such that the nominal and the lower-value switching frequencies together result in the fewest cases of interference throughout the AM band, and can be selected by the value of the FREQ_ADJ resistor connected to AGND in master mode.

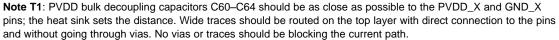
For slave-mode operation, turn off the oscillator by pulling the FREQ_ADJ pin to VREG. This configures the OSC_I/O pins as inputs, which must be slaved from an external clock.

PRINTED CIRCUIT BOARD RECOMMENDATION

Use an unbroken ground plane to have a good low-impedance and -inductance return path to the power supply for power and audio signals. PCB layout, audio performance and EMI are linked closely together. The circuit contains high, fast-switching currents; therefore, care must be taken to prevent damaging voltage spikes. Routing of the audio input should be kept short and together with the accompanying audio-source ground. A local ground area underneath the device is important to keep solid to minimize ground bounce. It is always good practice to follow the EVM layout as a guideline.

Netlist for this printed circuit board is generated from the schematic in Figure 14.





Note T2: Close decoupling of PVDD with low impedance X7R ceramic capacitors is placed under the heat sink and close to the pins. This is valid for C60, C61, C62, and C63.

Note T3: Heat sink must have a good connection to PCB ground.

Note T4: Output filter capacitors must be linear in the applied voltage range, preferably metal film types.

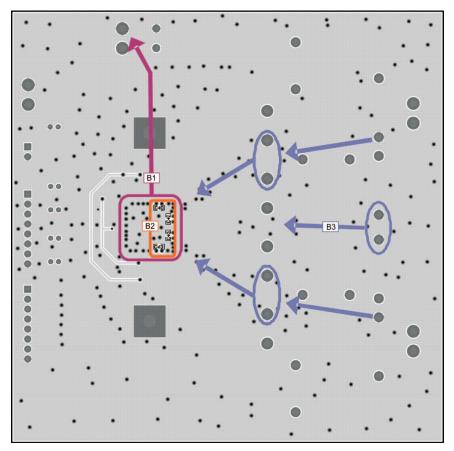
Figure 19. Printed Circuit Board – Top Layer

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Note B1: It is important to have a direct-low impedance return path for high current back to the power supply. Keep impedance low from top to bottom side of PCB through a lot of ground vias.

Note B2: Bootstrap low-impedance X7R ceramic capacitors placed on bottom side provide a short, low-inductance current loop.

Note B3: Return currents from bulk capacitors and output filter capacitors

Figure 20. Printed Circuit Board – Bottom Layer

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REVISION HISTORY

Changes from Original (November 2010) to Revision A

•	Changed Title From: 600-W MONO To 400-W MONO	. 1
•	Changed Feature From: 600 W per Channel in Mono PBTL Configuration To: 400 W per Channel in Mono PBTL Configuration	. 1
•	Changed the Pin One Location Package image	. 2
•	Replaced the PACKAGE HEAT DISSIPATION RATINGS table with the THERMAL INFORMATION table	. 3
•	Changed R _L (PBTL) Load Impedance Min value From: 1.6 Ω To: 2.4 Ω , and Typ value From 2 To: 3 Ω	. 4
•	Added footnotes ⁽¹⁾ and ⁽²⁾ to the ROC table	. 4
•	Added R _{OCP} information to the ROC Table	. 4
•	Deleted - $R_L = 2 \Omega$, 10%, THD+N, clipped input signal From P_O in the Audio Specification (PBTL) table	10
•	Changed the I _{OC} Typical Value From: 19 A To: 15 A	11
•	Replaced the TYPICAL CHARACTERISTICS, PBTL CONFIGURATION graphs	15
•	Added section - Click and Pop in SE-Mode	25
•	Added section - PBTL Overload and Short Circuit	25
		—

(1) See additional details for SE and PBTL in the System Design Considerations section.

(2) Values are for actual measured impedance over all combinations of tolerance, current and temperature and not simply the component rating.

Changes from Revision A (November 2011) to Revision B

	Changed the R _{INT PU} parameters From: OTW1 to VREG, OTW2 to VREG, SD to VREG To: OTW, OTW1, OTW2,	
	CLIP, READY, SD to VRE	11
•	Added text to the PHD Package section.	24
•	Added text to the DKD Package section	24



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Page

Page

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TEXAS INSTRUMENTS





TAPE AND REEL INFORMATION

TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*	All dimensions are nominal												
	Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	TAS5630BDKDR	HSSOP	DKD	44	500	330.0	24.4	14.7	16.4	4.0	20.0	24.0	Q1
	TAS5630BPHDR	HTQFP	PHD	64	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

25-Jan-2012

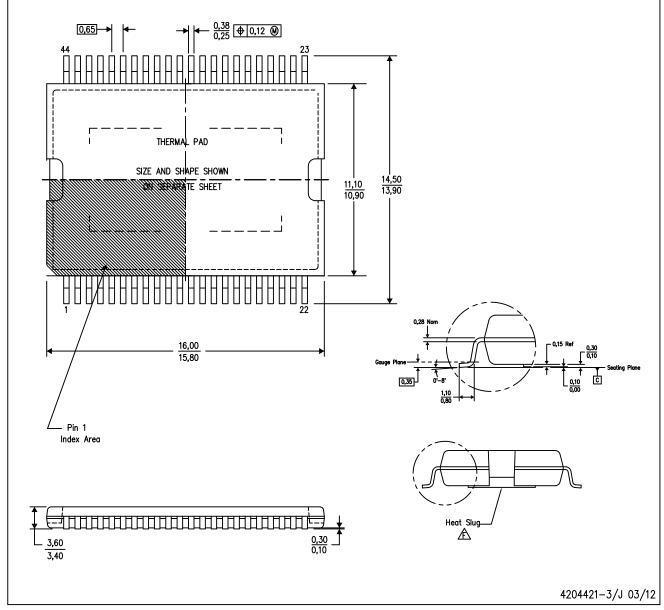


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5630BDKDR	HSSOP	DKD	44	500	346.0	346.0	41.0
TAS5630BPHDR	HTQFP	PHD	64	1000	346.0	346.0	41.0

DKD (R-PDSO-G44)

PowerPAD[™] PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.15mm.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com http://www.ti.com.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- 🛆 The package thermal performance is optimized for conductive cooling with attachment to an external heat sink.

PowerPAD is a trademark of Texas Instruments.



DKD (R-PDSO-G44)

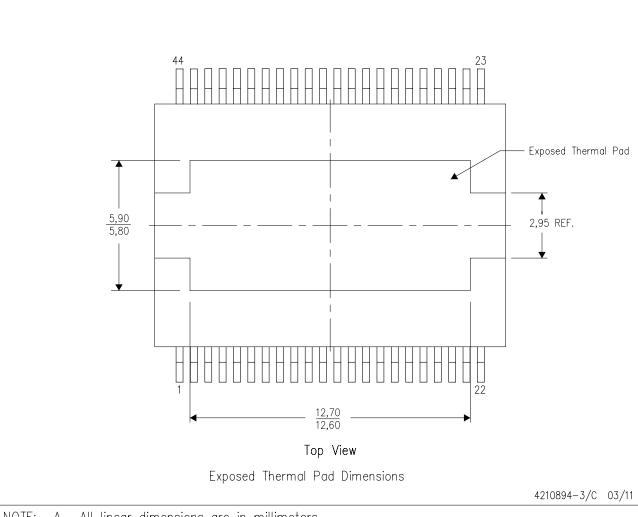
PowerPAD[™] PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

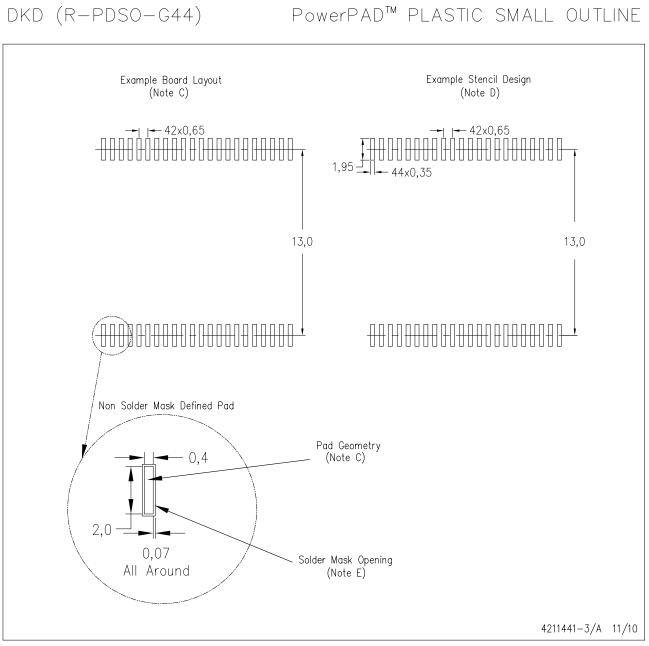
For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: A. All linear dimensions are in millimeters





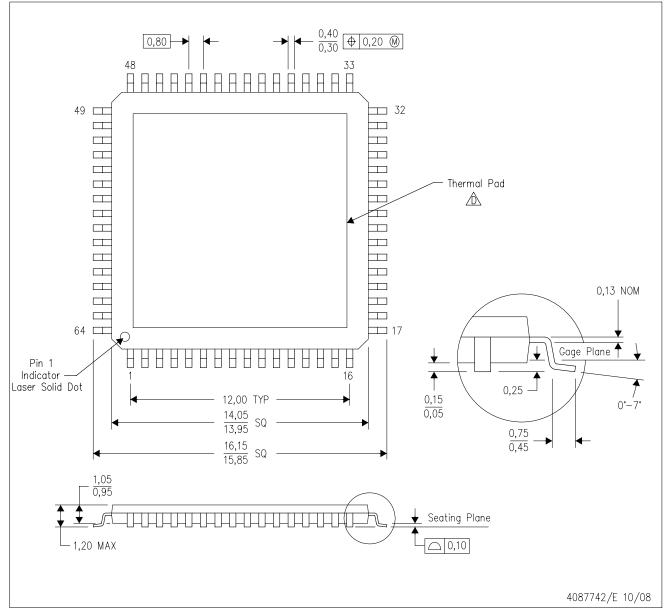
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.



PHD (S-PQFP-G64) PowerPAD[™] PLASTIC QUAD FLATPACK (DIE DOWN)



A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com http://www.ti.com. See the product data sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

NOTES:



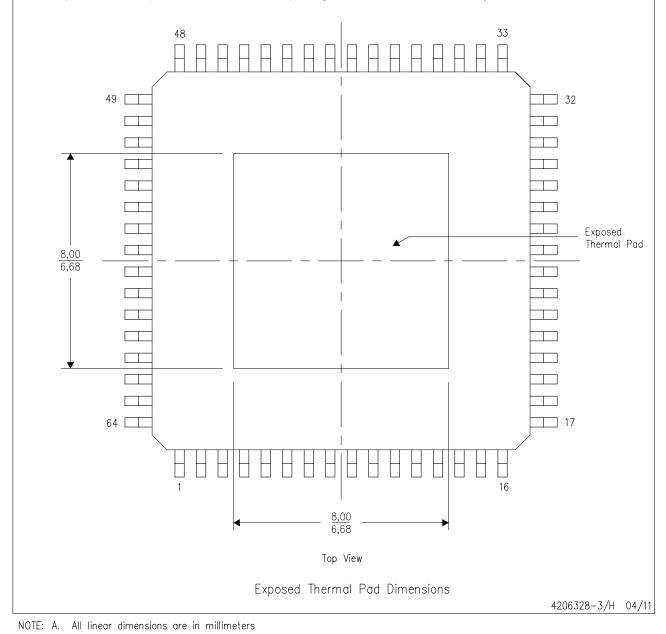
PHD (S-PQFP-G64) PowerPAD[™] PLASTIC QUAD FLATPACK (DIE DOWN)

THERMAL INFORMATION

This PowerPAD[™] package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



PowerPAD is a trademark of Texas Instruments



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