SDAS083C - APRIL 1982 - REVISED MARCH 2002

- Eight Latches in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- pnp Inputs Reduce dc Loading on Data Lines

### description

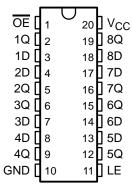
These octal transparent D-type latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

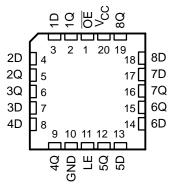
A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

OE does not affect internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

SN54ALS373A, . . . J OR W PACKAGE SN54AS373 . . . J PACKAGE SN74ALS373A, SN74AS373 . . . DW, N, OR NS PACKAGE (TOP VIEW)



SN54ALS373A, SN54AS373 . . . FK PACKAGE (TOP VIEW)





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



#### **ORDERING INFORMATION**

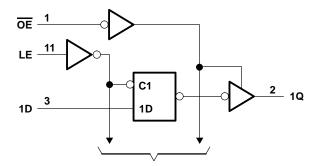
TA	PACI	KAGE <sup>†</sup>	ORDERABLE PART NUMBER	TOP-SIDE Marking
	PDIP – N	Tube	SN74ALS373AN	SN74ALS373AN
	PDIF - IN	Tube	SN74AS373N	SN74AS373N
		Tube	SN74ALS373ADW	ALS373A
0°C to 70°C	SOIC - DW	Tape and reel	SN74ALS373ADWR	AL3373A
0 0 10 70 0	SOIC - DW	Tube	SN74AS373DW	AS373
		Tape and reel	SN74AS373DWR	A5373
	SOP – NS	COD NO Town and work	SN74ALS373ANSR	ALS373A
	30F = N3	Tape and reel	SN74AS373NSR	74AS373
	CDIP – J	Tube	SNJ54ALS373AJ	SNJ54ALS373AJ
	CDIP = J	Tube	SNJ54AS373J	SNJ54AS373J
–55°C to 125°C	–55°C to 125°C CFP − W Tul		SNJ54ALS373AW	SNJ54ALS373AW
	LCCC – FK	Tube	SNJ54ALS373AFK	SNJ54ALS373AFK
	LCCC - FK	Tube	SNJ54AS373FK	SNJ54AS373FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE** (each latch)

	INPUTS		OUTPUT
OE	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	$Q_0$
Н	Χ	Χ	Z

## logic diagram (positive logic)



**To Seven Other Channels** 

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# absolute maximum ratings over operating free-air temperature range (SN54ALS373A, SN74ALS373A) (unless otherwise noted)<sup>†</sup>

Supply voltage, V <sub>CC</sub>		7 V
Input voltage, V <sub>I</sub>		7 V
Voltage applied to any output in the high state o	or power-off state	5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 1):	DW package	58°C/W
	N package	69°C/W
	NS package	60°C/W
Storage temperature range, T <sub>stg</sub>		-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

		SN	4ALS37	'3A	SN74ALS373A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vсс	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			8.0	V
loн	High-level output current			-1			-2.6	mA
loL	Low-level output current			12			24	mA
TA	Operating free-air temperature	-55		125	0		70	°C

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN54ALS373A MIN MAX		SN74AL	UNIT	
				MIN	MAX	UNIT
fclock	Clock frequency					MHz
t <sub>W</sub>	Pulse duration, LE high	12		10		ns
t <sub>su</sub>	Setup time, data before LE↓	10		10		ns
t <sub>h</sub>	Hold time, data after LE $\downarrow$	7		7		ns



NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST 00	NUDITIONS	SNS	4ALS37	3A	SN7	4ALS37	3A	UNIT
PARAMETER	lESI CC	ONDITIONS	MIN	TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX	UNII
VIK	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA			-1.5			-1.5	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V <sub>CC</sub> -2			V <sub>CC</sub> -2			
	V <sub>CC</sub> = 4.5 V	$I_{OH} = -1 \text{ mA}$	2.4	3.3					V
	vCC = 4.5 v	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
Voi	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 12 mA		0.25	0.4		0.25	0.4	V
VOL		$I_{OL} = 24 \text{ mA}$					0.35	0.5	V
lozh	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V			20			20	μΑ
lozL	$V_{CC} = 5.5 \text{ V},$	$V_0 = 0.4 \text{ V}$			-20			-20	μΑ
l <sub>l</sub>	$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = 7 V			0.1			0.1	mA
lН	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			20			20	μΑ
Ι <sub>ΙL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V			-0.1			-0.1	mA
IO <sup>‡</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	-20		-112	-30		-112	mA
	V <sub>CC</sub> = 5.5 V	Outputs high		9	16		9	16	mA
<sup>I</sup> cc		Outputs low		16	25		16	25	
		Outputs disabled		17	27		17	27	

 $<sup>\</sup>overline{\dagger}$  All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C <sub>l</sub> R1 R2	_ = 50 pf l = 500 Ω 2 = 500 Ω	2,	,	UNIT
			SN54AL	S373A	SN74AL	S373A	
			MIN	MAX	MIN	MAX	
<sup>t</sup> PLH	D	0	2	17	2	12	ns
<sup>t</sup> PHL	U	Q	1	19	4	16	113
t <sub>PLH</sub>	LE	A O	6	29	6	22	ns
<sup>t</sup> PHL	LL	Any Q	1	27	7	23	115
<sup>t</sup> PZH	ŌĒ	A Q	6	22	1	18	no
t <sub>PZL</sub>	UE	Any Q	5	24	5	20	ns
<sup>t</sup> PHZ	ŌĒ	Any Q	2	16	1	10	nc
t <sub>PLZ</sub>	OE .	Ally Q	2	24	2	12	ns

<sup>§</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



<sup>&</sup>lt;sup>‡</sup> The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I<sub>OS</sub>.

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# absolute maximum ratings over operating free-air temperature range (SN54AS373, SN74AS373) (unless otherwise noted)

Supply voltage, V <sub>CC</sub>	
Input voltage, V <sub>I</sub>	
Voltage applied to any output in the high state or power	er-off state 5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 1): DW p	ackage 58°C/W
N pag	kage 69°C/W
NS pa	ackage 60°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

		SI	N54AS37	3	SN74AS373			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vсс	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
ІОН	High-level output current			-12			-15	mA
loL	Low-level output current			32			48	mA
TA	Operating free-air temperature	-55		125	0		70	°C

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN54AS373 MIN MAX		SN74A	UNIT	
				MIN	MAX	UNII
fclock	Clock frequency					MHz
t <sub>W</sub>	Pulse duration, LE high	5.5*		4.5*		ns
t <sub>su</sub>	Setup time, data before LE↓	2*		2*		ns
t <sub>h</sub>	Hold time, data after LE↓	3*		3*		ns

<sup>\*</sup> On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



NOTE 2: The package thermal impedance is calculated in accordance with JESD 51-7.

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#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEST OF	CAUDITIONS	SN	154AS37	3	SN	UNIT		
PARAMETER	IESI C	ONDITIONS	MIN	TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX	UNII
VIK	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I <sub>OH</sub> = -2 mA	V <sub>CC</sub> -2			V <sub>CC</sub> -2			
Voн	V <sub>CC</sub> = 4.5 V	$I_{OH} = -12 \text{ mA}$	2.4	3.2					V
	vCC = 4.5 v	$I_{OH} = -15 \text{ mA}$				2.4	3.3		
Voi	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 32 mA		0.27	0.5				V
VOL		I <sub>OL</sub> = 48 mA					0.32	0.5	V
lozh	$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.7 \text{ V}$			50			50	μΑ
lozL	$V_{CC} = 5.5 V,$	$V_0 = 0.4 \text{ V}$			-50			-50	μΑ
l <sub>l</sub>	$V_{CC} = 5.5 V$ ,	V <sub>I</sub> = 7 V			0.1			0.1	mA
lін	$V_{CC} = 5.5 V$ ,	V <sub>I</sub> = 2.7 V			20			20	μΑ
Ι <sub>Ι</sub> L	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V		-0.02	-0.5		-0.02	-0.5	mA
10 <sup>‡</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	-30		-112	-30		-112	mA
	V <sub>CC</sub> = 5.5 V	Outputs high		55	90		55	90	mA
lcc		Outputs low		55	85		55	85	
		Outputs disabled		65	100		65	100	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

## switching characteristics (see Figure 1)

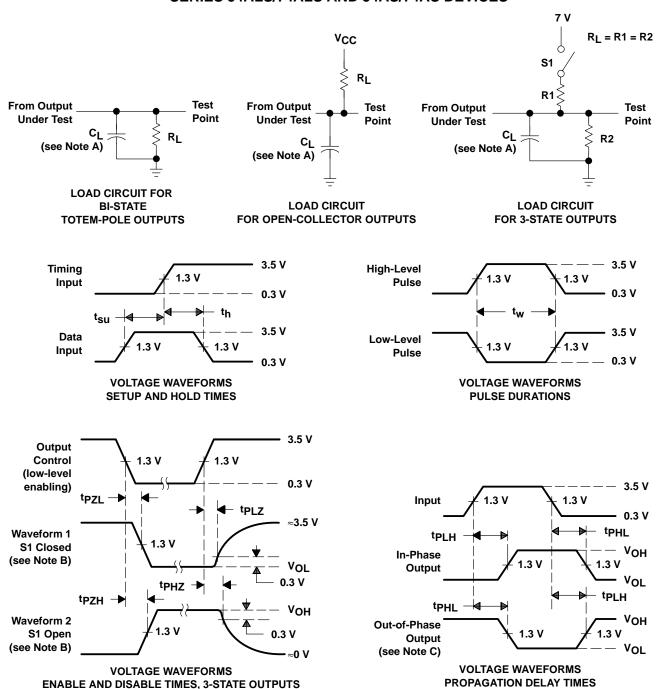
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C <sub>l</sub> R' R:	CC = 4.5 L = 50 pF I = 500 Ω 2 = 500 Ω λ = MIN t	2, 2,	',	UNIT
			SN54A	S373	SN74A	S373	
			MIN	MAX	MIN	MAX	
<sup>t</sup> PLH	D	Q	3	9	3.5	6	ns
<sup>t</sup> PHL	U		3	8	3.5	6	
<sup>t</sup> PLH	LE	A O	6.5	14.5	6.5	11.5	ns
<sup>t</sup> PHL	LL	Any Q	5	9	5	7.5	115
<sup>t</sup> PZH	ŌĒ	A O	2	7.5	2	6.5	no
<sup>t</sup> PZL	OE .	Any Q	4.5	10.5	4.5	9.5	ns
<sup>t</sup> PHZ	ŌĒ	Any Q	3	10	3	6.5	no
t <sub>PLZ</sub>	OE .	Ally Q	3	8	3	7	ns

<sup>§</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



<sup>‡</sup> The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, IOS.

#### PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics:  $PRR \le 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



25-Jan-2012

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
83020012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
8302001RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
8302001SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
JM38510/37203B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/37203BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
M38510/37203B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/37203BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SN54ALS373AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SN54AS373J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SN74ALS373ADBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	
SN74ALS373ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS373ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS373ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS373ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS373ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS373ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS373ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS373ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS373AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS373AN3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	
SN74ALS373ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS373ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	





25-Jan-2012

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74ALS373ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS373ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS373DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS373DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS373DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS373DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS373DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS373DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS373N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AS373N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	
SN74AS373NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AS373NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS373NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS373NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54ALS373AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54ALS373AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SNJ54ALS373AW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	
SNJ54AS373FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54AS373J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.



## PACKAGE OPTION ADDENDUM



ww.ti.com 25-Jan-2012

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373:

• Catalog: SN74ALS373A, SN74AS373

Military: SN54ALS373A, SN54AS373

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications



#### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS373ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ALS373ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74ALS373ANSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74AS373DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74AS373NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1





\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS373ADBR	SSOP	DB	20	2000	346.0	346.0	33.0
SN74ALS373ADWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74ALS373ANSR	SO	NS	20	2000	346.0	346.0	41.0
SN74AS373DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74AS373NSR	SO	NS	20	2000	346.0	346.0	41.0

## 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## W (R-GDFP-F20)

## CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

## PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

## 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

#### **28 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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