SN54ALS251 ... J PACKAGE

SDAS215A - APRIL 1982 - REVISED DECEMBER 1994

- 3-State Version of the 'ALS151
- 3-State Outputs Interface Directly With System Bus
- Perform Parallel-to-Serial Conversion
- Complementary Outputs Provide True and Inverted Data
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

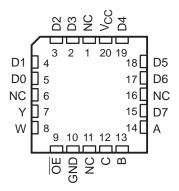
These data selectors/multiplexers contain full binary decoding to select one-of-eight data sources and feature controlled complementary 3-state outputs.

The 3-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at the high-impedance state), the low impedance of the signal-enabled output drives the bus line to a high or low logic level. Both outputs are controlled by the output-enable (\overline{OE}) input. The outputs are disabled when \overline{OE} is high.

The SN54ALS251 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74ALS251 is characterized for operation from 0°C to 70°C.

SN74ALS251 D OR N PACKAGE (TOP VIEW)					
D3 [D2 [D1 [D0 [Y [OE [GND [16 15 14 13 12 11 10 9	V _{CC} D4 D5 D6 D7 A B C		

SN54ALS251 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

	INP									
	SELECT	-	OE	OUTPUTS						
С	В	Α	OE	Y	W					
Х	Х	Х	Н	Z	Ζ					
L	L	L	L	D0	D0					
L	L	н	L	D1	D1					
L	Н	L	L	D2	D2					
L	Н	н	L	D3	D3					
н	L	L	L	D4	D4					
н	L	н	L	D5	D5					
н	Н	L	L	D6	D6					
н	Н	Н	L	D7	D7					

FUNCTION TABLE

D0, D1, ... D7 = the level of the respective D input

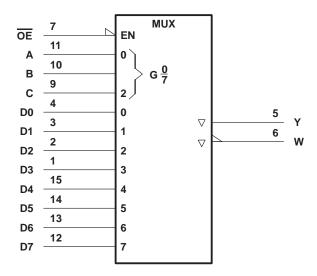
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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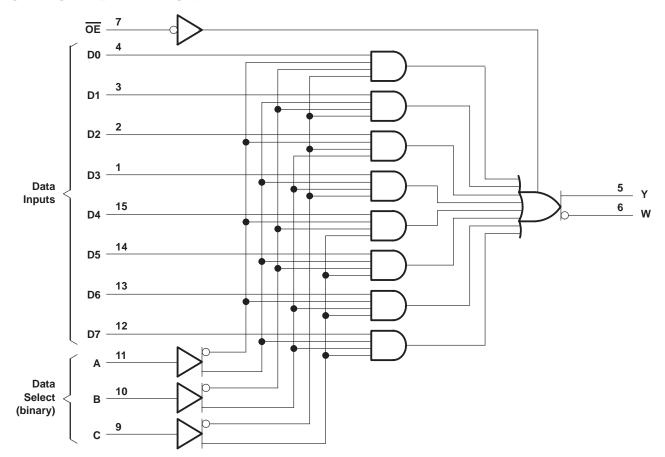
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logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{CC}	
Voltage applied to a disabled 3-state output	
Operating free-air temperature range, T _A : SN54ALS251	
SN74ALS251	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN	SN54ALS251			SN74ALS251			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
ЮН	High-level output current			-1			-2.6	mA	
IOL	Low-level output current			12			24	mA	
Т _А	Operating free-air temperature	-55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		7507.0	TEST CONDITIONS			51	SN	74ALS2	51	
		TEST CONDITIONS			TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lj = – 18 mA			-1.5			-1.5	V
		$V_{CC} = 4.5 V \text{ to } 5.5 V,$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2	2		V _{CC} -2	2		
∨он			$I_{OH} = -1 \text{ mA}$	2.4	3.3					V
		$V_{CC} = 4.5 V$	I _{OH} = -2.6 mA				2.4	3.2		
V _{OL}			I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		$V_{CC} = 4.5 V$	I _{OL} = 24 mA					0.35	0.5	V
IOZH		V _{CC} = 5.5 V,	V _O = 2.7 V			20			20	μΑ
IOZL		V _{CC} = 5.5 V,	$V_{O} = 0.4 V$			-20			-20	μΑ
lj		V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
Ι _{ΙΗ}		V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
IIL		V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	mA
۱ ₀ §		V _{CC} = 5.5 V,	V _O = 4.5 V	-20		-112	-30		-112	mA
ICC	Enabled		Inputs at GND		7	10		7	10	
	Disabled $V_{CC} = 5.5 V$		Inputs at 4.5 V		9.4	14		9.4	14	mA

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



SN54ALS251, SN74ALS251 1-OF-8 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS SDAS215A – APRIL 1982 – REVISED DECEMBER 1994

switching characteristics (see Figure 1)

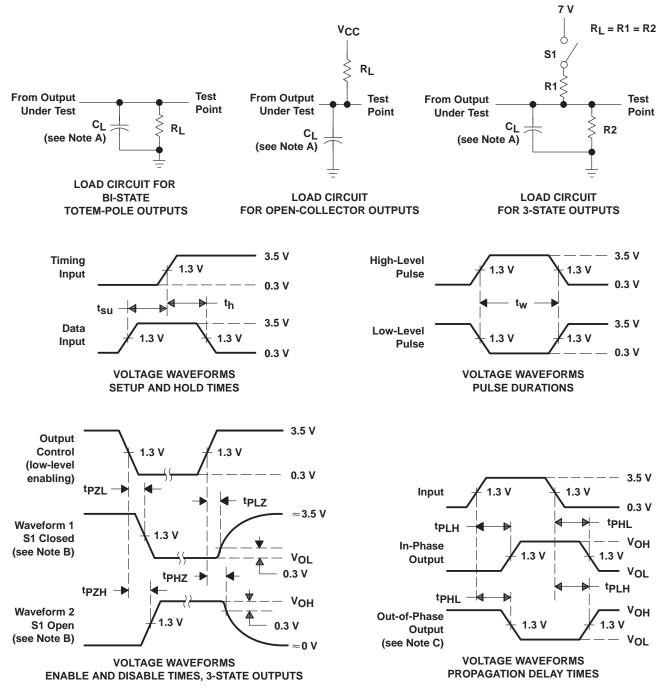
PARAMETER	FROM (INPUT)	TO (OUTPUT)	VC CL R1 R2 TA	UNIT			
			SN54A	LS251	SN74A	LS251	
			MIN	MAX	MIN	MAX	
tPLH		Y	1	21	5	18	20
^t PHL	A, B, or C	ř	7	34	8	24	ns
^t PLH	A, B, or C	W	5	38	8	24	
^t PHL		VV	7	26	7	23	ns
^t PLH	Anu D	Y W	2	15	2	10	
^t PHL	Any D		3	23	3	15	ns
^t PLH	Anu D		3	25	3	15	200
^t PHL	Any D		3	20	3	15	ns
^t PZH	OE	Y	3	21	3	15	
^t PZL	OE	ř	3	19	3	15	ns
^t PZH	OE	10/	3	21	3	15	20
tPZL	UE	W	3	19	3	15	ns
^t PZH	OE	V	2	12	2	10	
tPZL	UE	Y	1	18	1	10	ns
^t PZH	ŌĒ	W	2	12	2	10	ns
tPZL	UE	vv	1	18	1	10	115

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR \leq 1 MHz, t_{f} = t_{f} = 2 ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms





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5-Sep-2011

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
84135012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
8413501EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
8413501FA	ACTIVE	CFP	W	16	1	TBD	Call TI	Call TI	
SN54ALS251J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN74ALS251D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS251DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS251DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS251DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS251DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS251DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS251N	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS251NE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS251NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS251NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS251NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54ALS251FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54ALS251J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54ALS251W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.



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⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54ALS251, SN74ALS251 :

• Catalog: SN74ALS251

• Military: SN54ALS251

NOTE: Qualified Version Definitions:

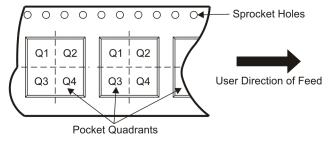
- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS251DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74ALS251NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1



PACKAGE MATERIALS INFORMATION

19-Mar-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS251DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74ALS251NSR	SO	NS	16	2000	346.0	346.0	33.0

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N**) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



4211283-4/D 06/11

D (R-PDSO-G16) PLASTIC SMALL OUTLINE Stencil Openings (Note D) Example Board Layout (Note C) -16x0,55 - 14x1,27 -14x1,27 16x1,95 4,80 4,80 Example Non Soldermask Defined Pad Example Pad Geometry (See Note C) 0,60 Example 2,00 Solder Mask Opening

(See Note E)

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

← 0,07 All Around

- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0-10 Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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