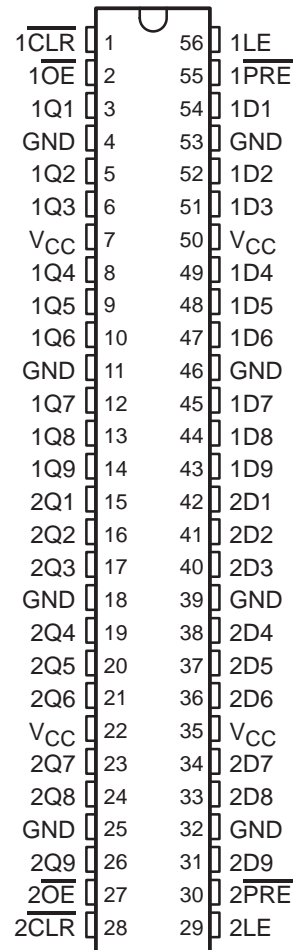


SN54ABT16843, SN74ABT16843 18-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Impedance State During Power Up and Power Down
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), 300-mil Shrink Small-Outline (DL) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABT16843 . . . WD PACKAGE
SN74ABT16843 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'ABT16843 18-bit bus-interface D-type latches are designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'ABT16843 can be used as two 9-bit latches or one 18-bit latch. The 18 latches are transparent D-type latches. The device provides true data at its outputs.

A buffered output-enable (\overline{OE}) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. The outputs are in the high-impedance state during power up and power down. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.



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18-BIT BUS-INTERFACE D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCBS223E – OCTOBER 1992 – REVISED MAY 1997

description (continued)

\overline{OE} does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16843 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT16843 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
 (each 9-bit latch)

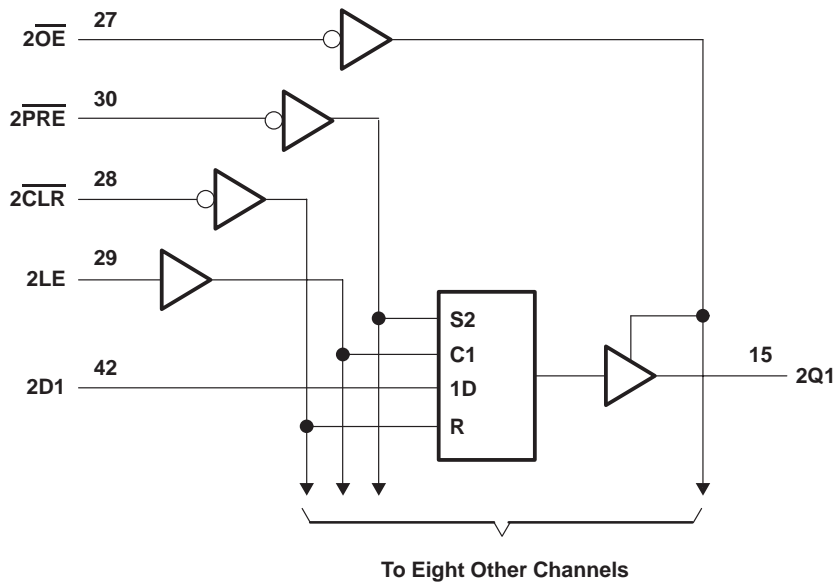
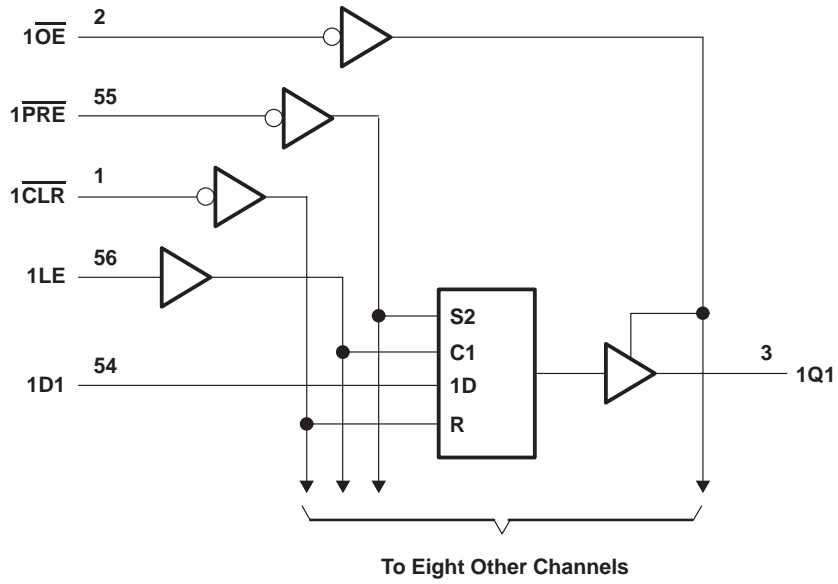
INPUTS					OUTPUT Q
\overline{PRE}	\overline{CLR}	\overline{OE}	LE	D	
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_0
X	X	H	X	X	Z



SN54ABT16843, SN74ABT16843
 18-BIT BUS-INTERFACE D-TYPE LATCHES
 WITH 3-STATE OUTPUTS

SCBS223E – OCTOBER 1992 – REVISED MAY 1997

logic diagram (positive logic)



SN54ABT16843, SN74ABT16843

18-BIT BUS-INTERFACE D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SCBS223E – OCTOBER 1992 – REVISED MAY 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16843	96 mA
SN74ABT16843	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

	SN54ABT16843		SN74ABT16843		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH} High-level output current		-24		-32	mA
I_{OL} Low-level output current		48		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$ Power-up ramp rate	200		200		μ s/V
T_A Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

SN54ABT16843, SN74ABT16843 18-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS223E – OCTOBER 1992 – REVISED MAY 1997

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT16843		SN74ABT16843		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA		2.5		2.5		2.5		V
	V _{CC} = 5 V, I _{OH} = -3 mA		3		3		3		
	V _{CC} = 4.5 V	I _{OH} = -24 mA		2		2			
I _{OH} = -32 mA			2*				2		
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 48 mA		0.55		0.55			V
		I _{OL} = 64 mA		0.55*			0.55		
V _{hys}			100					mV	
I _I	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA
I _{OZPU} ‡	V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	μA
I _{OZPD} ‡	V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	μA
I _{OZH}	V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, $\overline{OE} \geq 2$ V			10		10		10	μA
I _{OZL}	V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, $\overline{OE} \geq 2$ V			-10		-10		-10	μA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA
I _{CEX}	Outputs high V _{CC} = 5.5 V, V _O = 5.5 V			50		50		50	μA
I _O §	V _{CC} = 5.5 V, V _O = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA
I _{CC}	Outputs high			0.5		0.5		0.5	mA
	Outputs low	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND		85		85		85	
	Outputs disabled			0.5		0.5		0.5	
ΔI _{CC} ¶	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5		1.5		1.5	mA
C _i	V _I = 2.5 V or 0.5 V			3.5					pF
C _o	V _O = 2.5 V or 0.5 V			8					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ This parameter is characterized, but not production tested.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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18-BIT BUS-INTERFACE D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCBS223E – OCTOBER 1992 – REVISED MAY 1997

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V _{CC} = 5 V, T _A = 25°C		SN54ABT16843		SN74ABT16843		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CLR low	3.3	3.3	3.3	3.3	3.3	ns
		PRE low	3.3	3.3	3.3	3.3		
		LE high	3.3	3.3	3.3	3.3		
t _{su}	Setup time, data before LE↓	High	0.9	0.9	0.9	0.9	ns	
		Low	0.6	0.6	0.6	0.6		
t _h	Hold time, data after LE↓	High	1.7	1.7	1.7	1.7	ns	
		Low	1.8	1.8	1.8	1.8		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

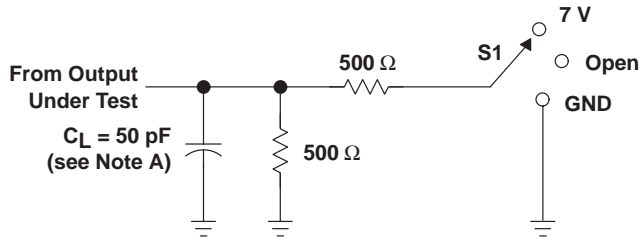
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			SN54ABT16843		SN74ABT16843		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	Q	1.6	3.1	4.2	1.6	5.1	1.6	4.8	ns
t _{PHL}			1.6	3.2	4.2	1.6	5	1.6	4.8	
t _{PLH}	LE	Q	2.3	4	5	2.3	6.3	2.3	5.9	ns
t _{PHL}			2.5	3.9	4.8	2.5	5.6	2.5	5.3	
t _{PLH}	PRE	Q	2.1	4	5.1	2.1	6.3	2.1	6.1	ns
t _{PHL}			2.2	3.7	4.6	2.2	5.3	2.2	5	
t _{PLH}	CLR	Q	1.9	3.7	4.8	1.9	5.7	1.9	5.4	ns
t _{PHL}			2.2	4.2	5.3	2.2	6.1	2.2	6	
t _{PZH}	OE	Q	1.6	3.3	4.3	1.6	5.5	1.6	5.4	ns
t _{PZL}			2	3.2	4.6	2	5.9	2	5.8	
t _{PHZ}	OE	Q	1.7	4	5.5	1.7	6.4	1.7	6.3	ns
t _{PLZ}			1.7	3.7	4.4	1.7	5.3	1.7	5.2	

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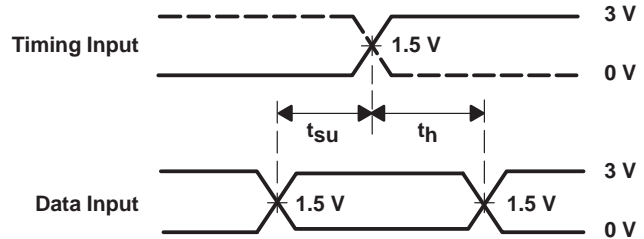


LOAD CIRCUIT

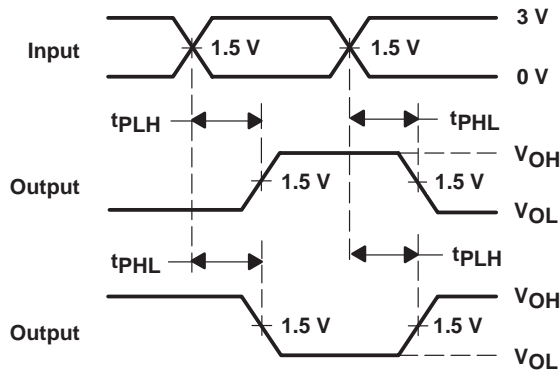
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



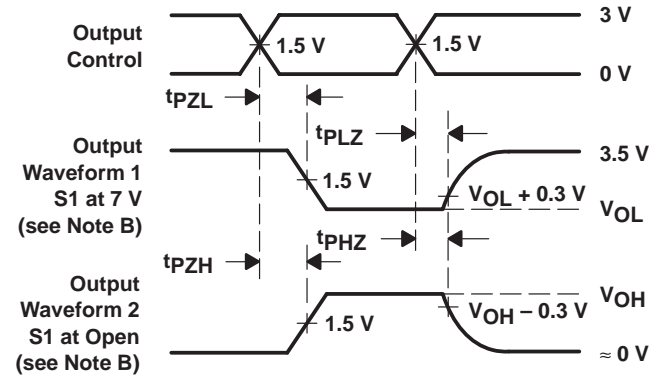
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16843DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16843DLR	SSOP	DL	56	1000	346.0	346.0	49.0

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