CBT3257A

Quad 1-of-2 multiplexer/demultiplexer Rev. 04 — 19 March 2009

Product data sheet

General description 1.

The CBT3257A is a quad 1-of-2 high-speed TTL-compatible multiplexer/demultiplexer. The low ON resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

Output enable (\overline{OE}) and select-control (S) inputs select the appropriate nB1 and nB2 outputs for the nA input data.

The CBT3257A is characterized for operation from -40 °C to +85 °C.

2. **Features**

- \blacksquare 5 Ω switch connection between two ports
- TTL-compatible input levels
- Minimal propagation delay through the switch
- Latch-up protection exceeds 500 mA per JEDEC standard JESD78 class II level A
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from –40 °C to +85 °C

Ordering information 3.

Table 1. **Ordering information**

Type number	Temperature range	Package		
		Name	Description	Version
CBT3257AD	–40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
CBT3257ADB	–40 °C to +85 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1

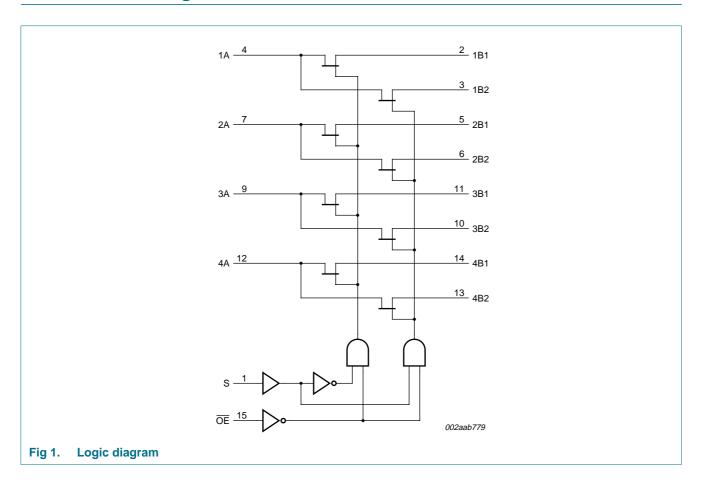


 Table 1.
 Ordering information ...continued

Type number	Temperature range	Package					
		Name	Description	Version			
CBT3257ADS	–40 °C to +85 °C	SSOP16[1]	plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT519-1			
CBT3257APW	–40 °C to +85 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1			
CBT3257ABQ	–40 °C to +85 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body $2.5\times3.5\times0.85$ mm	SOT763-1			

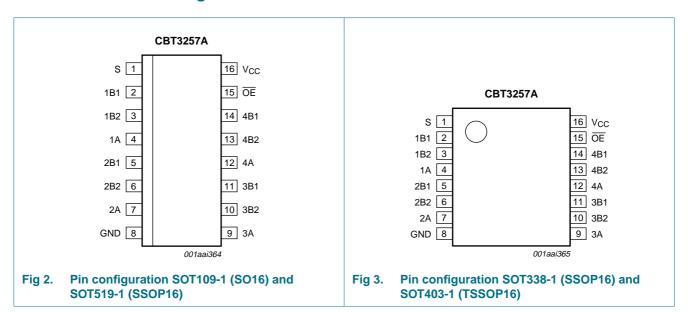
^[1] Also known as QSOP16.

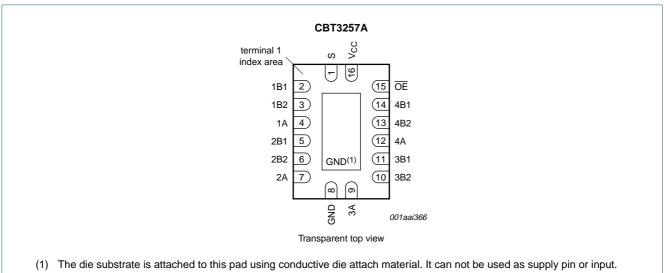
4. Functional diagram



Pinning information

5.1 **Pinning**





Pin configuration SOT763-1 (DHVQFN16) Fig 4.

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	select control input
1B1, 2B1, 3B1, 4B1,	2, 5, 11, 14	B1 outputs/inputs
1B2, 2B2, 3B2, 4B2	3, 6, 10, 13	B2 outputs/inputs
1A, 2A, 3A, 4A	4, 7, 9, 12	A inputs/outputs
GND	8	ground (0 V)
ŌĒ	15	output enable (active LOW)
V _{CC}	16	positive supply voltage

6. Functional description

Table 3. Function selection

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level; \ X = Don't \ care.$

Inputs		Switch
OE	s	
L	L	nA to nB1
L	Н	nA to nB2
Н	X	switch off

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

V _I in	upply voltage nput voltage		-0.5	+7.0	V
	nput voltage		[4] 0 =		
			<u>[1]</u> –0.5	+7.0	V
I _{SW} sv	witch current	continuous current through each switch	-	128	mA
I _{IK} in	nput clamping current	V _I < 0 V	-50	_	mA
T _{stg} st	torage temperature		-65	+150	°C
P _{tot} to	otal power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$			
		SO16 package	<u>[2]</u> _	500	mW
		SSOP16 package	<u>[3]</u> _	500	mW
		TSSOP16 package	<u>[3]</u> _	500	mW
		DHVQFN16 package	<u>[4]</u> _	500	mW

^[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

^[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 $^{\circ}\text{C}.$

^[3] For SSOP16 and TSSOP16 package: Ptot derates linearly with 5.5 mW/K above 70 °C.

^[4] For DHVQFN16 package: Ptot derates linearly with 4.5 mW/K above 70 °C.

8. Recommended operating conditions

Table 5. Operating conditions

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		4.5	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	V
V_{IL}	LOW-level input voltage		-	8.0	V
T _{amb}	ambient temperature	operating in free-air	-40	+85	°C

9. Static characteristics

Table 6. Static characteristics

 $T_{amb} = -40 \,^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	$V_{CC} = 4.5 \text{ V}; I_I = -18 \text{ mA}$	-	-	-1.2	V
V_{pass}	pass voltage	$V_I = V_{CC} = 5.0 \text{ V}; I_O = -100 \mu\text{A}$	3.4	3.6	3.9	V
I _I	input leakage current	$V_{CC} = 5.5 \text{ V}; V_{I} = \text{GND or } 5.5 \text{ V}$	-	-	±1	μΑ
I _{CC}	supply current	V_{CC} = 5.5 V; I_O = 0 mA; V_I = V_{CC} or GND	-	-	3	μΑ
ΔI_{CC}	additional supply current	per input; V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND	[2] -	-	2.5	mA
Cı	input capacitance	control pins; $V_I = 3 \text{ V or } 0 \text{ V}$	-	3.3	-	pF
$C_{io(off)}$	off-state input/output capacitance	A port; $V_O = 3 \text{ V or } 0 \text{ V}$; $\overline{OE} = V_{CC}$	-	9.9	-	pF
		B port; $V_O = 3 \text{ V or } 0 \text{ V}$; $\overline{OE} = V_{CC}$	-	6.4	-	pF
R _{ON}	ON resistance	V _{CC} = 4.5 V	[3]			
		$V_1 = 0 \ V; \ I_1 = 64 \ mA$	-	5	7	Ω
		$V_{I} = 0 V; I_{I} = 30 mA$	-	5	7	Ω
		$V_I = 2.4 \text{ V}; I_I = 15 \text{ mA}$	-	10	15	Ω

^[1] All typical values are measured at V_{CC} = 5 V; T_{amb} = 25 °C.

^[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

^[3] Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (A or B) terminals.

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10. Dynamic characteristics

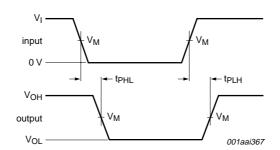
Table 7. Dynamic characteristics

 $T_{amb} = -40 \,^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$; $V_{CC} = 4.5 \,^{\circ}\text{V}$ to 5.5 V; for test circuit see Figure 7.

Symbol	Parameter	Conditions	Min	Max	Unit
t _{pd}	propagation delay	nA to nBn or nBn to nA; see Figure 5	[1][2]	0.25	ns
		S to nA or nBn; see Figure 5	[1][2] 1.6	5.0	ns
t _{en}	enable time	OE to nA or nBn; see Figure 6	<u>[2]</u> 1.8	5.1	ns
		S to nA or nBn; see Figure 6	<u>[2]</u> 1.6	5.2	ns
t _{dis}	disable time	OE to nA or nBn; see Figure 6	2.2	5.5	ns
		S to nA or nBn; see Figure 6	<u>[2]</u> 1.0	5.0	ns

^[1] This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical ON resistance of the switch and a load capacitance, when driven by an ideal voltage source (zero output impedance).

11. AC waveforms



Measurement points are given in Table 8.

 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. The input (nA; nBn) to output (nBn; nA) or input (S) to output (nBn; nA) propagation delay times

^[2] t_{PLH} and t_{PHL} are the same as t_{pd} . t_{PZL} and t_{PZH} are the same as t_{en} . t_{PLZ} and t_{PHZ} are the same as t_{dis} .

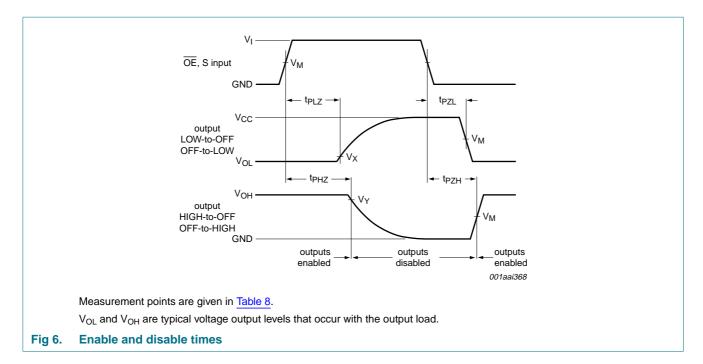
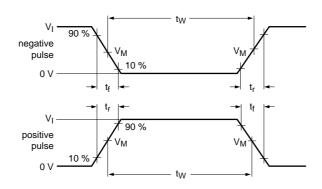
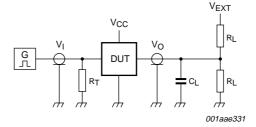


Table 8. Measurement points

Supply voltage	Input		Output				
V _{CC}	V _I	V _M	V _M	V _X	V _Y		
4.5 V to 5.5 V	GND to 3.0 V	1.5 V	1.5 V	V _{OL} + 0.3 V	$V_{OH} - 0.3 V$		

12. Test information





Test data is given in Table 9.

Definitions for test circuit:

 R_1 = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to the output impedance Z_0 of the pulse generator.

 V_{EXT} = External voltage for measuring switching times.

Fig 7. Test circuit for measuring switching times

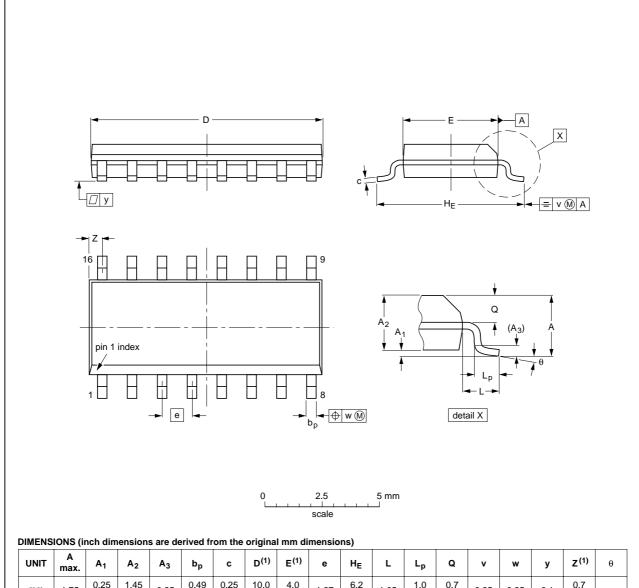
Table 9. Test data

Supply voltage	Input		Load		V _{EXT}			
V _{CC}	VI	t _r , t _f	C _L R _L		t _{PLH} , t _{PHL}	t _{PLZ} , t _{PZL}	t _{PHZ} , t _{PZH}	
4.5 V to 5.5 V	GND to 3.0 V	≤ 2.5 ns	50 pF	500 Ω	open	7.0 V	open	

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



UNIT	A max.	A ₁	A ₂	A ₃	b _p	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016		0.01	0.01	0.004	0.028 0.012	0°

Note

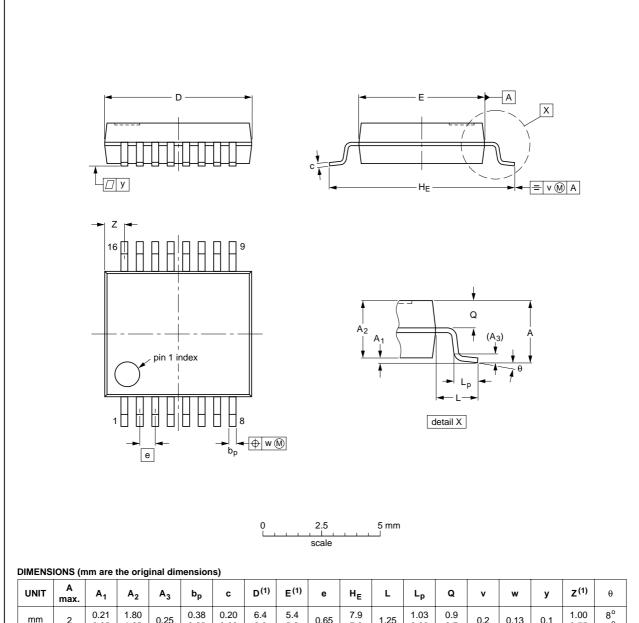
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT109-1	076E07	MS-012			99-12-27 03-02-19

Fig 8. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



_																			
	UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
	mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

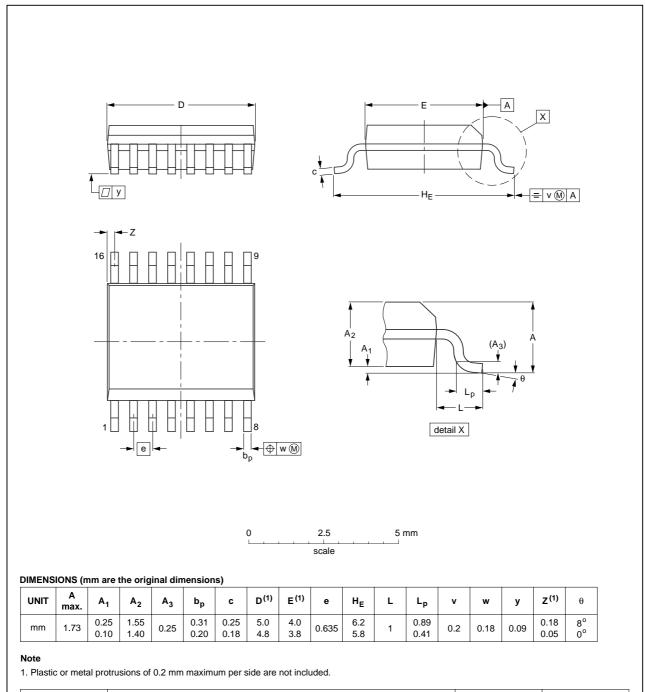
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

		EUROPEAN	ISSUE DATE	
JEDEC	JEITA	PROJECTION	1330E DATE	
MO-150			99-12-27 03-02-19	
			JEDEC JEITA	

Package outline SOT338-1 (SSOP16) Fig 9.

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm SOT519-1

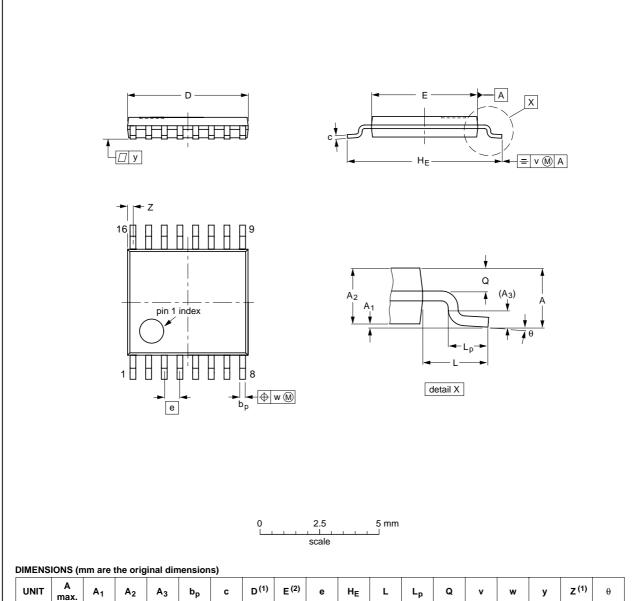


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VER	RSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE	
SOT	Г519-1					-99-05-04- 03-02-18	

Fig 10. Package outline SOT519-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



	•					•												
UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN ISSUE DATE			
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE		
SOT403-1		MO-153			-99-12-27 03-02-18		

Fig 11. Package outline SOT403-1 (TSSOP16)

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DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm SOT763-1

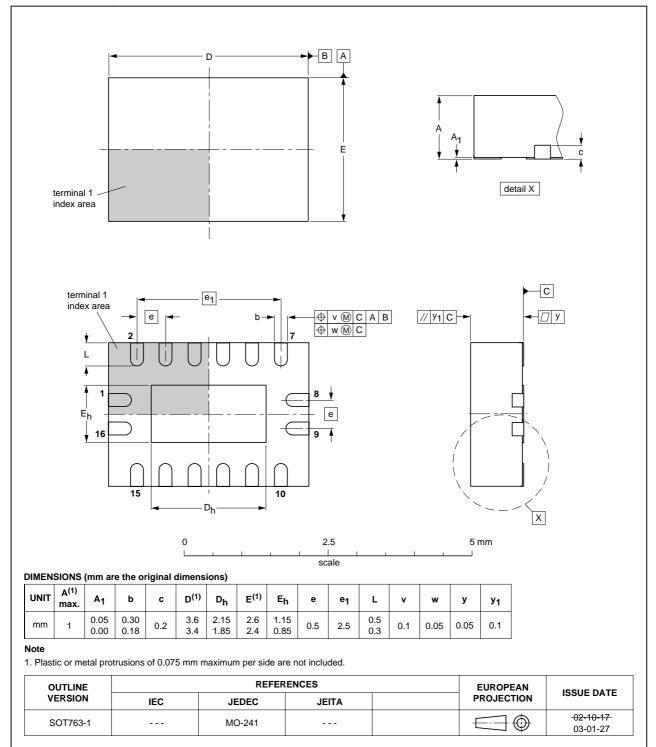


Fig 12. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBT3257A_4	20090319	Product data sheet	-	CBT3257A_3
Modifications:	• Table 4 "Lim	iting values" modified.		
CBT3257A_3	20080704	Product data sheet	-	CBT3257A_2
CBT3257A_2	20070704	Product data sheet	-	CBT3257A_1
CBT3257A_1	20051027	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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NXP Semiconductors CBT3257A

Quad 1-of-2 multiplexer/demultiplexer

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