TAS5631

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SLES221C-JULY 2009-REVISED APRIL 2010

300-W STEREO / 600-W MONO PurePath™ HD DIGITAL-INPUT POWER STAGE

Check for Samples: TAS5631

FEATURES

- PurePath[™] HD Enabled Integrated Feedback Provides:
 - Signal Bandwidth up to 80 kHz for High-Frequency Content From HD Sources
 - Ultralow 0.03% THD at 1 W Into 4 Ω
 - Flat THD at All Frequencies for Natural Sound
 - 80-dB PSRR (BTL, No Input Signal)
 - >100-dB (A-weighted) SNR
 - Click- and Pop-Free Start-Up
- Multiple Configurations Possible on the Same PCB With Stuffing Options:
 - Mono Parallel Bridge-Tied Load (PBTL)
 - Stereo Bridge-Tied Load (BTL)
 - 2.1 Single-Ended Stereo Pair and Bridge-Tied Load Subwoofer
 - Quad Single-Ended Outputs
- Total Output Power at 10% THD+N
 - 600 W in Mono PBTL Configuration
 - 300 W per Channel in Stereo BTL Configuration
 - 145 W per Channel in Quad Single-Ended Configuration
- High-Efficiency Power Stage (>88%) With 60-mΩ Output MOSFETs
- Two Thermally Enhanced Package Options:
 - PHD (64-Pin QFP)
 - DKD (44-Pin PSOP3)
- Self-Protection Design (Including Undervoltage, Overtemperature, Clipping, and Short-Circuit Protection) With Error Reporting
- EMI Compliant When Used With Recommended System Design

APPLICATIONS

- Mini Combo System
- AV Receivers
- DVD Receivers
- Active Speakers

DESCRIPTION

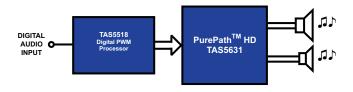
The TAS5631 is a high-performance PWM input class-D amplifier with integrated closed-loop feedback technology (known as PurePath HD technology) with the ability to drive up to 300 W $^{(1)}$ stereo into 4- Ω to 8- Ω speakers from a single 50-V supply.

PurePath HD technology enables traditional AB-amplifier performance (<0.03% THD) levels while providing the power efficiency of traditional class-D amplifiers.

Unlike traditional class-D amplifiers, the distortion curve only increases once the output levels move into clipping.

PurePath HD technology enables lower idle losses, making the device even more efficient.

Note 1. Achievable output power levels are dependent on the thermal configuration of the target application. A high-performance thermal interface material between the package exposed heat slug and the heat sink should be used to achieve high output-power levels.



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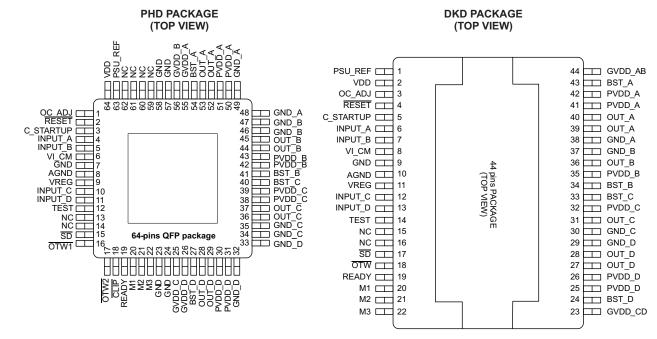


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

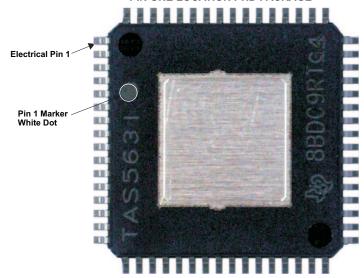
DEVICE INFORMATION

Terminal Assignment

Both package types contains a heat slug that is located on the top side of the device for convenient thermal coupling to the heat sink.



PIN ONE LOCATION PHD PACKAGE



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MODE SELECTION PINS

M	MODE PINS		DIA(M INDUT(1) OUTPUT		DESCRIPTION						
М3	M2	M1	PWWINPUT	WM INPUT ⁽¹⁾ CONFIGURATION		DESCRIPTION					
0	0	0	2N	2 × BTL	AD mode						
0	0	1	_	_	Reserved						
0	1	0	2N	2 × BTL	BD mode						
0	1	1	1N	1 x BTL +2 x SE	AD mode						
1	0	0	1N	4 × SE	AD mode						
					INPUT_C ⁽²⁾	INPUT_D ⁽²⁾					
1	0	1	1	1	1	1	2N 1N	1 × PBTL	0	0	AD mode
					1	0	BD mode				
1	1	0									
1	1	1		Reserved							

- (1) The 1N and 2N naming convention is used to indicate the number of PWM lines to the power stage per channel in a specific mode.
- (2) INPUT_C and INPUT_D are used to select between a subset of AD and BD mode operations in PBTL mode.

PACKAGE HEAT DISSIPATION RATINGS(1)

PARAMETER	TAS5631PHD	TAS5631DKD
R _{0JC} (°C/W) – 2 BTL or 4 SE channels	2.63	14
R _{0JC} (°C/W) – 1 BTL or 2 SE channel(s)	4.13	2.04
R _{0JC} (°C/W) – 1 SE channel	6.45	3.45
Pad area (2)	64 mm ²	80 mm ²

- (1) $R_{\theta JC}$ is junction-to-case; $R_{\theta CH}$ is case-to-heatsink.
- (2) R_{θCH} is an important consideration. Assume a 2-mil (0.051-mm) thickness of thermal grease with a thermal conductivity of 2.5 W/mK between the pad area and the heat sink and both channels active. The R_{θCH} with this condition is 1.1°C/W for the PHD package and 0.44°C/W for the DKD package.

Table 1. ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE	DESCRIPTION
0°C-70°C	TAS5631PHD	64-pin HTQFP
0°C-70°C	TAS5631DKD	44-pin PSOP3

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted (1)

	TAS5631		UNIT
VDD to AGND		-0.3 to 13.2	V
GVDD to AGND		-0.3 to 13.2	V
PVDD_X to GND_X ⁽²⁾		-0.3 to 69	V
OUT_X to GND_X ⁽²⁾		-0.3 to 69	V
BST_X to GND_X ⁽²⁾		-0.3 to 82.2	V
BST_X to GVDD_X ⁽²⁾		-0.3 to 69	V
VREG to AGND		-0.3 to 4.2	V
GND_X to GND		-0.3 to 0.3	V
GND_X to AGND		-0.3 to 0.3	V
GND to AGND	-0.3 to 0.3		V
INPUT_X, OC_ADJ, M1, M2, M3, OS PSU_REF to AGND	SC_IO+, OSC_IO-, FREQ_ADJ, VI_CM, C_STARTUP,	-0.3 to 4.2	V
RESET, SD, OTW1, OTW2, CLIP, R	EADY to AGND	-0.3 to 7	V
Maximum continuous sink current (S	D, OTW1, OTW2, CLIP, READY)	9	mA
Maximum operating junction tempera	ature range, T _J	0 to 150	°C
Storage temperature, T _{stg}		-40 to 150	°C
Clastrostatic discharge	Human-body model ⁽³⁾ (all pins)	±2	kV
Electrostatic discharge	Charged-device model ⁽³⁾ (all pins)	±500	V

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
PVDD_x	Half-bridge supply	DC supply voltage	25	50	52.5	V
GVDD_x	Supply for logic regulators and gate-drive circuitry	DC supply voltage	10.8	12	13.2	V
VDD	Digital regulator supply voltage	DC supply voltage	10.8	12	13.2	V
R _L (BTL)			3.5	4		
R _L (SE)	Load impedance	Output filter according to schematics in the application information section.	1.8	2		Ω
R _L (PBTL)		are approached information section.	1.6	2		
L _{OUTPUT} (BTL)			7	10		
L _{OUTPUT} (SE)	Output filter inductance	Minimum output inductance at I _{OC}	7	15		μН
L _{OUTPUT} (PBTL)			7	10		
f _{PWM}	PWM frame rate		352	384	500	kHz
T_{J}	Junction temperature	·	0		150	°C

TERMINAL FUNCTIONS

TERMINAL			Function ⁽¹⁾	DESCRIPTION
NAME	PHD NO.	DKD NO.	Function	DESCRIPTION
AGND	8	10	Р	Analog ground
BST_A	54	43	Р	HS bootstrap supply (BST); external 0.033-μF capacitor to OUT_A required
BST_B	41	34	Р	HS bootstrap supply (BST); external 0.033-μF capacitor to OUT_B required

(1) I = Input, O = Output, P = Power

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These voltages represents the dc voltage + peak ac waveform measured at the terminal of the device in all conditions.

Failure to follow good anti-static ESD handling during manufacture and rework contributes to device malfunction. Make sure the operators handling the device are adequately grounded through the use of ground straps or alternative ESD protection.

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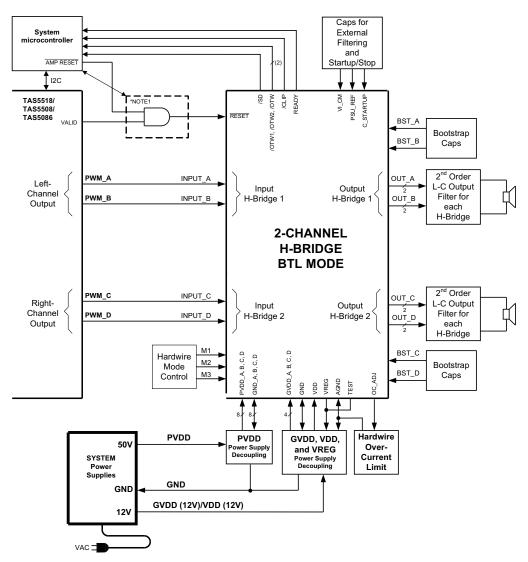
TERMINAL FUNCTIONS (continued)

	TERMINAL		(1)				
NAME	PHD NO.	DKD NO.	Function ⁽¹⁾	DESCRIPTION			
BST_C	40	33	Р	HS bootstrap supply (BST); external 0.033-μF capacitor to OUT_C required			
BST_D	27	24	Р	HS bootstrap supply (BST); external 0.033-μF capacitor to OUT_D required			
CLIP	18	_	0	Clipping warning; open drain; active-low			
C_STARTUP	3	5	0	Start-up ramp requires a charging capacitor of 4.7 nF to AGND.			
TEST	12	14	1	Connect to VREG node			
GND	7, 23, 24, 57, 58	9	Р	Ground			
GND_A	48, 49	38	Р	Power ground for half-bridge A			
GND_B	46, 47	37	Р	Power ground for half-bridge B			
GND_C	34, 35	30	Р	Power ground for half-bridge C			
GND_D	32, 33	29	Р	Power ground for half-bridge D			
GVDD_A	55	_	Р	Gate drive voltage supply requires 0.1-μF capacitor to AGND.			
GVDD_B	56	_	Р	Gate drive voltage supply requires 0.1-μF capacitor to AGND.			
GVDD_C	25	_	Р	Gate drive voltage supply requires 0.1-μF capacitor to AGND.			
GVDD_D	26	_	Р	Gate drive voltage supply requires 0.1-μF capacitor to AGND.			
GVDD_AB	_	44	Р	Gate drive voltage supply requires 0.22-μF capacitor to AGND.			
GVDD_CD	_	23	Р	Gate drive voltage supply requires 0.22-μF capacitor to AGND.			
INPUT_A	4	6	I	Input signal for half-bridge A			
INPUT_B	5	7	1	Input signal for half-bridge B			
INPUT_C	10	12	I	Input signal for half-bridge C			
INPUT_D	11	13	1	Input signal for half-bridge D			
M1	20	20	1	Mode selection			
M2	21	21	1	Mode selection			
M3	22	22	I	Mode selection			
NC	59–62	_	_	No connect; pins may be grounded.			
NC	13, 14	15, 16	_	No connect; pins may be grounded.			
OC_ADJ	1	3	0	Analog overcurrent programming pin requires resistor to ground.			
OTW	_	18	0	Overtemperature warning signal, open-drain, active-low			
OTW1	16	_	0	Overtemperature warning signal, open-drain, active-low			
OTW2	17	_	0	Overtemperature warning signal, open-drain, active-low			
OUT_A	52, 53	39, 40	0	Output, half-bridge A			
OUT_B	44, 45	36	0	Output, half-bridge B			
OUT_C	36, 37	31	0	Output, half-bridge C			
OUT_D	28, 29	27, 28	0	Output, half-bridge D			
PSU_REF	63	1	Р	PSU reference requires close decoupling of 4.7 μF to AGND.			
PVDD_A	50, 51	41, 42	Р	Power-supply input for half-bridge A requires close decoupling of 0.01-μF capacitor in parallel with 1-μF capacitor to GND_A.			
PVDD_B	42, 43	35	Р	Power-supply input for half-bridge B requires close decoupling of 0.01-μF capacitor in parallel with 1-μF capacitor to GND_B.			
PVDD_C	38, 39	32	Р	Power-supply input for half-bridge C requires close decoupling of 0.01 - μ F capacitor in parallel with 1 - μ F capacitor to GND_C.			
PVDD_D	30, 31	25, 26	Р	Power-supply input for half-bridge D requires close decoupling of 0.01-μF capacitor in parallel with 1-μF capacitor to GND_D.			
READY	19	19	0	Normal operation; open-drain; active-high			
RESET	2	4	1	Device reset input; active-low			
SD	15	17	0	Shutdown signal; open-drain, active-low			
VDD	64	2	Р	Power supply for digital voltage regulator requires a 47- μ F capacitor in parallel with a 0.1- μ F capacitor to GND for decoupling.			
VI_CM	6	8	0	Analog comparator reference node requires close decoupling of 4.7 µF to AGND.			
VREG	9	11	Р	Digital regulator supply filter pin requires 0.1-μF capacitor to AGND.			

Product Folder Link(s): TAS5631



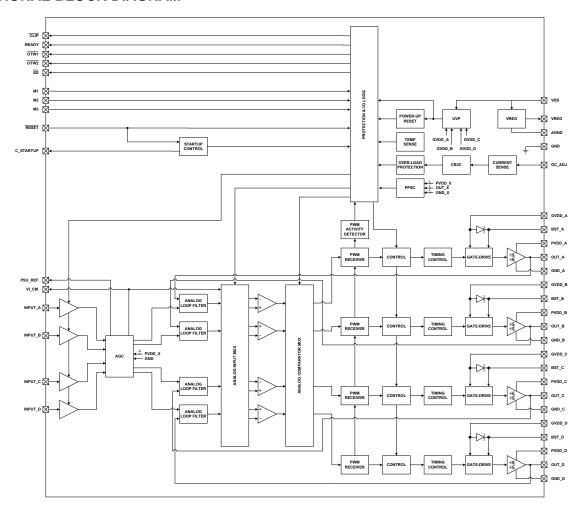
TYPICAL SYSTEM BLOCK DIAGRAM

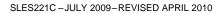


(1) Logic AND is inside or outside the microcontroller.

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FUNCTIONAL BLOCK DIAGRAM





AUDIO CHARACTERISTICS (BTL)

Audio performance is recorded as a chipset consisting of a TAS5518 PWM processor (modulation index limited to 97.7%) and a TAS5631 power stage. PCB and system configurations are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 50 V, GVDD_X = 12 V, R_L = 4 Ω , f_S = 384 kHz, R_{OC} = 22 k Ω , T_C = 75°C; output filter: L_{DEM} = 7 μ H, C_{DEM} = 680 nF, MODE = 000, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
		$R_L = 4 \Omega$, 10% THD+N, clipped input signal	300		
		$R_L = 6 \Omega$, 10% THD+N, clipped input signal	210		
D	Power output per channel	$R_L = 8 \Omega$, 10% THD+N, clipped input signal	160		w
Po		$R_L = 4 \Omega$, 1% THD+N, unclipped input signal	240		VV
		$R_L = 6 \Omega$, 1% THD+N, unclipped input signal	160		
		$R_L = 8 \Omega$, 1% THD+N, unclipped input signal	125		
THD+N	Total harmonic distortion + noise	1 W	0.03%		
V_n	Output integrated noise	A-weighted, TAS5518 modulator	180		μV
Vos	Output offset voltage	No signal	40	150	mV
SNR	Signal-to-noise ratio ⁽¹⁾	A-weighted, TAS5518 modulator	103		dB
DNR	Dynamic range	A-weighted, input level –60 dBFS using TAS5518 modulator	103		dB
P _{idle}	Power dissipation due to idle losses (I _{PVDD_X})	P _O = 0, four channels switching ⁽²⁾	3.9		W

⁽¹⁾ SNR is calculated relative to 1% THD-N output level.

AUDIO SPECIFICATION (Single-Ended Output)

Audio performance is recorded as a chipset consisting of a TAS5086 PWM processor (modulation index limited to 97.7%) and a TAS5631 power stage. PCB and system configurations are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 50 V, GVDD_X = 12 V, $R_L = 2 \Omega$, $R_S = 384 kHz$, $R_{OC} = 22 k\Omega$, $R_C = 75 °C$; output filter: $R_{DEM} = 7 \mu$ H, $R_C = 470 n$ F, MODE = 100, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
		$R_L = 2 \Omega$, 10%, THD+N, clipped input signal	145		
		$R_L = 3 \Omega$, 10%, THD+N, clipped input signal	100		
D	Dower output nor shorned	$R_L = 4 \Omega$, 10%, THD+N, clipped input signal	I, clipped input signal I, clipped input signal I, clipped input signal I, clipped input signal I	W	
Po	Power output per channel	$R_L = 2 \Omega$, 1% THD+N, unclipped input signal	110		VV
		$R_L = 3 \Omega$, 1% THD+N, unclipped input signal	75		
		$R_L = 4 \Omega$, 1% THD+N, unclipped input signal	55	145 100 75 110 75 55 0.04% 140 100	
THD+N	Total harmonic distortion + noise	1 W	0.04%		
V_n	Output integrated noise	A-weighted, TAS5086 modulator	140		μV
SNR	Signal-to-noise ratio ⁽¹⁾	A-weighted, TAS5086 modulator	100		dB
DNR	Dynamic range	A-weighted, input level –60 dBFS using TAS5086 modulator	100		dB
P _{idle}	Power dissipation due to idle losses (I _{PVDD_X})	P _O = 0, 4 channels switching ⁽²⁾	3		W

⁽¹⁾ SNR is calculated relative to 1% THD-N output level.

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⁽²⁾ Actual system idle losses also are affected by core losses of output inductors.

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AUDIO SPECIFICATION (PBTL)

Audio performance is recorded as a chipset consisting of a TAS5518 PWM processor (modulation index limited to 97.7%) and a TAS5631 power stage. PCB and system configurations are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 50 V, GVDD_X = 12 V, $R_L = 2 \Omega$, $R_S = 384 kHz$, $R_{OC} = 22 k\Omega$, $R_C = 75 °C$; output filter: $R_{DEM} = 7 \mu$ H, $R_{DEM} = 1 \mu$ F, MODE = 101-00, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN TYP MA	X UNIT
		$R_L = 2 \Omega$, 10%, THD+N, clipped input signal	600	
		$R_L = 3 \Omega$, 10%, THD+N, clipped input signal	400	
D	Davis autout an abancal	$R_L = 4 \Omega$, 10%, THD+N, unclipped input signal	300	W
Po	Power output per channel	$R_L = 2 \Omega$, 1% THD+N, unclipped input signal	480	VV
		$R_L = 3 \Omega$, 1% THD+N, unclipped input signal	310	
		$R_L = 4 \Omega$, 1% THD+N, unclipped input signal	ped input signal 600 ped input signal 400 slipped input signal 300 sped input signal 480 sped input signal 310 sped input signal 310 sped input signal 230 sped input signal 170	
THD+N	Total harmonic distortion + noise	1 W	0.03%	
V _n	Output integrated noise	A-weighted, TAS5518 modulator	170	μV
SNR	Signal-to-noise ratio ⁽¹⁾	A-weighted, TAS5518 modulator	103	dB
DNR	Dynamic range	A-weighted, input level –60 dBFS using TAS5518 modulator	103	dB
P _{idle}	Power dissipation due to idle losses (I _{PVDD_X})	P _O = 0, 4 channels switching ⁽²⁾	3.7	W

⁽¹⁾ SNR is calculated relative to 1% THD-N output level.

ELECTRICAL CHARACTERISTICS

 $PVDD_X = 50V$, $GVDD_X = 12 V$, VDD = 12V, T_C (case temperature) = $75^{\circ}C$, $f_S = 384$ kHz, unless otherwise specified.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL \	OLTAGE REGULATOR AND CURRENT CONSU	IMPTION	•		•	
VREG	Voltage regulator, only used as reference node, VREG	VDD = 12 V	3	3.3	3.6	٧
VI_CM	Analog comparator reference node, VI_CM		1.5	1.75	1.9	V
	VDD cumbly current	Operating, 50% duty cycle		22.5		A
I _{VDD}	VDD supply current	Idle, reset mode		22.5		mA
	Cata averalis averant man half heider	50% duty cycle		12.5		A
I _{GVDD_x}	Gate-supply current per half-bridge	Reset mode	1.5 1.75 1.9 22.5 22.5 12.5 1.5 1.5 7 19.5 7 60 100	mA		
I _{PVDD x}	Half-bridge idle current	50% duty cycle without output filter or load		19.5		mA
. , , , , , , , , , , , , , , , , , , ,	Ç .	Reset mode, no switching		750		μΑ
OUTPUT-ST	AGE MOSFETs					
	Drain-to-source resistance, low side (LS)	T _J = 25°C, excludes metallization		60	100	mΩ
R _{DS(on)}	Drain-to-source resistance, high side (HS)	resistance, GVDD = 12 V		60	5 1.9 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5	mΩ

Product Folder Link(s): TAS5631

⁽²⁾ Actual system idle losses are affected by core losses of output inductors.

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ELECTRICAL CHARACTERISTICS (continued)

 $PVDD_X = 50V$, $GVDD_X = 12 V$, VDD = 12V, T_C (case temperature) = $75^{\circ}C$, $f_S = 384$ kHz, unless otherwise specified.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I/O PROTECT	ION					
$V_{uvp,G}$	Undervoltage protection limit, GVDD_X			10		V
V _{uvp,hyst} (1)				0.6		V
OTW1 ⁽¹⁾	Overtemperature warning 1		95	100	105	°C
OTW2 ⁽¹⁾	Overtemperature warning 2		115	125	135	°C
OTW _{hyst} ⁽¹⁾	Temperature drop needed below OTW temperature for OTW to be inactive after OTW event			25		°C
OTE ⁽¹⁾	Overtemperature error		145	155	0.6 100 105 125 135 25 155 165 30 25 2.6 19 19 19 150 3 1.45 100 26 33 3.3 3.6	°C
OIE	OTE-OTW differential			30		°C
OTE _{HYST} (1)	A reset must occur for \$\overline{SD}\$ to be released following an OTE event			25		°C
OLPC	Overload protection counter	f _{PWM} = 384 kHz		2.6		ms
I _{oc}	Overcurrent limit response	Resistor – programmable, nominal peak current in 1- Ω load, 64-pin QFP package (PHD) $R_{OCP} = 22 \text{ k}\Omega$		19		А
	Overcurrent minit response	Resistor – programmable, nominal peak current in 1- Ω load, 44-pin PSOP3 package (DKD) R_{OCP} = 24 k Ω		19		A
	Overcurrent response time, latched	Resistor – programmable, nominal peak current in 1- Ω load, $R_{OCP} = 47 \ k\Omega$		19	1.45 100 105 105 105 105 105 105 105 105 10	А
Гост	Overcurrent response time	Time from application of short condition to Hi-Z of affected half-bridge		150		ns
I _{PD}	Internal pulldown resistor at output of each half-bridge	Connected when RESET is active to provide bootstrap charge. Not used in SE mode.		3		mA
STATIC DIGIT	AL SPECIFICATIONS					
V _{IH}	High-level input voltage	INDUT V MA MO MO DECET	1.9			V
V _{IL}	Low-level input voltage	INPUT_X, M1, M2, M3, RESET			1.45	V
I _{lkg}	Input leakage current				100	μА
OTW/SHUTDO	OWN (SD)					
R _{INT_PU}	Internal pullup resistance, OTW1 to VREG, OTW2 to VREG, SD to VREG		20	26	33	kΩ
V	High lavel syderity of the co	Internal pullup resistor	3	3.3	3.6	
V _{OH}	High-level output voltage	External pullup of 4.7 kΩ to 5 V	4.5		1.45 100 33 3.6 5	V
V _{OL}	Low-level output voltage	I _O = 4 mA		200	500	mV
FANOUT	Device fanout OTW1, OTW2, SD, CLIP, READY	No external pullup		30		devices

⁽¹⁾ Specified by design

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THD+N - Total Harmonic Distortion + Noise - %

0.005

20m

INSTRUMENTS

TYPICAL CHARACTERISTICS, BTL CONFIGURATION

Figure 1.

2

Po - Output Power - W

5 10 20

50 100

400

100m200m

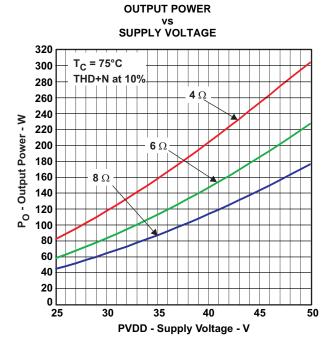


Figure 2.

UNCLIPPED OUTPUT POWER VS SUPPLY VOLTAGE

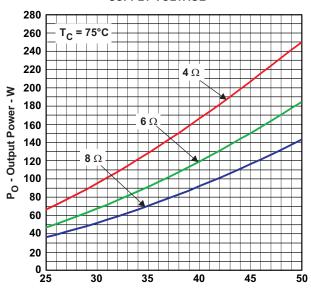


Figure 3.

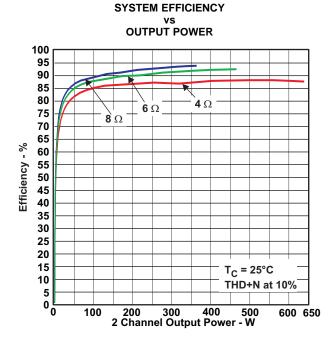
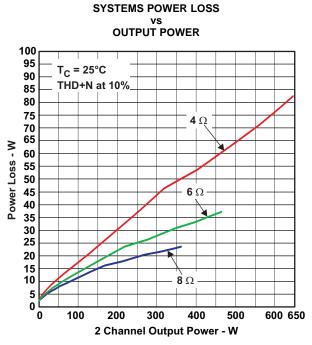


Figure 4.

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TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)





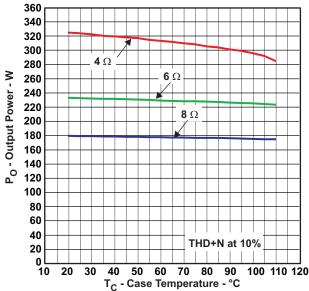
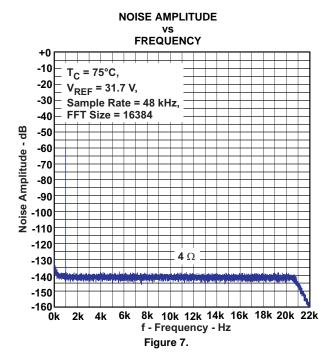


Figure 5. Figure 6.



INSTRUMENTS

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TYPICAL CHARACTERISTICS, SE CONFIGURATION

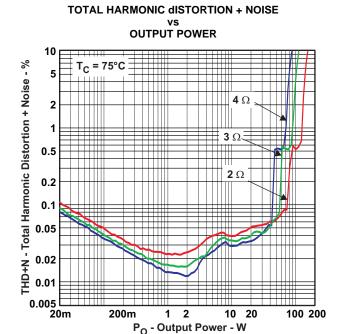
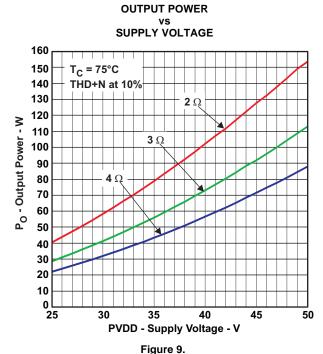
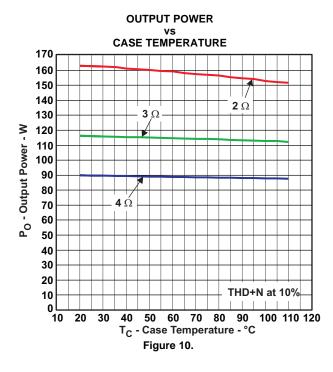


Figure 8.

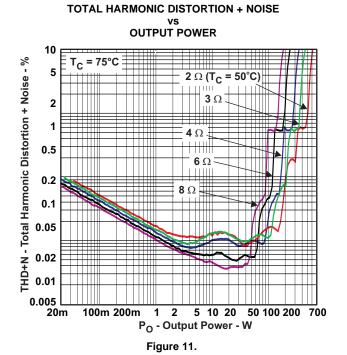


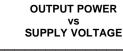


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TYPICAL CHARACTERISTICS, PBTL CONFIGURATION





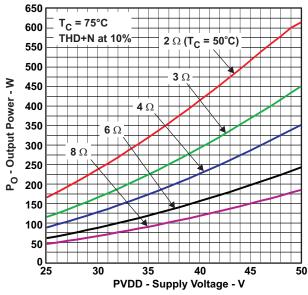
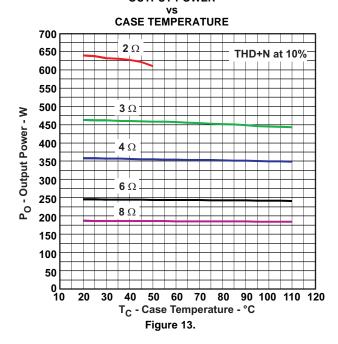


Figure 12.

OUTPUT POWER



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APPLICATION INFORMATION

PCB MATERIAL RECOMMENDATION

FR-4 2-oz. (70 μ m) glass epoxy material is recommended for use with the TAS5631. The use of this material can provide for higher power output, improved thermal performance, and better EMI margin (due to lower PCB trace inductance).

PVDD CAPACITOR RECOMMENDATION

The large capacitors used in conjunction with each full bridge are referred to as the PVDD capacitors. These capacitors should be selected for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well-designed system power supply, $1000~\mu F$, 63~V support more applications. The PVDD capacitors should be the low-ESR type because they are used in a circuit associated with high-speed switching.

DECOUPLING CAPACITOR RECOMMENDATION

To design an amplifier that has robust performance, passes regulatory requirements, and exhibits good audio performance, good-quality decoupling capacitors should be used. In practice, X7R should be used in this application.

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. This fact is particularly true in the selection of the 0.1- μ F capacitor that is placed on the power supply to each half-bridge. It must withstand the voltage overshoot of the PWM switching, the heat generated by the amplifier during high power output, and the ripple current created by high power output. A minimum voltage rating of 63 V is required for use with a 50-V power supply.

SYSTEM DESIGN RECOMMENDATIONS

The following schematics and PCB layouts illustrate best practices in the use of the TAS5631.

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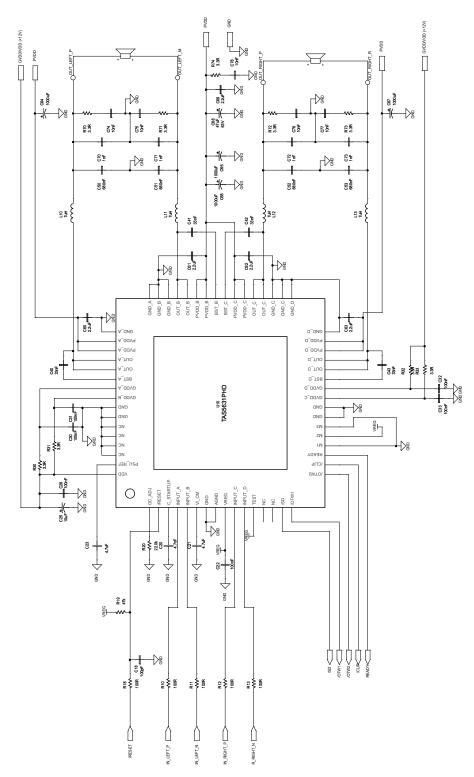


Figure 14. Typical Differential (2N) BTL Application With BD Modulation Filters



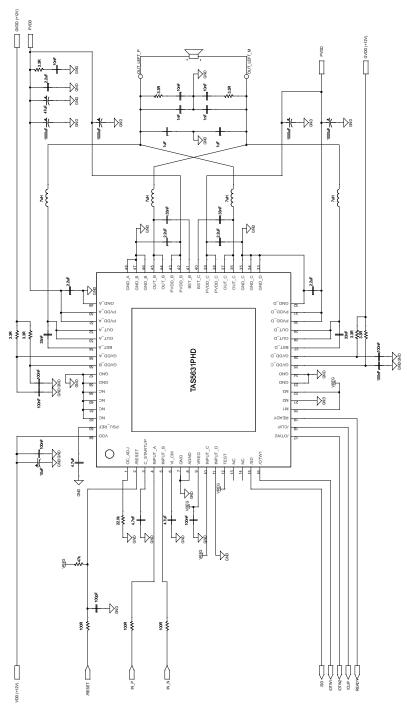


Figure 15. Typical (2N) PBTL Application With AD Modulation Filters



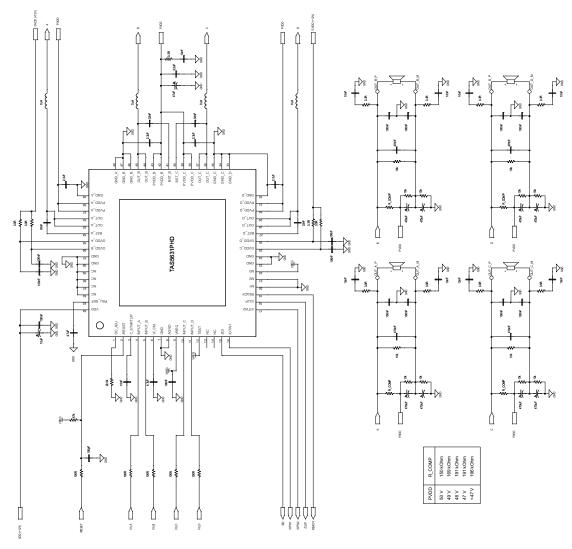


Figure 16. Typical SE Application

INSTRUMENTS

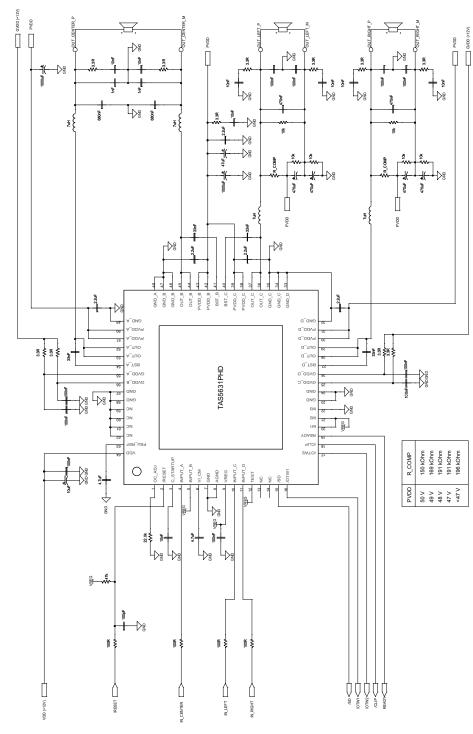


Figure 17. Typical 2.1 System (2N) Input BTL and (1N) Input SE Application

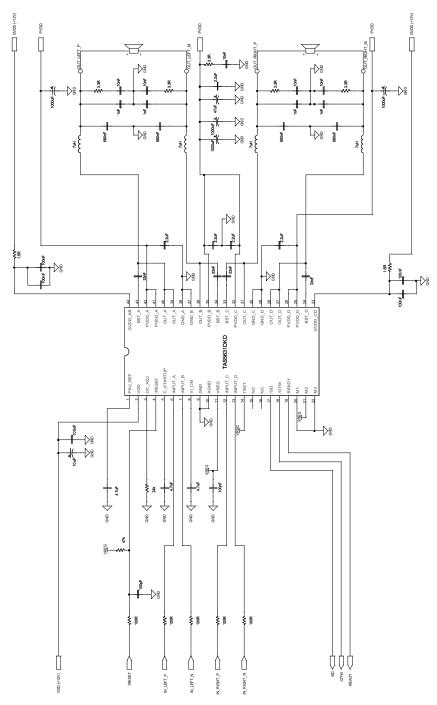


Figure 18. Typical Differential Input BTL Application With BD Modulation Filters, DKD Package

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THEORY OF OPERATION

POWER SUPPLIES

To facilitate system design, the TAS5631 needs only a 12-V supply in addition to the (typical) 50-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only an external capacitor for each half-bridge.

To provide outstanding electrical and acoustical characteristics, the PWM signal path, including gate drive and output stage, is designed as identical, independent half-bridges. For this reason, each half-bridge has separate gate-drive supply pins (GVDD_X), bootstrap pins (BST_X), and power-stage supply pins (PVDD_X). Furthermore, an additional pin (VDD) is provided as a supply for all common circuits. Although supplied from the same 12-V source, it is highly recommended to separate GVDD_A, GVDD_B, GVDD_C, GVDD_D, and VDD on the printed-circuit board (PCB) by RC filters (see application diagram for details). These RC filters provide the recommended high-frequency isolation. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided. (See reference board documentation for additional information.)

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 300 kHz to 4000 kHz, it is recommended to use 33-nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X pin is decoupled with a 2.2-µF ceramic capacitor placed as close as possible to each supply pin. It is recommended to follow the PCB layout of the TAS5631 reference design. For additional information on recommended power supply and required components, see the application diagrams in this data sheet.

The 12-V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 50-V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit. Moreover, the TAS5631 is fully protected against erroneous power-stage turnon due to parasitic gate charging. Thus, voltage-supply ramp rates (dV/dt) are non-critical within the specified range (see the Recommended Operating Conditions table of this data sheet).

SYSTEM POWER-UP/POWER-DOWN SEQUENCE

Powering Up

The TAS5631 does not require a power-up sequence. The outputs of the H-bridges remain in a high-impedance state until the gate-drive supply voltage (GVDD_X) and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the <u>Electrical Characteristics</u> table of this data sheet). Although not specifically required, it is recommended to hold RESET in a low state while powering up the device. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output.

Powering Down

The TAS5631 does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the Electrical Characteristics table of this data sheet). Although not specifically required, it is a good practice to hold RESET low during power down, thus preventing audible artifacts including pops or clicks.

Product Folder Link(s): TAS5631

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ERROR REPORTING

The \overline{SD} , $\overline{OTW1}$, and $\overline{OTW2}$ pins are active-low, open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown is signaled by the \overline{SD} pin going low. Likewise, \overline{OTW} and $\overline{OTW2}$ go low when the device junction temperature exceeds 125°C and $\overline{OTW1}$ goes low when the junction temperature exceeds 100°C (see the following table).

SD	OTW1	OTW2, OTW	DESCRIPTION
0	0	0	Overtemperature (OTE) or overload (OLP) or undervoltage (UVP)
0	0	1	Overload (OLP) or undervoltage (UVP). Junction temperature higher than 100°C (overtemperature warning)
0	1	1	Overload (OLP) or undervoltage (UVP)
1	0	0	Junction temperature higher than 125°C (overtemperature warning)
1	0	1	Junction temperature higher than 100°C (overtemperature warning)
1	1	1	Junction temperature lower than 100°C and no OLP or UVP faults (normal operation)

Note that asserting RESET low forces the SD signal high, independent of faults being present. TI recommends monitoring the OTW signal using the system microcontroller and responding to an overtemperature warning signal by, e.g., turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

To reduce external component count, an internal pullup resistor to 3.3 V is provided on both \overline{SD} and \overline{OTW} outputs. Level compliance for 5-V logic can be obtained by adding external pullup resistors to 5 V (see the Electrical Characteristics table of this data sheet for further specifications).

DEVICE PROTECTION SYSTEM

The TAS5631 contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overload, overtemperature, and undervoltage. The TAS5631 responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the ^{SD} pin low. In situations other than overload and overtemperature error (OTE), the device automatically recovers when the fault condition has been removed, i.e., the supply voltage has increased.

The device functions on errors, as shown in the following table.

BTL Mo	de	PBTL M	PBTL Mode SE Mode			
Local Error In	Local Error In Turns Off		Turns Off	Local Error In	Turns Off	
А		Α		Α	A . D	
В	A + B	В	A . D . C . D	В	A + B	
С	0 - 0	С	A + B + C + D	С	0 - 0	
D	C + D	D		D	C + D	

Bootstrap UVP does not shut down according to the table; it shuts down the respective half-bridge.

PIN-TO-PIN SHORT-CIRCUIT PROTECTION (PPSC)

The PPSC detection system protects the device from permanent damage if a power output pin (OUT_X) is shorted to GND_X or PVDD_X. For comparison, the OC protection system detects an overcurrent after the demodulation filter, whereas PPSC detects shorts directly at the pin before the filter. PPSC detection is performed at startup, i.e., when VDD is supplied; consequently, a short to either GND_X or PVDD_X after system startup does not activate the PPSC detection system. When PPSC detection is activated by a short on the output, all half-bridges are kept in a Hi-Z state until the short is removed; the device then continues the start-up sequence and starts switching. The detection is controlled globally by a two-step sequence. The first step ensures that there are no shorts from OUT_X to GND_X; the second step tests that there are no shorts from OUT X to PVDD X. The total duration of this process is roughly proportional to the capacitance of the

Product Folder Link(s): TAS5631



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output LC filter. The typical duration is <15 ms/ μ F. While the PPSC detection is in progress, \overline{SD} is kept low, and the device does not react to changes applied to the RESET pin. If no shorts are present, the PPSC detection passes, and \overline{SD} is released. A device reset does not start a new PPSC detection. PPSC detection is enabled in BTL and PBTL output configurations; the detection is not performed in SE mode. To make sure not to trip the PPSC detection system, it is recommended not to insert resistive load to GND_X or PVDD_X.

OVERTEMPERATURE PROTECTION

The two different package options have individual overtemperature protection schemes.

PHD Package

The TAS5631 PHD package option has a three-level temperature-protection system that asserts an active-low warning signal (OTW1) when the device junction temperature exceeds 100°C (typical), (OTW2) when the device junction temperature exceeds 125°C (typical) and, if the device junction temperature exceeds 155°C (typical), the device is <u>put</u> into thermal shutdown, resulting in all half-bridge outputs being set in <u>the high-impedance</u> (Hi-Z) state and SD being asserted low. OTE is latched in this case. To clear the OTE latch, RESET must be asserted. Thereafter, the device resumes normal operation.

DKD Package

The TAS5631 DKD package option has a two-level temperature-protection system that asserts an active-low warning signal (OTW) when the device junction temperature exceeds 125°C (typical) and, if the device junction temperature exceeds 155°C (typical), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and SD being asserted low. OTE is latched in this case. To clear the OTE latch, RESET must be asserted. Thereafter, the device resumes normal operation.

UNDERVOLTAGE PROTECTION (UVP) AND POWER-ON RESET (POR)

The UVP and POR circuits of the TAS5631 fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach values stated in the Electrical Characteristics table. Although GVDD_X and VDD are independently monitored, a supply-voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and SD being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

DEVICE RESET

When RESET is asserted low, all power-stage FETs in the four half-bridges are forced into a high-impedance (Hi-Z) state.

In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the reset input low enables weak pulldown of the half-bridge outputs. In the SE mode, the output is forced into a high-impedance state when asserting the reset input low. Asserting the reset input low removes any fault information to be signaled on the SD output, i.e., SD is forced high. A rising-edge transition on the reset input allows the device to resume operation after an overload fault. To ensure thermal reliability, the rising edge of reset must occur no sooner than 4 ms after the falling edge of SD.

SYSTEM DESIGN CONSIDERATIONS

A rising-edge transition on the reset input allows the device to execute the startup sequence and start switching.

Apply only audio when the state of READY is high; that starts and stops the amplifier without having audible artifacts that are heard in the output transducers. If an overcurrent protection event is introduced, the READY signal goes low; hence, filtering is needed if the signal is intended for audio muting in non-microcontroller systems.

The CLIP signal indicates that the output is approaching clipping. The signal can be used to either an audio volume decrease or intelligent power supply controlling a low and a high rail.

The device inverts the audio signal from input to output.

The VREG pin is not recommended to be used as a voltage source for external circuitry.

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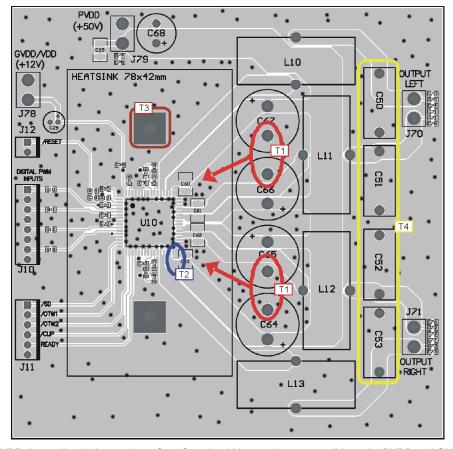
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PRINTED CIRCUIT BOARD RECOMMENDATION

Use an unbroken ground plane to have good low-impedance and -inductance return path to the power supply for power and audio signals. PCB layout, audio performance and EMI are linked closely together. The circuit contains high, fast-switching currents; therefore, care must be taken to prevent damaging voltage spikes. Routing for the audio input should be kept short and together with the accompanying audio source ground. It is important to keep a solid local ground area underneath the device to minimize ground bounce.

Netlist for this printed circuit board is generated from the schematic in Figure 14.



Note T1: PVDD decoupling bulk capacitors C60–C64 should be as close as possible to the PVDD and GND_X pins; the heat sink sets the distance. Wide traces should be routed on the top layer with direct connection to the pins and without going through vias. No vias or traces should be blocking the current path.

Note T2: Close decoupling of PVDD with low-impedance X7R ceramic capacitors is placed under the heat sink and close to the pins.

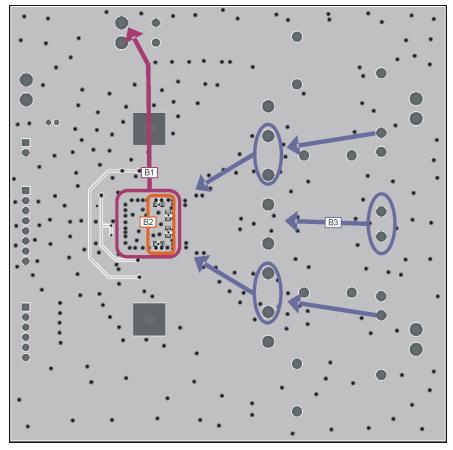
Note T3: Heat sink must have a good connection to PCB ground.

Note T4: Output filter capacitors must be linear in the applied voltage range, and preferably metal film types.

Figure 19. Printed Circuit Board - Top Layer

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Note B1: It is important to have a direct, low-impedance return path for high current back to the power supply. Keep impedance low from top to bottom side of PCB through a lot of ground vias.

Note B2: Bootstrap low-impedance X7R ceramic capacitors placed on bottom side provide a short low-inductance current loop.

Note B3: Return currents from bulk capacitors and output filter capacitors

Figure 20. Printed Circuit Board - Bottom Layer

REVISION HISTORY

Ch	nanges from Original (July 2009) to Revision A	Page
•	Deleted Product Preview from the PHD package	3
Ch	nanges from Revision A (September 2009) to Revision B	Page
•	Changed OLPC - Overload protection counter TYP value From: 1.3 To: 2.6 ms	10
Ch	nanges from Revision B (January 2010) to Revision C	Page
•	Deleted text form the last paragraph of the DESCRIPTION: Coupled with TI's class-G power-supply reference design for TAS563x, industry-leading levels of efficiency can be achieved.	1
•	Changed the front page illustration	1
	Changed Pin 41 From BST_C To BST_B in the PHD PACKAGE	





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TAS5631DKD	NRND	HSSOP	DKD	44	29	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	
TAS5631DKDR	NRND	HSSOP	DKD	44	500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	
TAS5631PHD	NRND	HTQFP	PHD	64	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-5A-260C-24 HR	
TAS5631PHDR	NRND	HTQFP	PHD	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-5A-260C-24 HR	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5631DKDR	HSSOP	DKD	44	500	330.0	24.4	14.7	16.4	4.0	20.0	24.0	Q1
TAS5631PHDR	HTQFP	PHD	64	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

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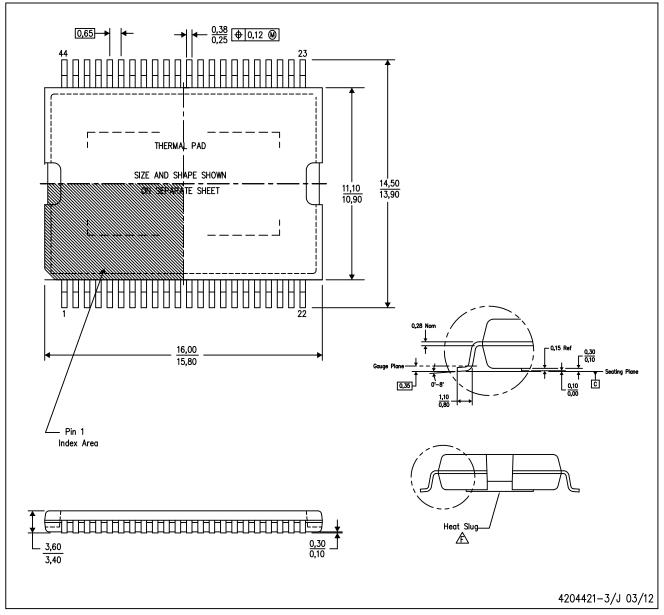


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5631DKDR	HSSOP	DKD	44	500	346.0	346.0	41.0
TAS5631PHDR	HTQFP	PHD	64	1000	346.0	346.0	41.0

DKD (R-PDSO-G44)

PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.15mm.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com www.ti.com.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- The package thermal performance is optimized for conductive cooling with attachment to an external heat sink.

PowerPAD is a trademark of Texas Instruments.



DKD (R-PDSO-G44)

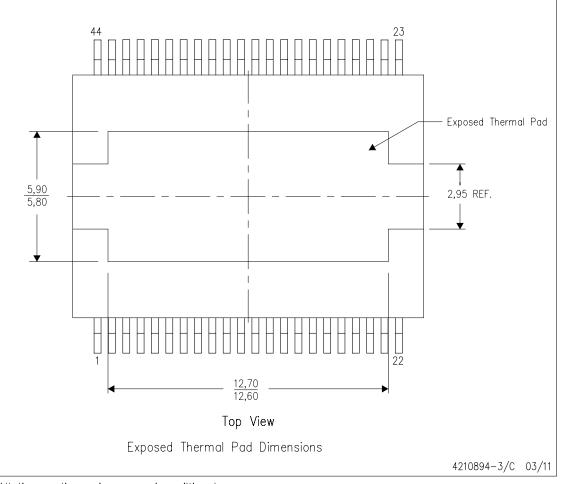
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

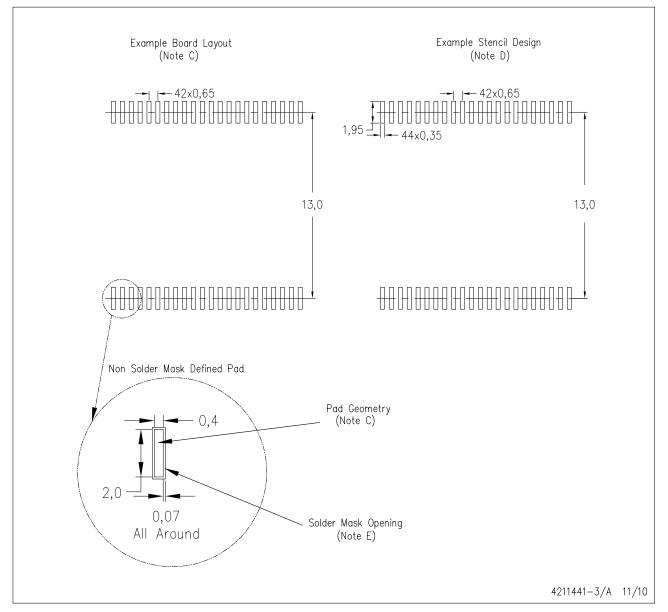
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: A. All linear dimensions are in millimeters

DKD (R-PDSO-G44)

PowerPAD™ PLASTIC SMALL OUTLINE



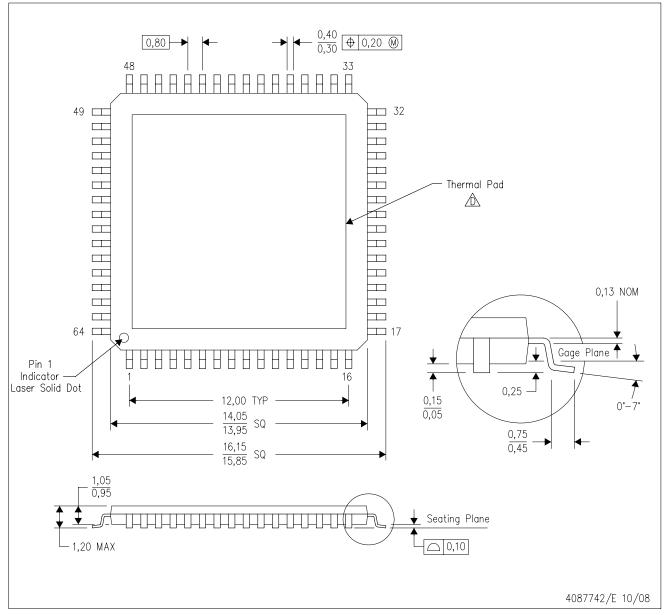
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.



PHD (S-PQFP-G64) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com http://www.ti.com. See the product data sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.



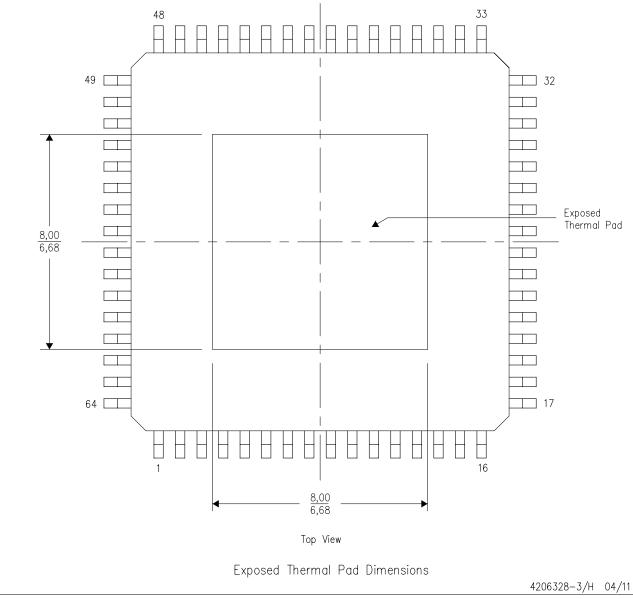
PHD (S-PQFP-G64) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)

THERMAL INFORMATION

This PowerPAD^m package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: A. All linear dimensions are in millimeters

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