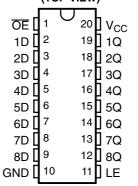
# SN54BCT573, SN74BCT573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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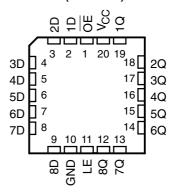
- Operating Voltage Range of 4.5 V to 5.5 V
- State-of-the-Art BiCMOS Design Significantly Reduces I<sub>CCZ</sub>
- Full Parallel Access for Loading

SN54BCT573 . . . J OR W PACKAGE SN74BCT573 . . . DW, N, OR NS PACKAGE (TOP VIEW)



- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

SN54BCT573 . . . FK PACKAGE (TOP VIEW)



#### description/ordering information

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'BCT573 devices are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels that were set up at the D inputs.

A buffered output-enable  $(\overline{OE})$  input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

OE does not affect internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

#### ORDERING INFORMATION

T <sub>A</sub>	PACKA	GE <sup>†</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube	SN74BCT573N	SN74BCT573N
000 to 7000	0010 0111	Tube	SN74BCT573DW	DOTE 70
0°C to 70°C	SOIC - DW	Tape and reel	SN74BCT573DWR	BCT573
	SOP - NS	Tape and reel	SN74BCT573NSR	BCT573
	CDIP – J	Tube	SNJ54BCT573J	SNJ54BCT573J
–55°C to 125°C	CFP – W	Tube	SNJ54BCT573W	SNJ54BCT573W
	LCCC - FK	Tube	SNJ54BCT573FK	SNJ54BCT573FK

<sup>&</sup>lt;sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



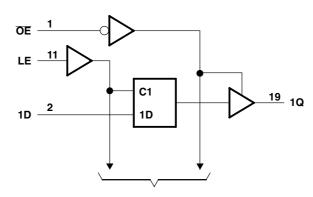
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# FUNCTION TABLE (each latch)

	INPUTS	OUTPUT	
ŌĒ	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	$Q_0$
Н	X	Χ	Z

#### logic diagram (positive logic)



To Seven Other Channels

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, Vo	
Voltage range applied to any output in the high state, VO	0.5 V to V <sub>CC</sub>
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
Current into any output in the low state: SN54BCT573	96 mA
SN74BCT573	
Package thermal impedance, θ <sub>JA</sub> (see Note 2): DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The package thermal impedance is calculated in accordance with JESD 51-7.



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#### recommended operating conditions (see Note 3)

		SN	54BCT5	73	SN74BCT573		UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
I <sub>IK</sub>	Input clamp current			-18			-18	mA
I <sub>OH</sub>	High-level output current			-12			-15	mA
I <sub>OL</sub>	Low-level output current			48			64	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

24244555		SN	54BCT5	73	SN	74BCT5	73		
PARAMETER	IEST	CONDITIONS	MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
V <sub>IK</sub>	$V_{CC} = 4.5 \text{ V},$	I <sub>I</sub> = -18 mA			-1.2			-1.2	V
		$I_{OH} = -3 \text{ mA}$	2.4	3.3		2.4	3.3		
$V_{OH}$	V <sub>CC</sub> = 4.5 V	$I_{OH} = -12 \text{ mA}$	2	3.2					V
		$I_{OH} = -15 \text{ mA}$				2	3.1		
.,	V 45.V	$I_{OL} = 48 \text{ mA}$		0.38	0.55				٧
$V_{OL}$	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 64 \text{ mA}$					0.42	0.55	<b>V</b>
I <sub>I</sub>	$V_{CC} = 5.5 V,$	V <sub>I</sub> = 5.5 V			0.4			0.4	mA
I <sub>IH</sub>	$V_{CC} = 5.5 \text{ V},$	$V_{I} = 2.7 \text{ V}$			20			20	μΑ
I <sub>IL</sub>	$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = 0.5 V			-0.6			-0.6	mA
I <sub>OS</sub> ‡	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 0	-100		-225	-100		-225	mA
I <sub>OZH</sub>	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 2.7 V			50			50	μΑ
I <sub>OZL</sub>	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 0.5 V			-50			-50	μΑ
I <sub>CCL</sub>	$V_{CC} = 5.5 \text{ V},$	Outputs open			62			62	mA
I <sub>CCH</sub>	$V_{CC} = 5.5 \text{ V},$	Outputs open			8			8	mA
I <sub>CCZ</sub>	$V_{CC} = 5.5 \text{ V},$	Outputs open			8			8	mA
C <sub>i</sub>	V <sub>CC</sub> = 5 V,	V <sub>I</sub> = 2.5 V or 0.5 V		5.5			5.5		pF
C <sub>o</sub>	V <sub>CC</sub> = 5 V,	V <sub>O</sub> = 2.5 V or 0.5 V		7.5			7.5		pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V <sub>CC</sub> =	: 5 V, 25°C	SN54B	CT573	SN74B	UNIT	
		MIN	MIN MAX MIN MAX MIN MA		MAX			
t <sub>w</sub>	Pulse duration, LE high	4		4		4		ns
t <sub>su</sub>	Setup time, data before LE $\downarrow$	1		2.5		1		ns
t <sub>h</sub>	Hold time, data after LE↓	4		4		4		ns

<sup>‡</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

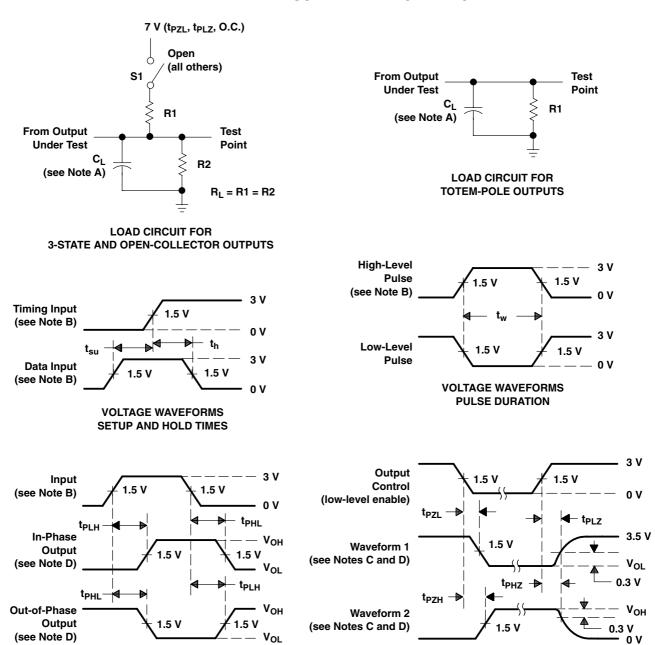
## SN54BCT573, SN74BCT573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO V <sub>CC</sub> = 5 T <sub>A</sub> = 25°			,	SN54B	CT573	SN74B	UNIT	
	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	_		2	5	7.2	1	9.8	2	8.4	
t <sub>PHL</sub>	D	Q	2.8	5.9	8.2	1.5	10.3	2.8	9.6	ns
t <sub>PLH</sub>		Q	2.4	6.1	7.2	2	9.7	2.4	8.1	
t <sub>PHL</sub>	LE		2.9	5.2	7.1	2	8.8	2.9	7.8	ns
t <sub>PZH</sub>	OF.	_	3	6.2	8.5	2.5	11	3	10.4	
t <sub>PZL</sub>	ŌĒ	Q	4.3	7.1	9.3	3.5	11.5	4.3	11	ns
t <sub>PHZ</sub>	OF.	Q	2.2	3.9	5.6	1.5	7.2	2.2	6	
t <sub>PLZ</sub>	ŌĒ		Q	1.7	3.6	5.2	1	7	1.7	6

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

**VOLTAGE WAVEFORMS** 

PROPAGATION DELAY TIMES (see Note D)

(see Note D)

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $t_f = t_f \leq$  2.5 ns, duty cycle = 50%.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.
- E. When measuring propagation delay times of 3-state outputs, switch S1 is open.
- F. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



0 V

**VOLTAGE WAVEFORMS** 

**ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS** 



5-Sep-2011

#### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-9583501Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9583501QRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
5962-9583501QSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
SN74BCT573DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74BCT573DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74BCT573DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74BCT573DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74BCT573DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74BCT573DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74BCT573N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74BCT573NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SNJ54BCT573FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54BCT573J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SNJ54BCT573W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



#### PACKAGE OPTION ADDENDUM

5-Sep-2011

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL. Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF SN54BCT573, SN74BCT573:

Catalog: SN74BCT573

Military: SN54BCT573

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

### PACKAGE MATERIALS INFORMATION

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#### TAPE AND REEL INFORMATION





		Dimension designed to accommodate the component width
		Dimension designed to accommodate the component length
P	<b>〈</b> 0	Dimension designed to accommodate the component thickness
		Overall width of the carrier tape
П	P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74BCT573DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74BCT573DWR	SOIC	DW	20	2000	346.0	346.0	41.0

### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# W (R-GDFP-F20)

# CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



# FK (S-CQCC-N\*\*)

### LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



# N (R-PDIP-T\*\*)

### PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

#### PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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