

February 2001 Revised May 2005

## 74LCX162373

# Low Voltage 16-Bit Transparent Latch with 5V Tolerant Inputs and Outputs and 26 $\Omega$ Series Resistor

#### **General Description**

The LCX162373 contains sixteen non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable  $(\overline{\text{OE}})$  is LOW. When  $\overline{\text{OE}}$  is HIGH, the outputs are in a high impedance state.

The LCX162373 is designed for low voltage (2.5V or 3.3V)  $V_{CC}$  applications with capability of interfacing to a 5V signal environment. The  $26\Omega$  series resistor in the output helps reduce output overshoot and undershoot.

The LCX162373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

#### **Features**

- 5V tolerant inputs and outputs
- 2.3V-3.6V V<sub>CC</sub> specifications provided
- $\blacksquare$  Equivalent 26 $\Omega$  series resistor outputs
- $\blacksquare$  6.2 ns t<sub>PD</sub> max (V<sub>CC</sub> = 3.3V), 20  $\mu$ A I<sub>CC</sub> max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- $\pm 12$  mA output drive ( $V_{CC} = 3.0V$ )
- Implements proprietary noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:

 $Human\ body\ model > 2000V$ 

Machine model > 200V

Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

**Note 1:** To ensure the high-impedance state during power up or down,  $\overline{\text{OE}}$  should be tied to  $V_{CC}$  through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

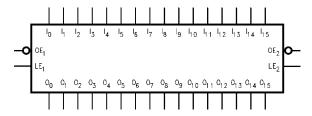
### **Ordering Code:**

Order Number	Package Number	Package Description
74LCX162373GX (Note 2)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]
74LCX162373MEA (Note 3)	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LCX162373MTD (Note 3)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Note 2: BGA package available in Tape and Reel only.

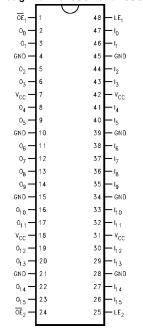
Note 3: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### **Logic Symbol**

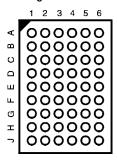


## **Connection Diagrams**

Pin Assignment for SSOP and TSSOP



Pin Assignment for FBGA



(Top Thru View)

## **Pin Descriptions**

Pin Names	Description
<del>OE</del> <sub>n</sub>	Output Enable Input (Active LOW)
LEn	Latch Enable Input
I <sub>0</sub> -I <sub>15</sub>	Inputs
O <sub>0</sub> -O <sub>15</sub>	Outputs
O <sub>0</sub> -O <sub>15</sub> NC	No Connect

## **FBGA Pin Assignments**

		1	2	3	4	5	6
	Α	O <sub>0</sub>	NC	OE <sub>1</sub>	LE <sub>1</sub>	NC	I <sub>0</sub>
Г	В	02	O <sub>1</sub>	NC	NC	I <sub>1</sub>	l <sub>2</sub>
Г	С	O <sub>4</sub>	O <sub>3</sub>	V <sub>CC</sub>	V <sub>CC</sub>	l <sub>3</sub>	I <sub>4</sub>
Г	D	O <sub>6</sub>	O <sub>5</sub>	GND	GND	l <sub>5</sub>	I <sub>6</sub>
	Е	Ο <sub>8</sub>	O <sub>7</sub>	GND	GND	I <sub>7</sub>	I <sub>8</sub>
Г	F	O <sub>10</sub>	O <sub>9</sub>	GND	GND	l <sub>9</sub>	I <sub>10</sub>
	G	O <sub>12</sub>	O <sub>11</sub>	V <sub>CC</sub>	V <sub>CC</sub>	I <sub>11</sub>	I <sub>12</sub>
	Н	O <sub>14</sub>	O <sub>13</sub>	NC	NC	I <sub>13</sub>	I <sub>14</sub>
	J	O <sub>15</sub>	NC	OE <sub>2</sub>	LE <sub>2</sub>	NC	I <sub>15</sub>

### **Truth Tables**

Inputs			Outputs
LE <sub>1</sub>	OE <sub>1</sub>	I <sub>0</sub> –I <sub>7</sub>	O <sub>0</sub> -O <sub>7</sub>
Х	Н	Х	Z
Н	L	L	L
Н	L	Н	Н
L	L	Χ	$O_0$

	Inputs		Outputs
LE <sub>2</sub>	OE <sub>2</sub>	I <sub>8</sub> -I <sub>15</sub>	O <sub>8</sub> -O <sub>15</sub>
Х	Н	Х	Z
Н	L	L	L
Н	L	Н	Н
L	L	X	O <sub>0</sub>

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial Z = High Impedance

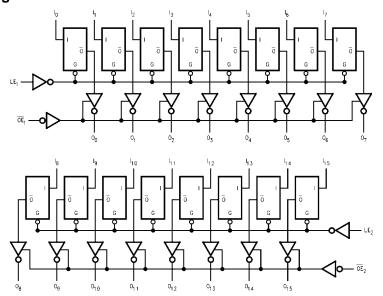
 $O_0$  = Previous  $O_0$  before HIGH-to-LOW transition of Latch Enable

## **Functional Description**

The LCX162373 contains sixteen D-type latches with 3-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE<sub>n</sub>) input is HIGH, data on the I<sub>n</sub> enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time

its I input changes. When  $LE_n$  is LOW, the latches store information that was present on the I inputs a setup time preceding the HIGH-to-LOW transition of  $LE_n$ . The 3-STATE standard outputs are controlled by the Output Enable  $(\overline{OE}_n)$  input. When  $\overline{OE}_n$  is LOW, the standard outputs are in the 2-state mode. When  $\overline{OE}_n$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

## **Logic Diagrams**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings(Note 4)

Symbol	Parameter	Value	Conditions	Units
V <sub>CC</sub>	Supply Voltage	-0.5 to +7.0		V
VI	DC Input Voltage	-0.5 to +7.0		V
Vo	DC Output Voltage	-0.5 to +7.0	Output in 3-STATE	V
		-0.5 to V <sub>CC</sub> + 0.5	Output in HIGH or LOW State (Note 5)	V
I <sub>IK</sub>	DC Input Diode Current	-50	V <sub>I</sub> < GND	mA
I <sub>OK</sub>	DC Output Diode Current	-50	V <sub>O</sub> < GND	mA
		+50	V <sub>O</sub> > V <sub>CC</sub>	IIIA
Io	DC Output Source/Sink Current	±50		mA
I <sub>CC</sub>	DC Supply Current per Supply Pin	±100		mA
I <sub>GND</sub>	DC Ground Current per Ground Pin	±100		mA
T <sub>STG</sub>	Storage Temperature	-65 to +150		°C

## **Recommended Operating Conditions** (Note 6)

Symbol	Parameter		Min	Max	Units
V <sub>CC</sub>	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	V
V <sub>I</sub>	Input Voltage		0	5.5	V
Vo	Output Voltage	HIGH or LOW State	0	V <sub>CC</sub>	V
		3-STATE	0	5.5	V
I <sub>OH</sub> /I <sub>OL</sub>	Output Current	$V_{CC} = 3.0V - 3.6V$		12	
		$V_{CC} = 2.7V - 3.0V$ $V_{CC} = 2.3V - 2.7V$		±8	mA
		$V_{CC} = 2.3V - 2.7V$		±4	
T <sub>A</sub>	Free-Air Operating Temperature		-40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V <sub>IN</sub> = 0.8V–2.0V, V <sub>CC</sub> = 3.0V		0	10	ns/V

Note 4: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 5:  $I_O$  Absolute Maximum Rating must be observed.

Note 6: Unused inputs must be held HIGH or LOW. They may not float.

## **DC Electrical Characteristics**

Symbol	Parameter	Conditions	v <sub>cc</sub>	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units
		Conditions	(V)	Min	Max	Oillis
V <sub>IH</sub>	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 - 3.6	2.0		V
V <sub>IL</sub>	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 - 3.6		8.0	V
V <sub>OH</sub>	HIGH Level Output Voltage	I <sub>OH</sub> = -100 μA	2.3 - 3.6	V <sub>CC</sub> - 0.2		
		$I_{OH} = -4 \text{ mA}$	2.3	1.8		
		$I_{OH} = -4 \text{ mA}$	2.7	2.2		V
		$I_{OH} = -6 \text{ mA}$	3.0	2.4		
		$I_{OH} = -8 \text{ mA}$	2.7	2.0		
		I <sub>OH</sub> = -12 mA	3.0	2.0		
V <sub>OL</sub>	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.3 - 3.6		0.2	
		I <sub>OL</sub> = 4 mA	2.3		0.6	
		$I_{OL} = 4 \text{ mA}$	2.7		0.4	V
		$I_{OL} = 6 \text{ mA}$	3.0		0.55	V
		I <sub>OL</sub> = 8 mA	2.7		0.6	
		I <sub>OL</sub> = 12 mA	3.0		8.0	
II	Input Leakage Current	$0 \leq V_I \leq 5.5V$	2.3 - 3.6		±5.0	μΑ
l <sub>OZ</sub>	3-STATE Output Leakage	$0 \le V_O \le 5.5V$	2.3 - 3.6		±5.0	
		$V_I = V_{IH}$ or $V_{IL}$				μА

## DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V <sub>CC</sub>	$T_A = -40^{\circ}$	C to ⊹85°C	Units
Cymbol	T di diffeter	Conditions	(V) Min Max		Jillo	
I <sub>OFF</sub>	Power-Off Leakage Current	$V_I$ or $V_O = 5.5V$	0		10	μА
I <sub>CC</sub>	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 – 3.6		20	μА
		$3.6V \le V_I, V_O \le 5.5V \text{ (Note 7)}$	2.3 – 3.6		±20	μΛ
$\Delta I_{CC}$	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> -0.6V	2.3 – 3.6		500	μΑ

Note 7: Outputs disabled or 3-STATE only.

## **AC Electrical Characteristics**

	Parameter	$T_A = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C},  R_L = 500\Omega$						
Symbol		$V_{CC} = 3.3V \pm 0.3V$		V <sub>CC</sub> =	V <sub>CC</sub> = 2.7V		$V_{CC}=2.5V\pm0.2V$	
Syllibol	Farameter	C <sub>L</sub> =	50 pF	C <sub>L</sub> =	50 pF	C <sub>L</sub> =	30 pF	Units
		Min	Max	Min	Max	Min	Max	
t <sub>PHL</sub>	Propagation Delay	1.5	6.2	1.5	6.7	1.5	7.4	ns
t <sub>PLH</sub>	I <sub>n</sub> to O <sub>n</sub>	1.5	6.2	1.5	6.7	1.5	7.4	115
t <sub>PHL</sub>	Propagation Delay	1.5	6.3	1.5	7.2	1.5	7.6	ns
t <sub>PLH</sub>	LE to O <sub>n</sub>	1.5	6.3	1.5	7.2	1.5	7.6	115
t <sub>PZL</sub>	Output Enable Time	1.5	6.9	1.5	7.3	1.5	9.0	ns
t <sub>PZH</sub>		1.5	6.9	1.5	7.3	1.5	9.0	115
t <sub>PLZ</sub>	Output Disable Time	1.5	6.0	1.5	6.3	1.5	7.2	ns
t <sub>PHZ</sub>		1.5	6.0	1.5	6.3	1.5	7.2	115
t <sub>S</sub>	Setup Time, I <sub>n</sub> to LE	2.5		2.5		3.0		ns
t <sub>H</sub>	Hold Time, I <sub>n</sub> to LE	1.5		1.5		2.0		ns
t <sub>W</sub>	LE Pulse Width	3.0		3.0		3.5		ns
toshl	Output to Output Skew (Note 8)		1.0					ns
toslh			1.0					113

Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## **Dynamic Switching Characteristics**

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C Typical	Units
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	3.3	0.35	
		$C_L = 30 \text{ pF}, V_{IH} = 2.5 \text{V}, V_{IL} = 0 \text{V}$	2.5	0.25	V
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$	3.3	-0.35	
		$C_L = 30 \text{ pF}, V_{IH} = 2.5 \text{V}, V_{IL} = 0 \text{V}$	2.5	-0.25	V

## Capacitance

Symbol	Parameter	Conditions	Typical	Units
C <sub>IN</sub>	Input Capacitance	$V_{CC} = Open, V_I = 0V \text{ or } V_{CC}$	7	pF
C <sub>OUT</sub>	Output Capacitance	$V_{CC} = 3.3V$ , $V_I = 0V$ or $V_{CC}$	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	$V_{CC} = 3.3V$ , $V_{I} = 0V$ or $V_{CC}$ , $f = 10$ MHz	20	pF

## AC LOADING and WAVEFORMS Generic for LCX Family

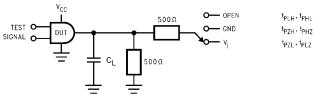
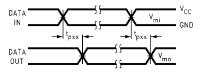
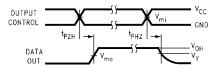


FIGURE 1. AC Test Circuit ( $C_L$  includes probe and jig capacitance)

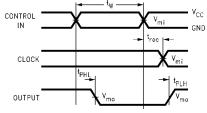
Test	Switch		
t <sub>PLH</sub> , t <sub>PHL</sub>	Open		
t <sub>PZL</sub> , t <sub>PLZ</sub>	6V at $V_{CC}$ = 3.3 ± 0.3V, and 2.7V $V_{CC}$ x 2 at $V_{CC}$ = 2.5 ± 0.2V		
t <sub>PZH</sub> , t <sub>PHZ</sub>	GND		



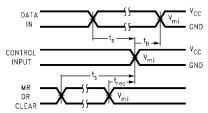
Waveform for Inverting and Non-Inverting Functions



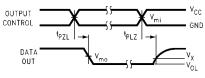
3-STATE Output High Enable and Disable Times for Logic



Propagation Delay. Pulse Width and  $t_{\rm rec}$  Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

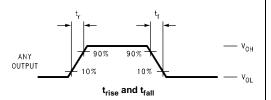
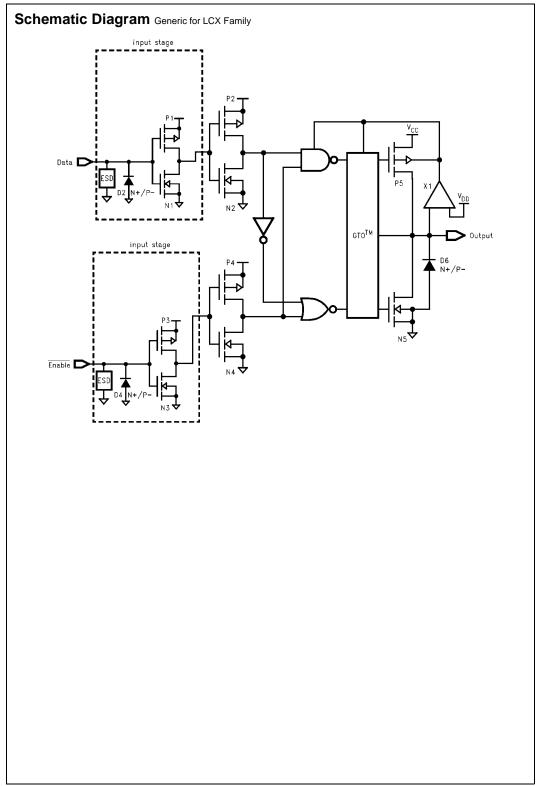
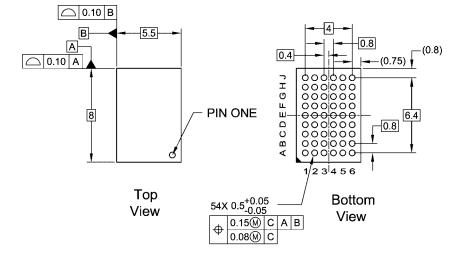


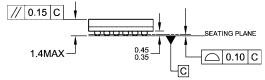
FIGURE 2. Waveforms (Input Characteristics; f =1MHz,  $t_r = t_f = 3ns$ )

Symbol	V <sub>CC</sub>			
	$3.3V \pm 0.3V$	2.7V	2.5V ± 0.2V	
$V_{mi}$	1.5V	1.5V	V <sub>CC</sub> /2	
$V_{mo}$	1.5V	1.5V	V <sub>CC</sub> /2	
V <sub>x</sub>	V <sub>OL</sub> + 0.3V	V <sub>OL</sub> + 0.3V	V <sub>OL</sub> + 0.15V	
V <sub>v</sub>	V <sub>OH</sub> – 0.3V	V <sub>OH</sub> – 0.3V	V <sub>OH</sub> – 0.15V	



## $\textbf{Physical Dimensions} \ \ \text{inches (millimeters) unless otherwise noted}$



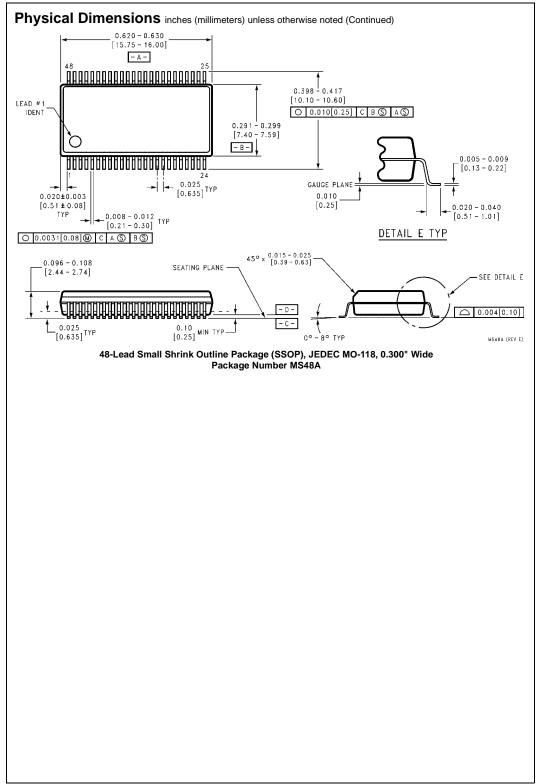


#### NOTES:

- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- **B. ALL DIMENSIONS IN MILLIMETERS**
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
  .35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
  D. DRAWING CONFORMS TO ASME Y14.5M-1994

#### BGA54ArevD

54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide Package Number BGA54A Preliminary



## Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 12.50±0.10 0.40 TYP -B-99. 9.20 8.10 50. O.2 C B A ALL LEAD TIPS PIN #1 IDENT 0.50 LAND PATTERN RECOMMENDATION 0.1 C SEE DETAIL A 0.90+0.15 ALL LEAD TIPS 0.09-0.20 0.10±0.05 0.17-0.27 0.50 ♦ 0.13@ A BS CS 12.00' TOP & BOTTOM DIMENSIONS ARE IN MILLIMETERS R0.16 GAGE PLANE 0.25 NOTES: A. CONFORMS TO JEDEC REGISTRATION MC-153, VARIATION ED, DATE 4/97. B. DIMENSIONS ARE IN MILLIMETERS. SEATING PLANE 0.60±0.10 1.00 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982. DETAIL A MTD48REVC

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48

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